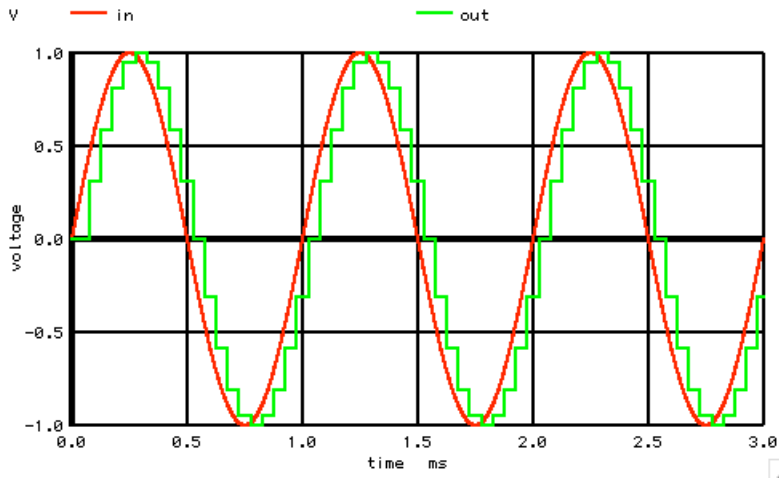


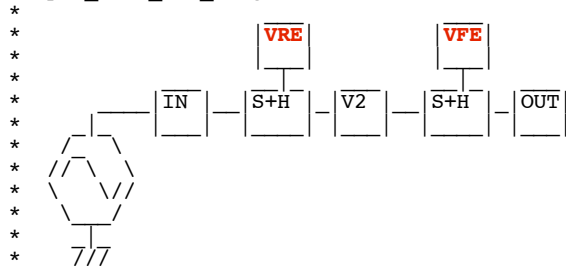
**Sample\_Hold\_Two\_Stage**

When two sample and hold circuits are connected using a two phase clock, the result is an analog delay element.



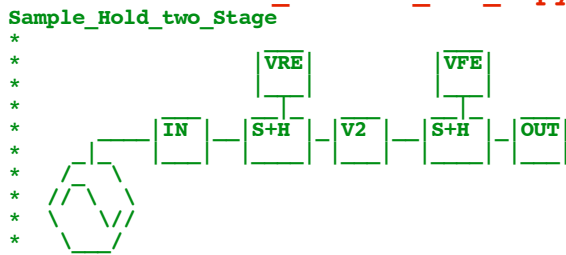
The idea is to input an analog voltage say on a rising edge and output that voltage on a falling edge. It can save a lot of trouble when inputs only read output when outputs are stationary. When outputs do move in voltages, inputs should all be open.

**Sample\_Hold\_two\_Stage**



```
*V SIN#   NODE_P NODE_N DC   VALUE   SIN(   V_DC   AC_MAG FREQ   DELAY  FDamp)
VIN#     IN      0      DC    0       SIN(    0     1     1k      )
*V PULSE# NODE_P NODE_N DC   VALUE   PULSE( VINIT  VPULSE TDELAY TRISE  TFALL  PWIDTH PERIOD )
VCLK     VCLK   0      DC    0       PULSE( 0     5     1n     1n     1n     25u    50u  )
XRE      VCLK   VRE     RISE_E
XFE      VCLK   VFE     FALL_E
XS_H     IN     V2      VRE   S_HOLD
XS_H2    V2     OUT     VFE   S_HOLD
.MODEL   SWP    SW(    VT=2.6 VH=.2  RON=1  ROFF=10MEG)
.control
*TRAN    TSTEP  TSTOP  TSTART TMAX
tran     1u    3m    0        1u
set      pensize = 2
plot    s_h:v1 s_h:v2
plot    in out
.endc
```

**Full\_Netlist\_For\_Copy\_Paste**



```

*
* 777
*
*V SIN#   NODE_P NODE_N DC   VALUE SIN( V_DC AC_MAG FREQ  DELAY FDamp)
VIN       IN     0     DC   0     SIN(  0    1    1k
*V PULSE# NODE_P NODE_N DC   VALUE PULSE( VINIT VPULSE TDELAY TRISE  TFALL  PWIDTH PERIOD )
VCLK     VCLK   0     DC   0     PULSE( 0    5    1n    1n    1n    25u    50u )
XRE      VCLK   VRE    RISE E
XFE      VCLK   VFE    FALL E
XS_H     IN     V2     VRE    S_HOLD
XS_H2    V2     OUT    VFE    S_HOLD
.MODEL   SWP    SW(    VT=2.6 VH=.2 RON=1 ROFF=10MEG)

```

```

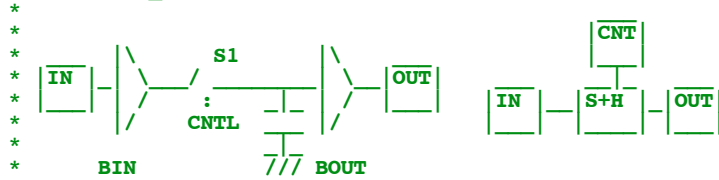
.control
*TRAN    TSTEP  TSTOP  TSTART TMAX
tran     1u     3m     0       1u
set      pensize = 2
plot     s_h:v1 s_h:v2
plot     in out
.endc

```

```

=====Sample_And_Hold=====
.SUBCKT  S_HOLD IN     OUT    CNT
*SXXXXXX N+     N-     NC+   NC-   MODEL    <ON><OFF>
S1       V1     V2     CNT   0     SWP
BIN      V1     0      V =   V(IN)
C1       V2     0      30n
BOUT     OUT    0      V =   V(V2)
.ENDS    S_HOLD

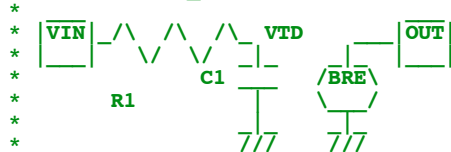
```



```

=====Rising Edge=====
.SUBCKT  RISE_E VIN    OUT
R1       VIN     VTD    100k
C1       VTD     0      1p
BRE      OUT     0      V = 5*u(V(VIN)-V(VTD)-.1)
.ENDS    RISE_E

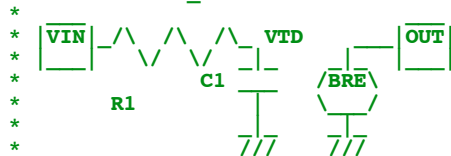
```



```

=====Falling Edge=====
.SUBCKT  FALL_E VIN    OUT
R1       VIN     VTD    100k
C1       VTD     0      1p
BRE      OUT     0      V = 5*u(V(VTD) -V(VIN)-.1)
.ENDS    FALL_E

```



.end

4.11.10 4.54PM  
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