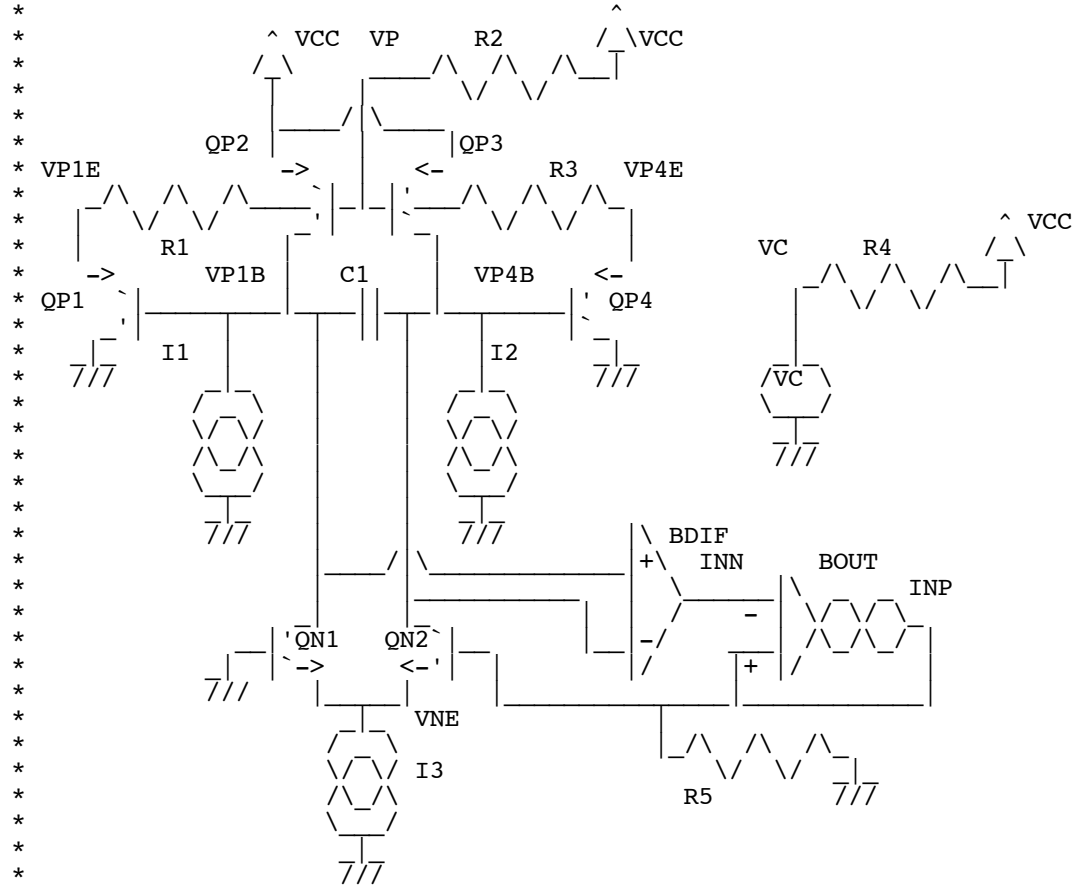


# DC CURRENT OSCILLATOR

\* dsauersanjose@aol.com 1/15/09  
 \* www.idea2ic.com



```

.OPTIONS GMIN = 1e-12
V PULSE VPL 0 PULSE( 0 1 1n 1n 1n .1m 1)
CSU VPL INP 1p
VCC VC 0 DC 5
R4 VC VCC 1

QN1 VP1B INP2 VNE NPNV
QN2 VP4B INP VNE NPNV
I3 VNE 0 5u

QP1 0 VP1B VP1E PNPL
QP2 VP1B VP VCC PNPL
QP3 VP4B VP VCC PNPL
QP4 0 VP4B VP4E PNPL
  
```

```

I1      VP1B  0    10u
I2      VP4B  0    10u
C0      VP1B  VP4B 20p
R1      VP    VP1E 20k
R2      VP    VCC  10k
R3      VP    VP4E 20k
BDIF    INN   0    V =    (v(VP1B) - v(VP4B))*.1
B OTA1  INP   0    I =    -1e-3*tanh(( v(INP)-v(INN) )/.001)
R5      INP   0    100
BINP2   INP2  0    V =    - V(INP)

BGATE   VG    0    V =    V(INP)*30+2.5
MP1     VD    VG    VCC2  VCC2  pchannel  w=6u l=1u
MN1     VD    VG    0      0      Nchannel  w=3u l=1u
R44     VC    VCC2  1

*.tran  10u   1m   0  10u   UIC

.MODEL  PNPL    PNP( BF=150 VAF=120 )
.MODEL  NPNV    NPN( BF=150 VAF=120 )
.model  nchannel nmos (level=3)
.model  pchannel pmos (level=3)

.control
set pensize = 2

tran    .1u   .1m   0  .1u
plot    v(vp1b) v(vp4b) title I3at5u
plot    v(inp) v(inn)
plot    v(vcc) -v(vc)
plot    v(vcc2) -v(vc) v(vcc) -v(vc)

alter   I3     dc = 10u
tran    .1u   .1m   0  .1u
plot    v(vp1b) v(vp4b) title I3at5u

op
dump
.endc

.end

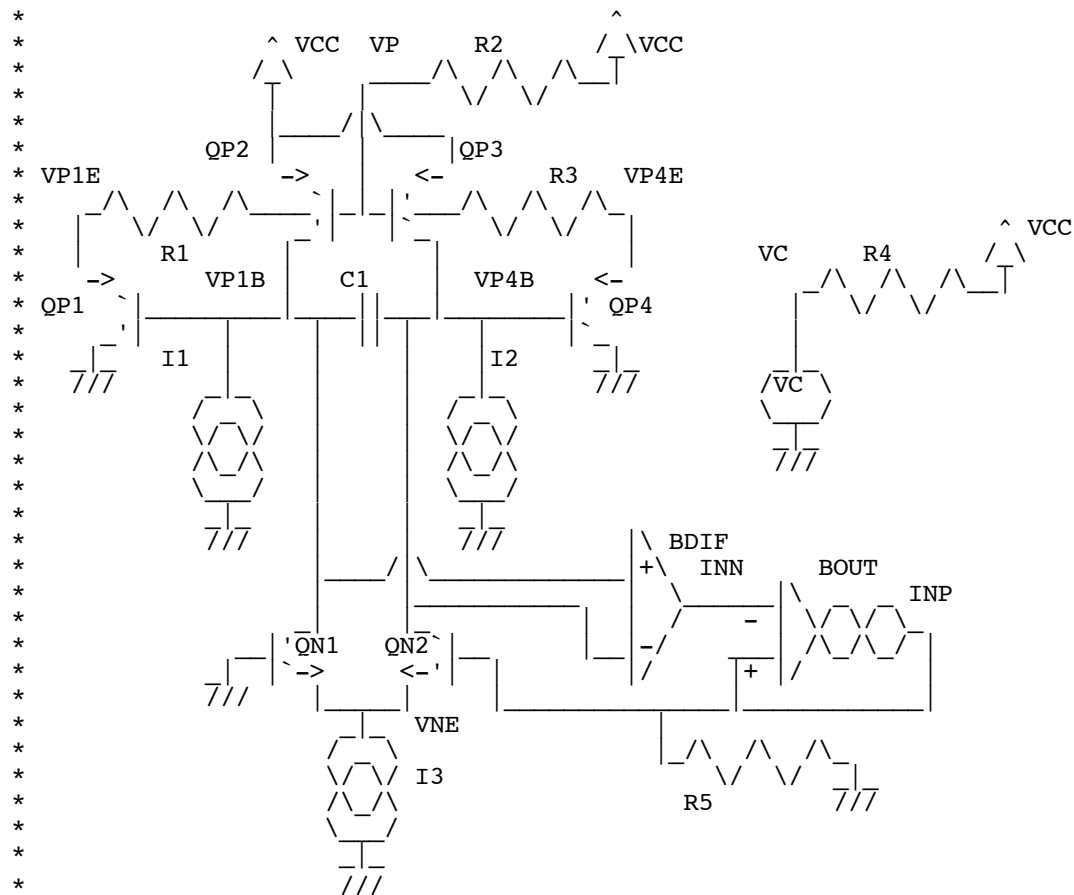
=====END_OF_SPICE=====

```

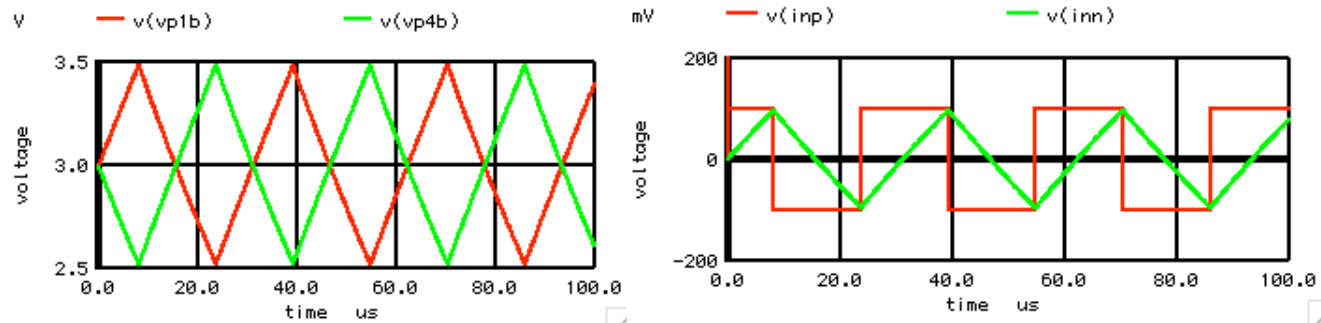
To Covert PDF to plain text click below  
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During the design of the LMC2001, the newly developed CS80 process was changing many of the rules that had been defining previous analog designs. One important change was the fact

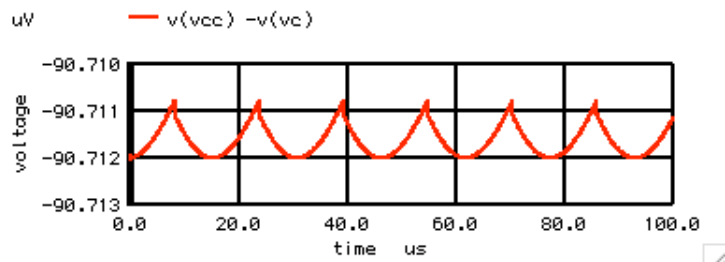
that a minimum geometry transistor was now about the same size as an emitter contact in a standard NPN transistor. This meant that a design engineer was no longer counting every single transistor. It also meant that transistors could now be run very fast at extremely low current.



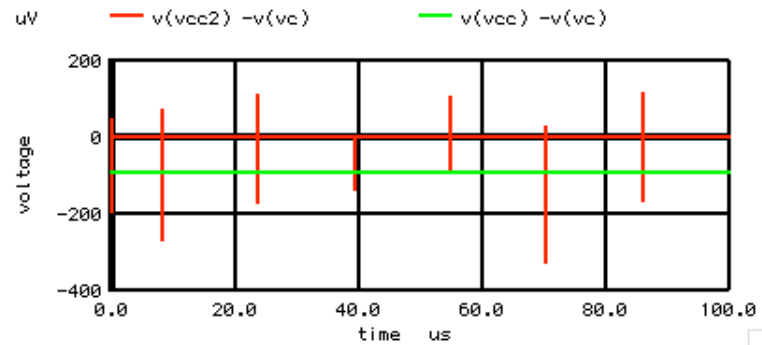
It was not uncommon for chopper amplifiers to display their chopper clock pretty much everywhere. The CS80 process made it possible to run all the chopper clock signal in a DC differential mode. This means that for every node voltage that goes up another equivalent voltage is going down.



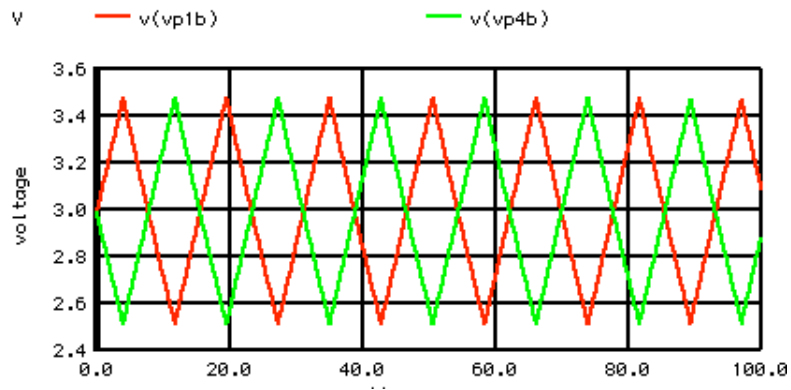
Looking at the supply current, early voltages produces a slight change in current as a function of clock cycle.



But to get a reference, the supply current of a minimum geometry CMOS inverter is shown along side.



It was common for chopper amplifiers to display chopper noise pretty much everywhere. Now was it possible to build a chopper which effectively drew DC current with no clock spikes on the supply?



**This oscillator can also be frequency modulated. If the clock were to get spread spectrum modulated, how well could the chopper clock be hidden?**