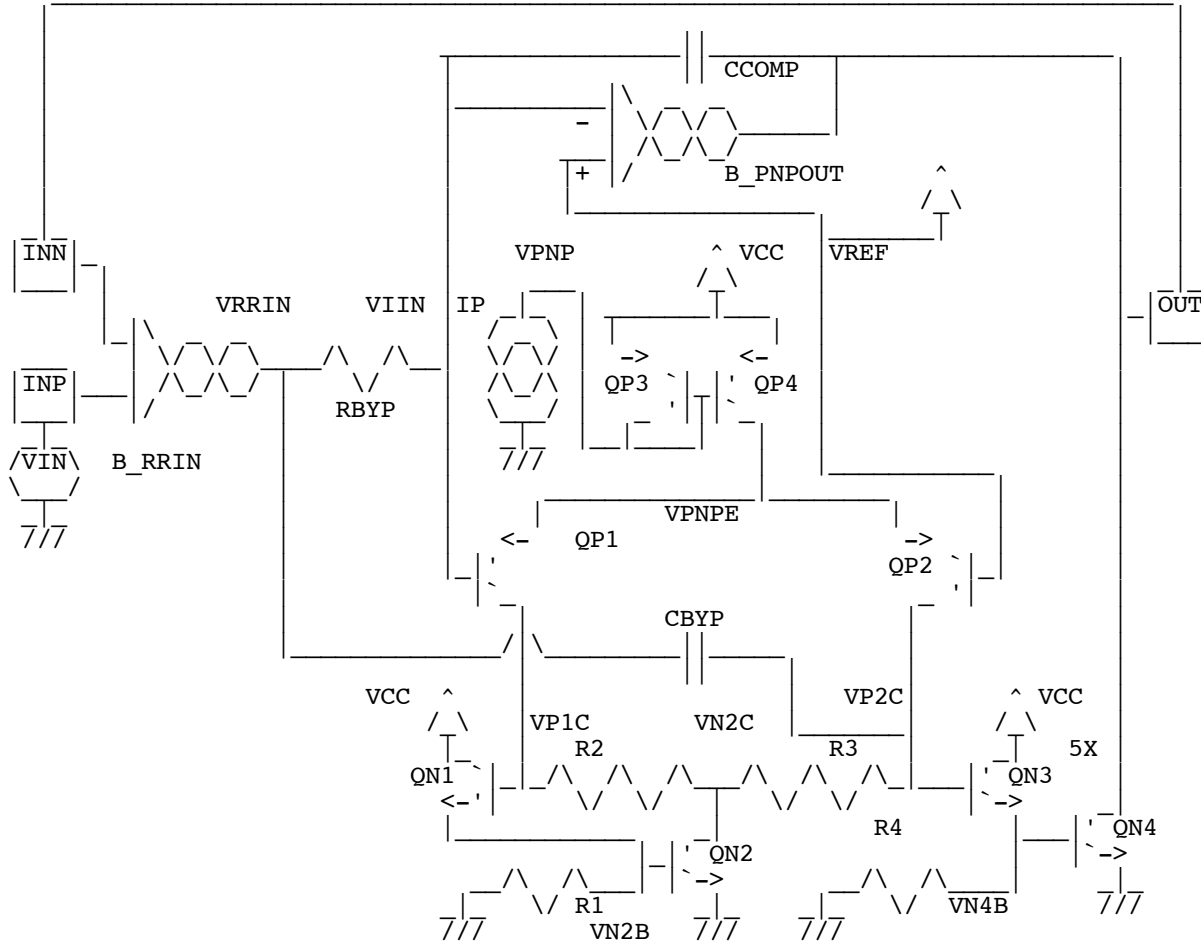


OUTPUT_STABILITY_REQUIREMENTS

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 * www.idea2ic.com

US Patent # 5546045



.OPTIONS method=gear GMIN=1e-18

VIN	INP	0	SIN(6	3	1K)	AC 1m
VREF	VREF	0	DC	6		
VCC	VCC	0	12			
IP	VPNP	0	40u			

```

B_RRIN   VRRIN   0      I = ( V(INP) - V(OUT) )/5000
RBYP     VRRIN   VIIN   1

QP1      VP1C    VIIN   VPNPE   PNPV    1
QP2      VP2C    VREF   VPNPE   PNPV    1
QP3      VPNPE   VPNP   VCC     PNPV    1
QP4      VPNP    VPNP   VCC     PNPV    1
QP5      VP5C    VPNP   VCC     PNPV    4
QN1      VCC     VP1C   VN2B    NPNV    1
QN2      VN2C    VN2B   0       NPNV    1
QN3      VCC     VP2C   VN4B    NPNV    1
QN4      OUT     VN4B   0       NPNV    10
R1       VN2B    0      20K
R2       VP1C    VN2C   5K
R3       VP2C    VN2C   5K
R4       VN4B    0      10K

CCOMP    OUT     VIIN   5p
BOTA     OUT     0      I = -200u

CBYP     VRRIN   VP2C   .2p

.tran    1u     2m     0       1u
.model   NPNV   npn     BF=150  CJE=.5p CJC=.3p CJS=1p
.model   PNPV   pnp     BF=60   CJE=.5p CJC=.3p CJS=1p

.control
run
set pensize = 2
ac       dec   10   10k   1000000K
let      gain = v(out)/( v(out)- v(inp) )
plot     dB(gain ) phase(gain) title WithNoByPass

alter    CBYP   capacitance = 2p
ac       dec   10   10k   1000000K
let      gain = v(out)/( v(out)- v(inp) )
plot     dB(gain ) phase(gain) title With2pFPass

alter    RBYP   resistance = 1K
ac       dec   10   10k   1000000K
let      gain = v(out)/( v(out)- v(inp) )
plot     dB(gain ) phase(gain) title With2pFand1KByPass

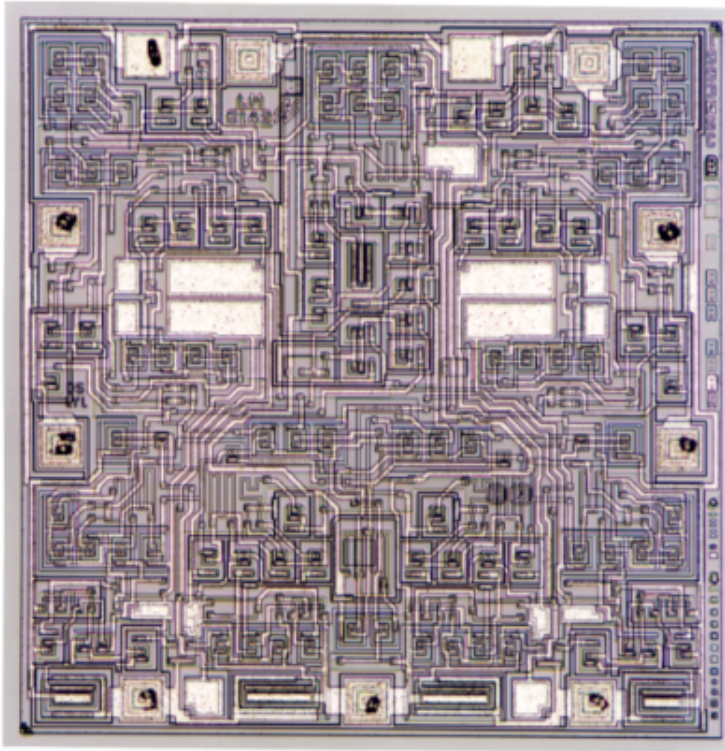
.endc
.end

* =====END=====

```

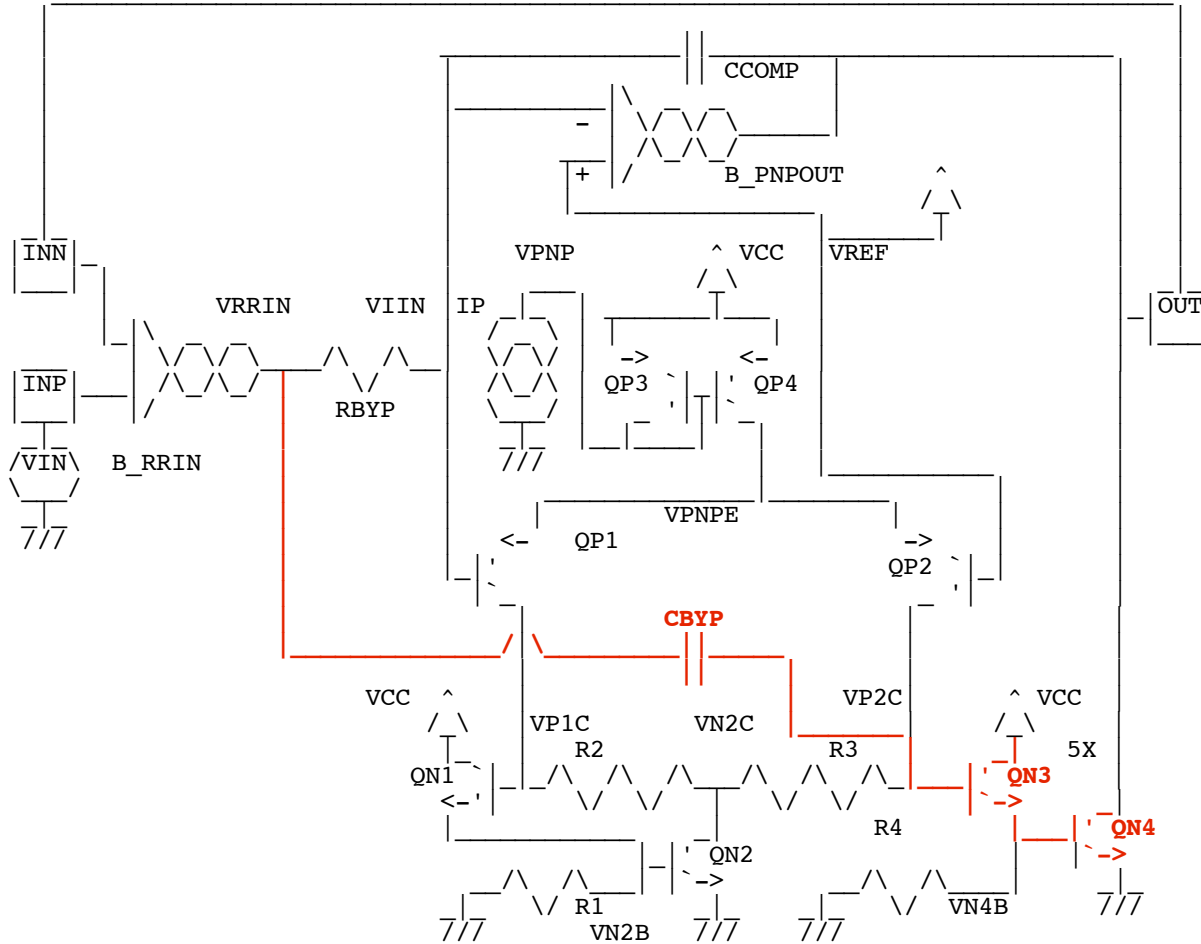
To Covert PDF to plain text click below
<http://www.fileformat.info/convert/doc/pdf2txt.htm>

The Actual output transistors in the LM6142 needs to conduct somewhere between one third to one half of the total supply current. This type of RRIO Op Amp is most unstable without a load since the ftau of the output transistors are being set by the stray emitter base capacitance and the emitter base current. This in itself created a problem in that it constrains the output transistors to be as small as possible. The die photo below shows the four output transistors for the two amplifiers at the bottom next to some pads and capacitors.

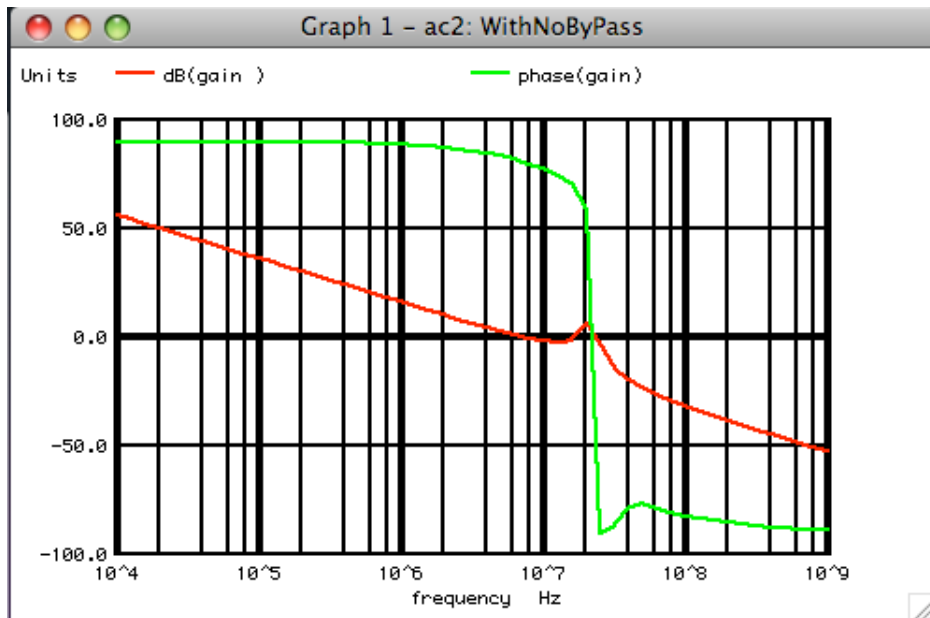


Usually output transistors are much more apparent, but in this case it is a very current starved design. Making the output transistors small also had some tradeoff in terms of beta rolling off the maximum output current available.

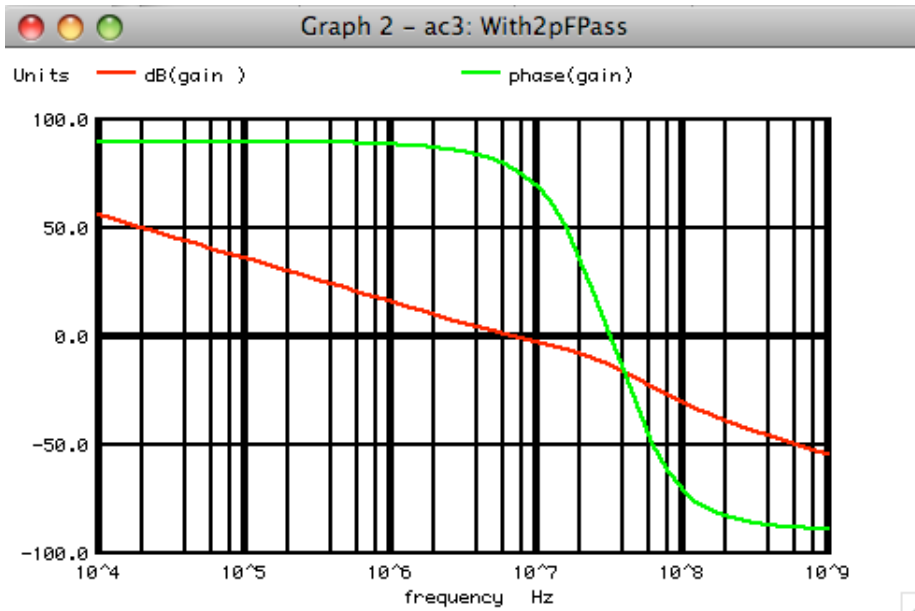
US Patent # 5546045



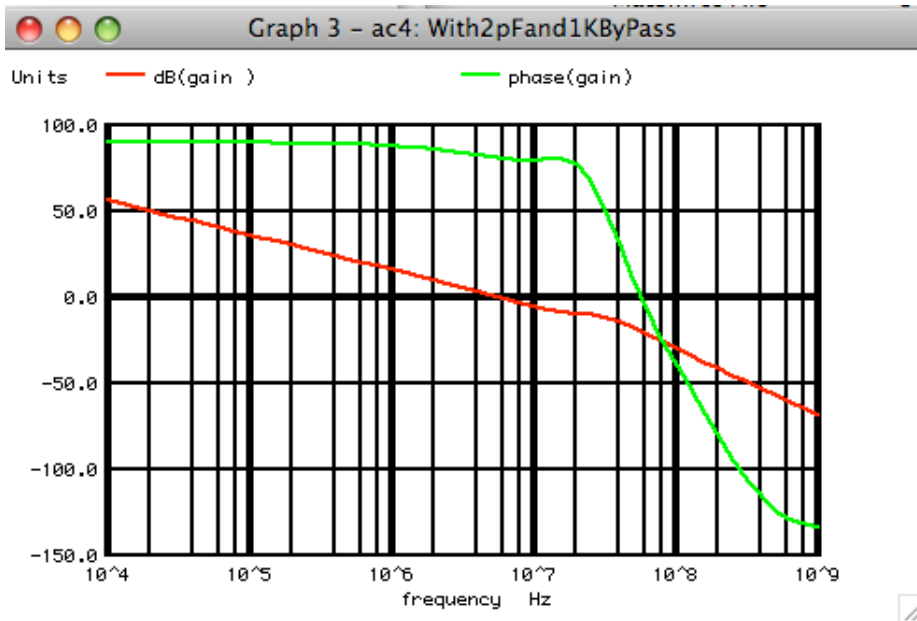
The same method to reducing signal path was needed to meet the supply current stability requirements. The simulation below shows that the output stage is just getting ready to oscillate when CBYP is only .2pF.



When CBYP is increased to 2pF, the high frequency signal path is essentially just CBYP and QN3 and QN4. Even though QN4 is drawing only 200uA and has a stray emitter base capacitance of about 2.5pF, the simulation below suggest stability.



It appears to be possible to reduce phase delay at higher frequencies even more by additionally changing the value of RBYP from 1 Ohm to 1KOhm.



This feature was effectively used to meet the unity gain stability requirement with 200pF loads.