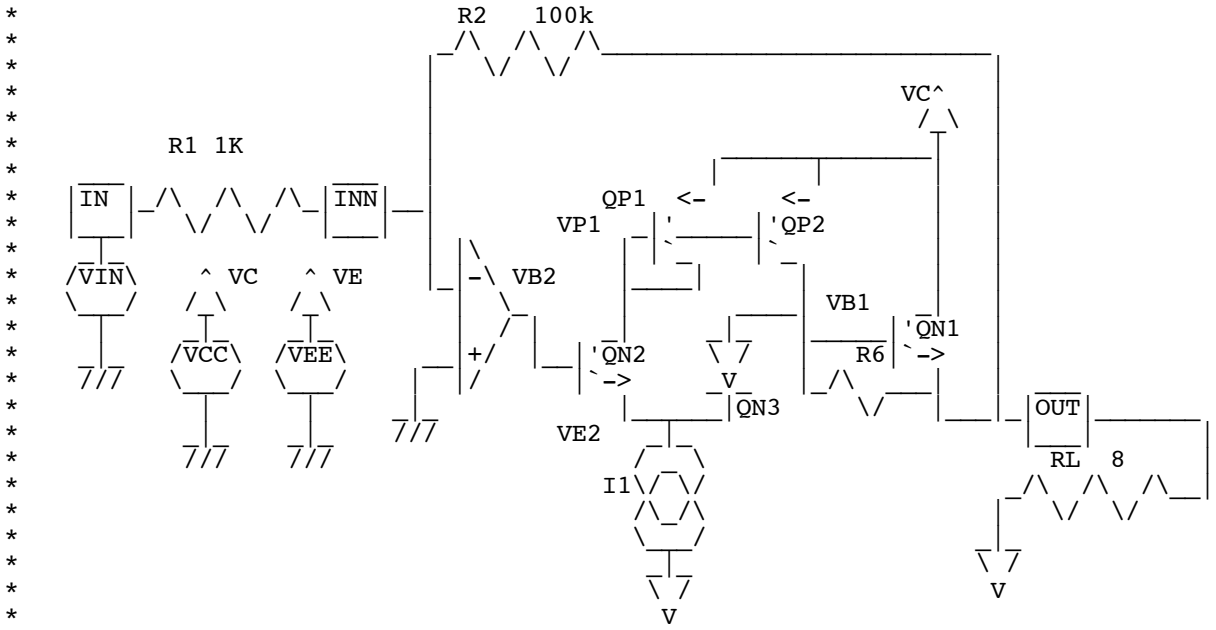
Top_Side_Invention

* dsauersanjose@aol.com 8/15/08
* www.idea2ic.com
* US PATENT # 4122401

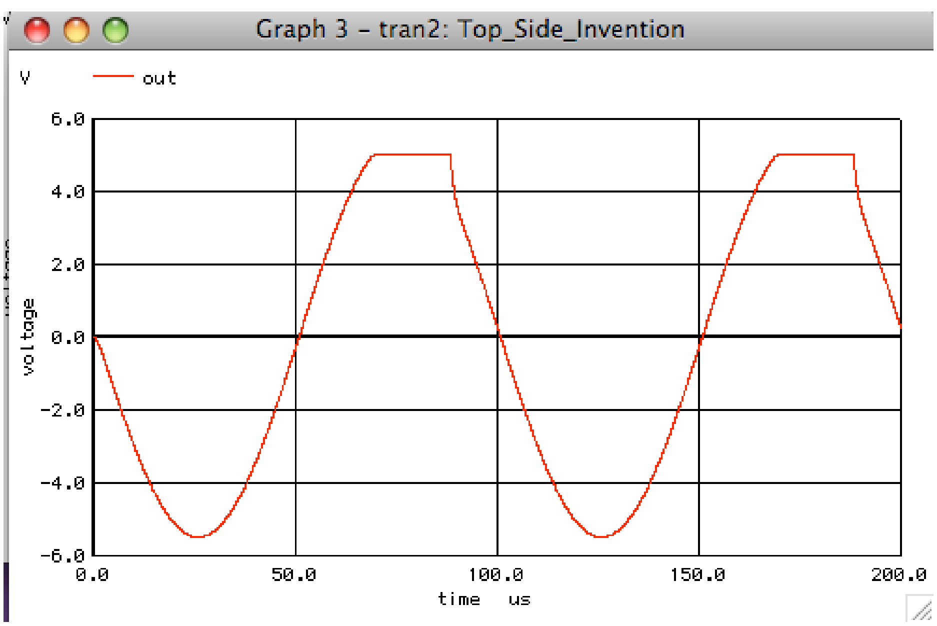


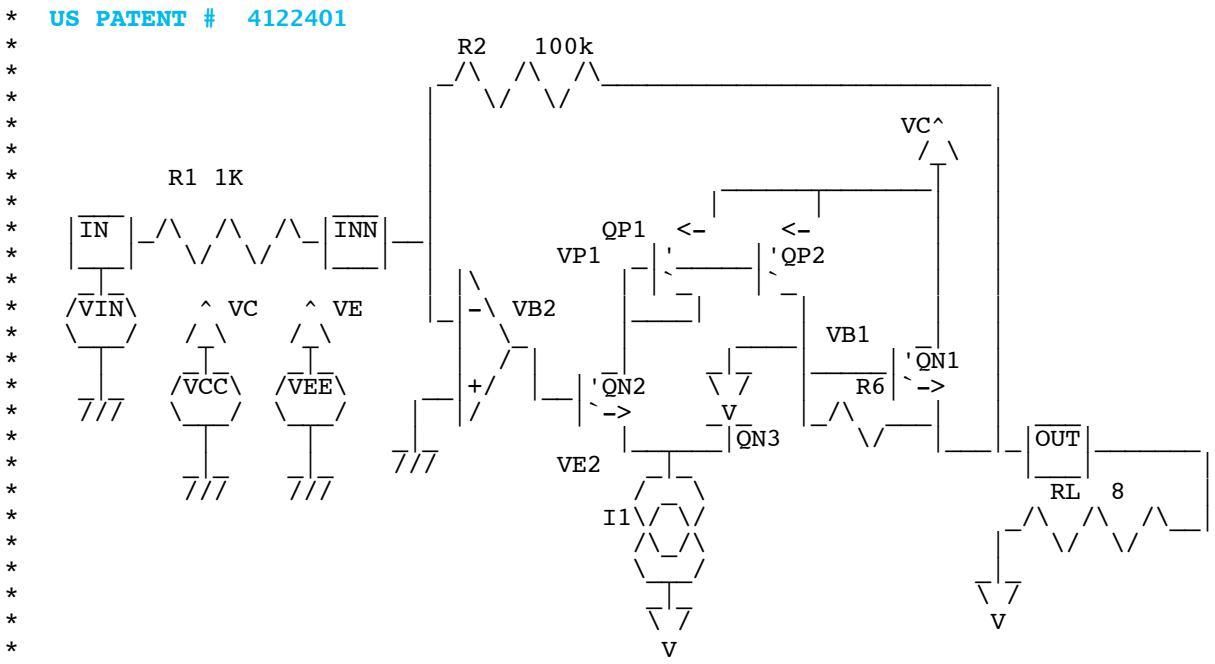

```
.OPTIONS  GMIN=1e-15 METHOD=gear ABSTOL=1e-15 temp=27 set srcsteps = 1


VCC     VC      0     DC      6
VEE     VE      0     DC      -7
VIN     IN      0     DC      0    SIN( 0 55m 10k 1n )
R1      IN      INN   1k
R2      INN     OUT   100k
X_OPA   INN     0     OUT1    OP_AMP
R3      OUT1    VB2   1k
QN2     VP1     VB2   VE2     NPNP 5
QP1     VP1     VP1   VC      PNPP 1
QP2     VB1     VP1   VC      PNPP 30
QN3     VB1     VB1   VE2     NPNP 5
I1      VE2     VE    8m
QN1     VC      VB1   OUT     NPNP 400
R6      VB1     OUT   20k
RL      OUT     VE    4

.tran    10n   .2m    0       10n


.control
run
set     pensize = 1
plot    out vb1 vc
plot    out
.endc


.SUBCKT  OP_AMP INN   INP  OUT
EGBUF    VDIFF  0     INN  INP  1
RGM1     VDIFF  VDIFF2 1k
RGM2     VDIFF2 VGND2  1k
CBW      OUT    VGND2  4p
CSP      VDIFF2 0      4f
EGOUT    OUT    0     VGND2 0    -100000000
.ENDS    OP_AMP
```

```
*
*                        CBW _|___|                .SUBCKT OP_AMP INN INP OUT
*                 VDIFF      ___  |____|OUT|
*                    ___/\   \/___|         |       |\
*    |INN|__       _|    \ RGM VGND /_|_\          |INN|__|  \
*    |___|  |_   /    \          |EGOUT|           |___|  |   \
*             + |EGBUF|      __|  \    /                 |OPA\_|OUT|
*               |     |        |   \__/                  |   /  |___|
*    |INP|__|‾  \____/         |    |   GAIN=-1M   |INP|__|  /
*    |___|           |GAIN=1  ///   |              |___|  | /
*                    |             ///                    |/
*                   ///                    ODB = 20MHz
*
.model     NPNP    NPN( BF=210  IS=1e-17   RC= 100)

.model     PNPP    PNP(   BF=30   IS=1e-17 IKF=7.6e-3  ITF=1.70E-6
+ CJE= 4e-12      CJC=1.826E-12   CJS=1.826E-12
+ TF=.03e-6   PTF=205       )

.end
```

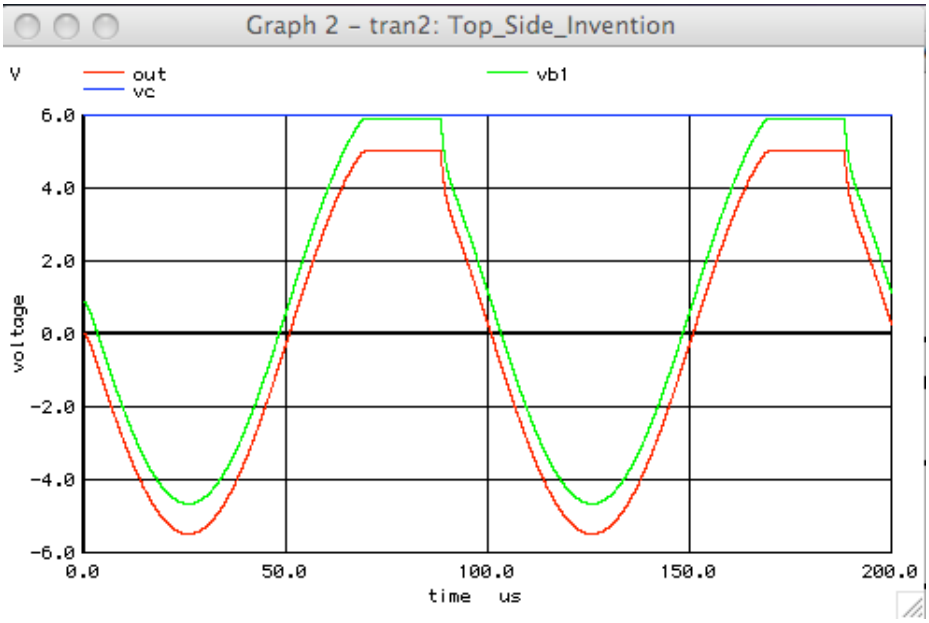
======Top_Side_Invention=============

What can make a topside composite unstable is the fact that there is a NPN and lateral PNP in a loop with a current loop gain of the produce of both the betas.Being that the beta of the NPN is several hundred, removing it from the loop should make the loop several hundred times more stable.





The invention shown above uses a diode and current source to make a smaller current loop. Transistor QN1 still needs to put out 5Amps. That means QP2 will still have to have as much current gain as possible. QP1 is only added to sort of stabilize AB bias. The 5Amps output requirement still needs current gain from both the PNP and NPN.
But both current gains don't have to be put together in the same loop.



With the top side composite much more stable, the stablity situation for the bottom side composite remains about the same.

***#1=============WinSpiceVersion=================**

```
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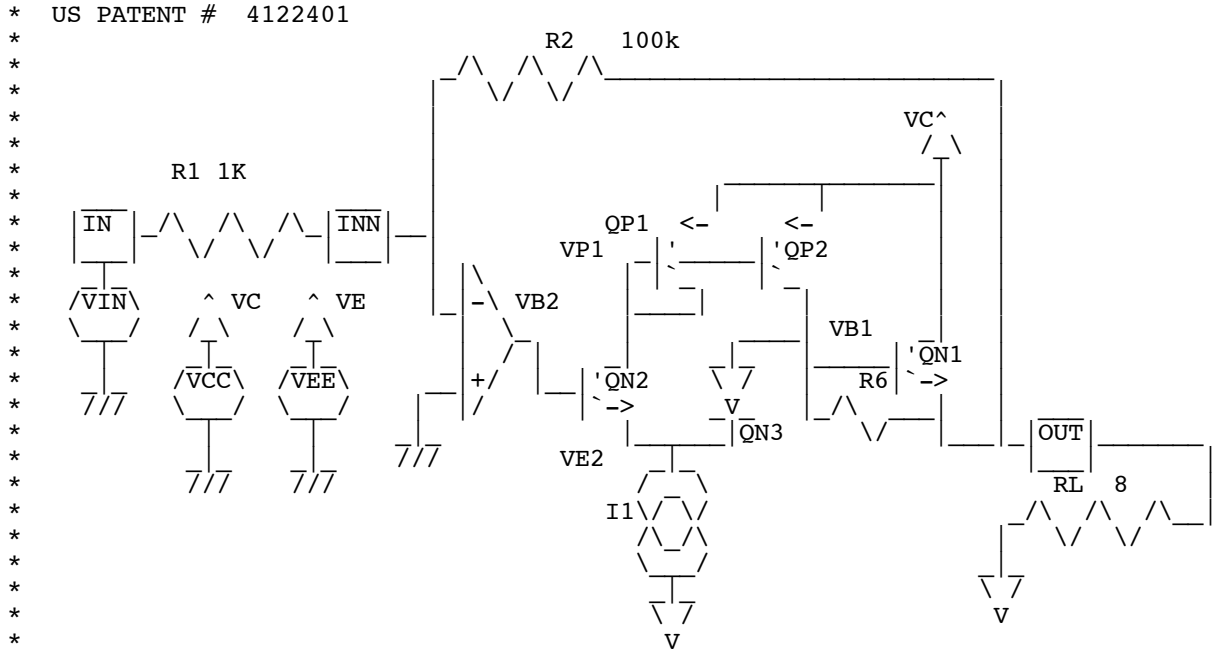


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R3      OUT1    VB2   1k
QN2     VP1     VB2   VE2     NPNP 5
QP1     VP1     VP1   VC      PNPP 1
QP2     VB1     VP1   VC      PNPP 30
QN3     VB1     VB1   VE2     NPNP 5
I1      VE2     VE    8m
QN1     VC      VB1   OUT     NPNP 400
R6      VB1     OUT   20k
RL      OUT     VE    4
.tran    10n   .2m    0       10n

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plot    out

.endc


.SUBCKT  OP_AMP INN   INP  OUT
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RGM1     VDIFF  VDIFF2 1k
RGM2     VDIFF2 VGND2  1k
CBW      OUT    VGND2  4p
CSP      VDIFF2 0      4f
EGOUT    OUT    0     VGND2 0    -100000000
.ENDS    OP_AMP

*
*                      CBW                .SUBCKT OP_AMP INN INP OUT
```

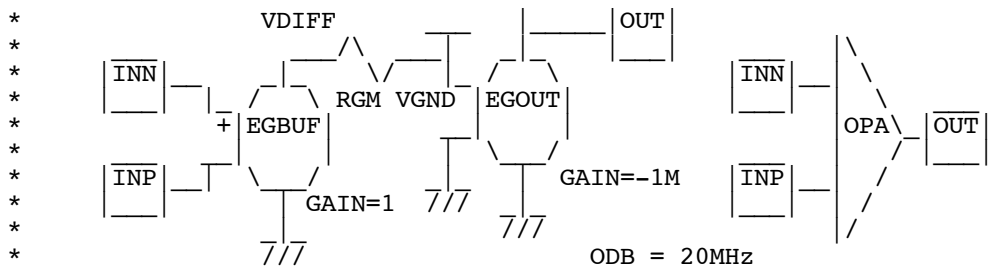


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