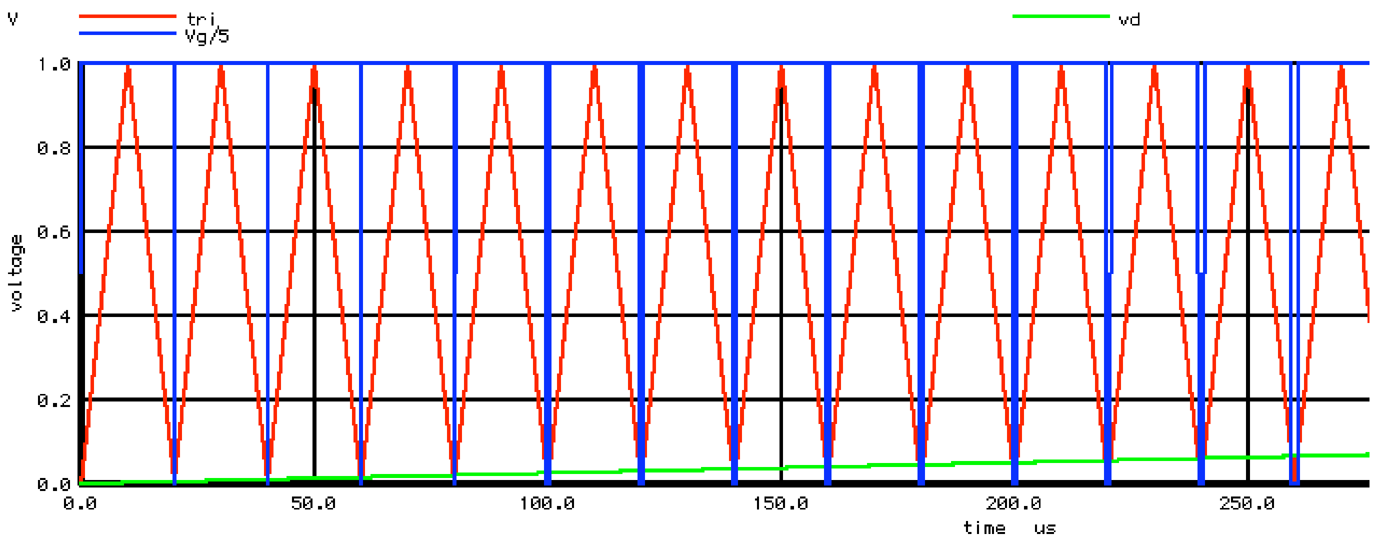
*=============**DUTY_CYCLE_RAMP_UP**===========

Where is the power lost in switching power supplies?
This example is using an inverter with some very large transistors, and some common values for L and C.

```
======================================================================
DUTY_CYCLE_RAMP_UP
*
*                  VCC _/\  /\  /\_ VP
*                     _|_  \/  \/   |
*                    /VCC\ RP      <-
*                    \___/        ||___ MP1
*                     _|_      ___||
*                     ///     |   ||_ VOUT_   _  _
*                             |         |  / \/ \/ \      ____      R1 = 5
* VDUTY     _|_________VG_____|        _|___| () ()  |___|OUT|__/\  /\  /\__
*          / _ \              |___||        L1           |___|    \/  \/   _|_
*   _|_   // \ \VG                ||___     100u           |     C1        ///
*  /VDT\  \   \//                 ||-> MN1                 |__||___ 3u
*  \___/   \___/          RN          |   Freq = 9 K          ||  _|_
*   _|_     _|_         _/\  /\  /\_|   Z=5.8Ohms                ///
*   ///     ///        _|_  \/  \/  VN
*                      ///
*
*
.OPTIONS  GMIN=1f       METHOD=trap   ABSTOL=1u     TEMP=27   srcsteps = 1  gminsteps = 1
.OPTIONS  RELTOL=.001   ABSTOL=1n     VNTOL=1u      ITL4=500  ITL1=400
*=========Create_Signal=================
VT        VT      0      DC      0       PWL(   0      0    1       1)
Vfreq     Vfreq   0      DC      50k
VD        VD      0      DC      0       PWL(   0      0    4m      1)
VPI       VPI     0      DC      3.141592653589793
B_TRI     TRI     0      V =     acos( cos(6.283185*V(VFreq)*V(VT)) )/v(VPI)
BVG       VG      0      V =     5*u( v(TRI) -v(VD))
VCC       VCC     0      DC      5
RPP       VCC     VP     1u
RN        VN      0      1u
MN1       VOUT    VG     VN      0       NMOSC    W=90000u    L=1u
MP1       VOUT    VG     VP      VCC     PMOSC    W=90000u    L=1u
L1        VOUT    OUT    100u
C1        OUT     0      3u
Rout      OUT     0      10K
BRout     OUT     0      I =     v(OUT)/v(Vrout)
Vrout     Vrout   0      5
*=========The_CMOS_Model_Files==================================
.model    NMOSC              NMOS(Level=  1   Cbs=2f Cbd=2f)
.model    PMOSC              PMOS(Level=  1   Cbs=2f Cbd=2f)
.control
*TRAN     TSTEP  TSTOP  TSTART TMAX   ?UIC?
tran      .1u    4m     0      .1u
set       pensize = 2
plot      tri vd Vg/5 xlimit 0 .4m
======================================================================
```

It is not real hard to create a triangle wave TRI and input it to one input of a voltage comparator VG. Apply a ramp up voltage VD at the other end of the comparator, and it is easy to ramp from 0% to 100% duty cycle over a 4msec transient analysis.

==

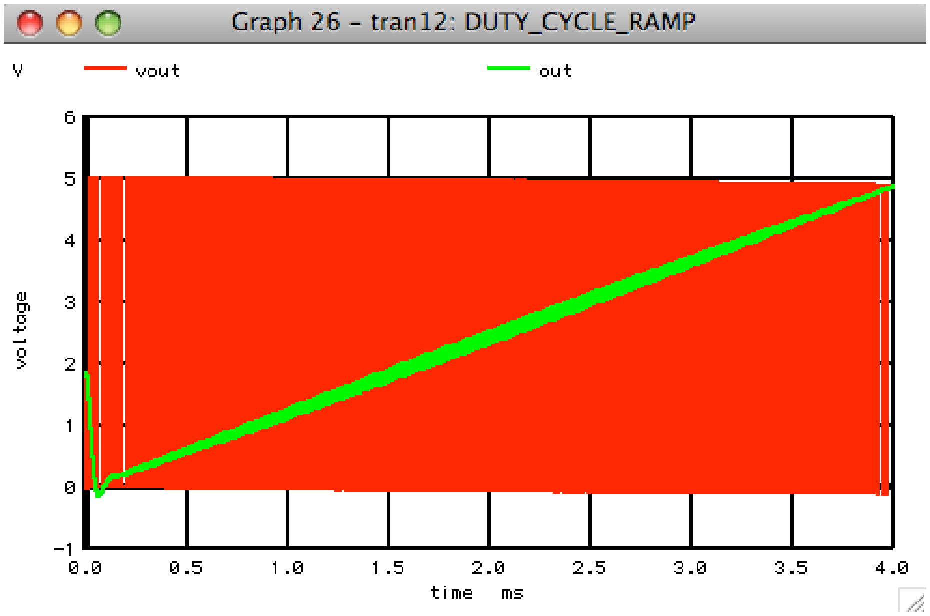


==

Putting in a square wave into a simple RLC network should just lowpass filter it. So the ramp up in duty cycle at the VOUT node should produce a linear ramp up at the OUT node.

==

```
*
*                  VCC _/\   /\   /\_ VP
*                     _|_   \/   \/   |
*                    /VCC\ RP       <-
*                    \___/        ||___ MP1
*                     _|_     ____||
*                     ///    |    ||_ VOUT_  _  _
*                            |       |   / \/ \/ \
*  VDUTY      _|________________VG    |    _|____| ()  () |__|OUT|__/\  /\  /\__    R1 = 5
*            /   \               |___||         L1           |___|   \/  \/    _|_
*    _|_   //  \   \VG               ||__      100u           |         C1      ///
*   /VDT\  \    \//                  ||-> MN1                 |__||__ 3u
*   \___/   \___/          RN          |      Freq = 9 K          || _|_
*    _|_     _|_          _/\  /\  /\_|      Z=5.8Ohms               ///
*    ///     ///        _|_  \/  \/   VN
*                       ///
*
plot      vout out
```



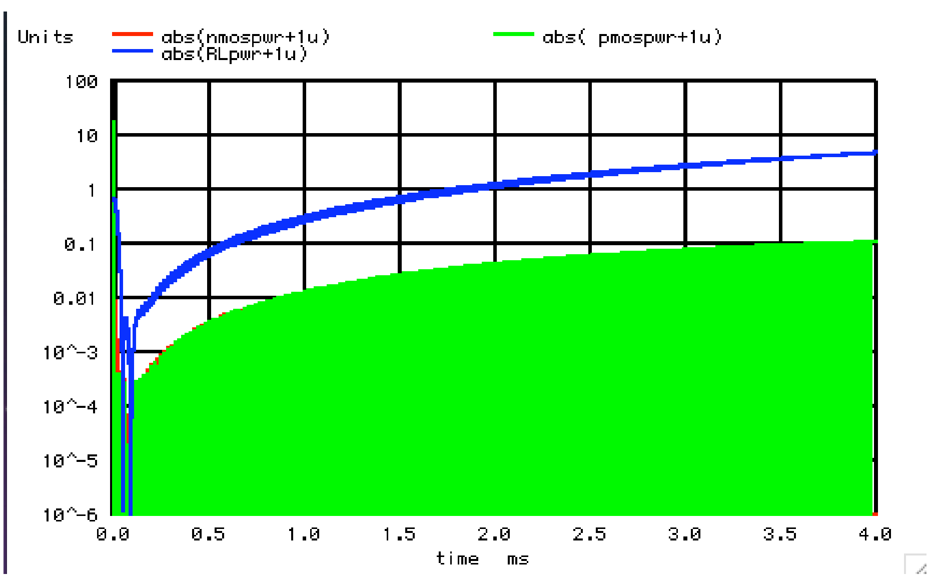
===

But the ramp up also allows power efficiency to be monitored over the full range of the duty cycle. The power of each transistor is found measuring source current and multiplying it by the voltage across the drain source of each transistor.

Plotting on a semi-log scale can better show the full duty cycle which is going from 0% to 100% over 4msec.

===

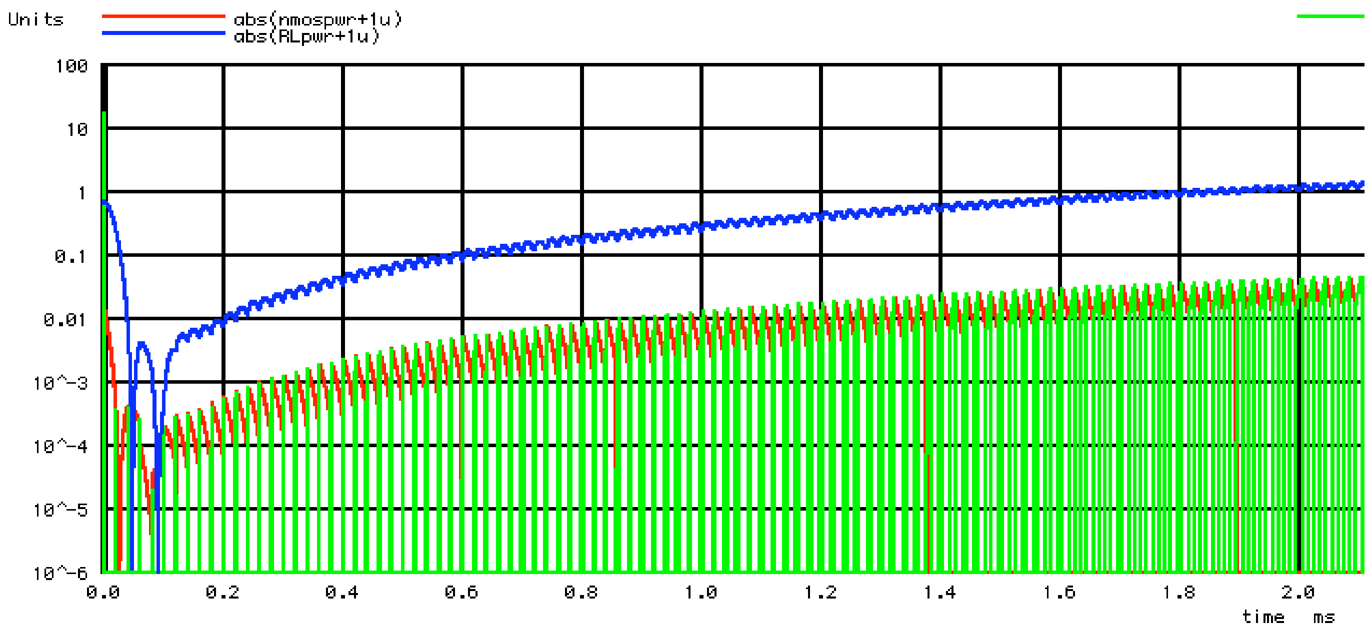
```
let      nmospwr  = vn*(vout-vn)*1000k
let      pmospwr  = (vcc-vp)*(vcc-vout)*1000k
let      RLpwr    =  out*out/Vrout[0]
plot     abs(nmospwr+1u) abs( pmospwr+1u) abs(RLpwr+1u) ylog
```



===

A closer look reveals that the power is being multiplexed between the
NMOS and PMOS transistors according to duty cycle.

==

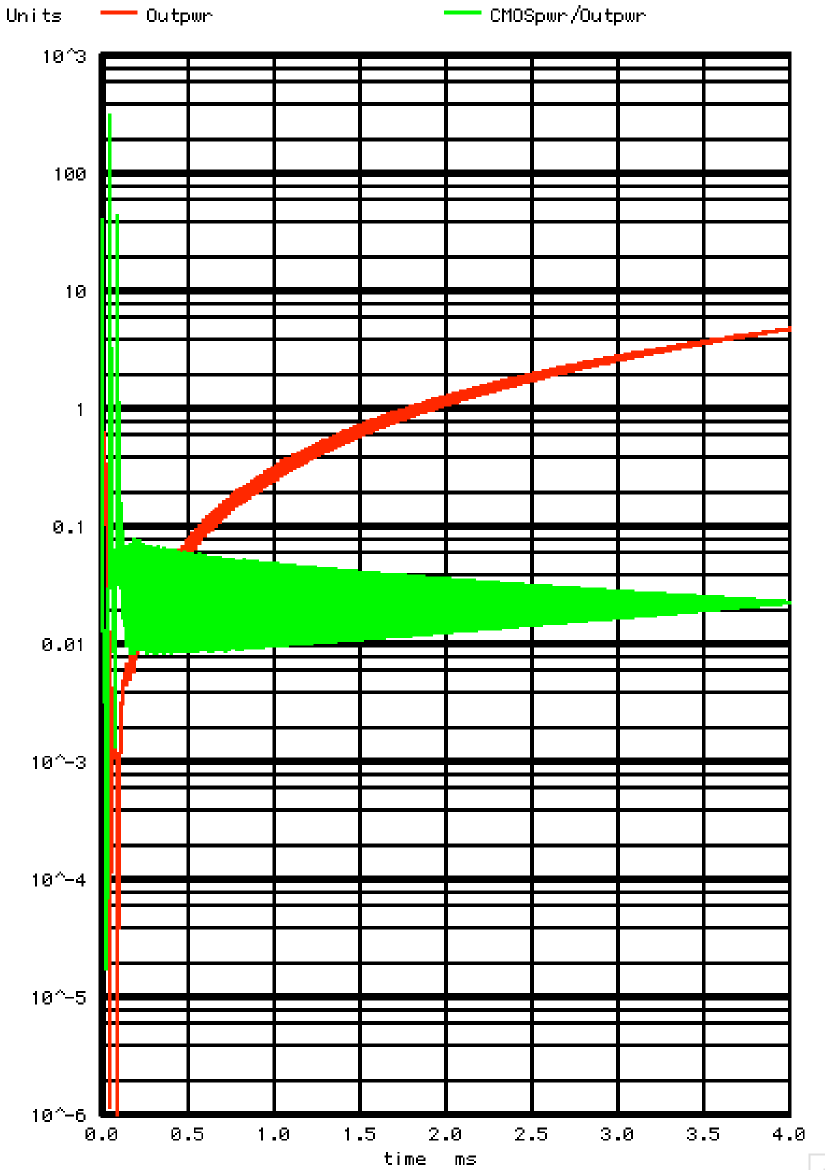


==

A more revealing plots shows the power loss as a fraction of output power. It looks like the transistors are losing around 2% of the power over the full duty cycle.

==

```
let      Outpwr  = abs(RLpwr+1u)
let      CMOSpwr = abs(nmospwr+1u) +abs( pmospwr+1u)
plot     Outpwr    CMOSpwr/Outpwr ylog
```



===

At 100% duty cycle, there are several ways to calculate the resistance of the PMOS device.

(5V-Voutmax)/5V = rout_PMOS/RL

===

```
print       Vrout[0]
let         rout_eq = Vrout[0]*(5-maximum(out))/5
print       rout_eq

let         numb = length(vout)-1
let         Pres = Vrout[0]*(vcc[0]-vout[$&numb))/vout[$&numb)
print       Pres
```

===

```
vrout[0]   =   5.00000e+00
rout_eq    =   1.35676e-01
pres       =   1.12386e-01
```

===

```
*
*                  VCC _/\  /\  /\_ VP
*                    _|_  \/  \/  _|
*                   /VCC\ RP      <-
*                   \___/     ||___ MP1
*                    _|_      ||
*                    ///   ___||_ VOUT_  _  _
*           ________________|  ||  | / \/ \/ \    ____     R1 = 5
* VDUTY     _|_         VG   |    _|___| ()  () |__|OUT|__/\  /\  /\__
*          / \               |___||           L1      |____|   \/  \/   _|_
*  _|_   //‾\  \VG             ||‾‾            100u     |    C1       ///
* /VDT\  \    \//              ||-> MN1                  |__||__ 3u
* \___/   \___/       RN         |     Freq = 9 K          ||  _|_
*  _|_     _|_      _/\  /\  /\_|     Z=5.8Ohms               ///
*  ///     ///     _|_  \/  \/  VN
*                  ///
*
==========================================================================
```

All resistance except RL have been made small. The output transistors are being modeled as being very large.
It appears that the PMOS device is acting like a switch with about 100mOhm resistance. Since the output load is 5 Ohms, that should produce a constant power loss of 2%.

.1Ohm/5Ohm = 0.02 = 2%

```
===========Full_Netlist_For_Copy_Paste========================
DUTY_CYCLE_RAMPUP
*
*                  VCC _/\  /\  /\_ VP
*                    _|_  \/  \/  _|
*                   /VCC\ RP      <-
*                   \___/     ||___ MP1
*                    _|_      ||
*                    ///   ___||_ VOUT_  _  _
*           ________________|  ||  | / \/ \/ \    ____     R1 = 5
* VDUTY     _|_         VG   |    _|___| ()  () |__|OUT|__/\  /\  /\__
*          / \               |___||           L1      |____|   \/  \/   _|_
*  _|_   //‾\  \VG             ||‾‾            100u     |    C1       ///
* /VDT\  \    \//              ||-> MN1                  |__||__ 3u
* \___/   \___/       RN         |     Freq = 9 K          ||  _|_
*  _|_     _|_      _/\  /\  /\_|     Z=5.8Ohms               ///
*  ///     ///     _|_  \/  \/  VN
*                  ///
*
*
.OPTIONS  GMIN=1f       METHOD=trap   ABSTOL=1u     TEMP=27   srcsteps = 1  gminsteps = 1
.OPTIONS  RELTOL=.001   ABSTOL=1n     VNTOL=1u      ITL4=500  ITL1=400
*=========Create_Signal=================
VT        VT     0      DC     0      PWL(   0      0    1      1)
Vfreq     Vfreq  0      DC     50k
VD        VD     0      DC     0      PWL(   0      0    4m      1)
VPI       VPI    0      DC     3.141592653589793
B_TRI     TRI    0      V =    acos( cos(6.283185*V(VFreq)*V(VT)) )/v(VPI)
BVG       VG     0      V =    5*u( v(TRI) -v(VD))
VCC       VCC    0      DC     5
RPP       VCC    VP     1u
RN        VN     0      1u
MN1       VOUT   VG     VN     0      NMOSC   W=90000u    L=1u
MP1       VOUT   VG     VP     VCC    PMOSC   W=90000u    L=1u
L1        VOUT   OUT    100u
C1        OUT    0      3u
Rout      OUT    0      10K
BRout     OUT    0      I =    v(OUT)/v(Vrout)
Vrout     Vrout  0      5
```

```
*=========The_CMOS_Model_Files=================================
.model    NMOSC             NMOS(Level=  1  Cbs=2f Cbd=2f)
.model    PMOSC             PMOS(Level=  1  Cbs=2f Cbd=2f)

.control
*TRAN     TSTEP  TSTOP  TSTART TMAX   ?UIC?
tran      .1u    4m     0      .1u
set       pensize = 2
plot      tri vd Vg/5 xlimit 0 .4m
plot      vout out

let       nmospwr = vn*(vout-vn)*1000k
let       pmospwr = (vcc-vp)*(vcc-vout)*1000k
let       RLpwr =   out*out/Vrout[0]
plot      abs(nmospwr+1u) abs( pmospwr+1u) abs(RLpwr+1u) ylog

let       Outpwr = abs(RLpwr+1u)
let       CMOSpwr =abs(nmospwr+1u) +abs( pmospwr+1u)
plot      Outpwr  CMOSpwr/Outpwr ylog

print     Vrout[0]
let       rout_eq = Vrout[0]*(5-maximum(out))/5
print     rout_eq

let       numb = length(vout)-1

let       Pres = Vrout[0]*(vcc[0]-vout[$&numb))/vout[$&numb)
print     Pres

.endc

.end
```


9.16.10_1.04PM
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