

ASYNC'06

A Level-Crossing Flash Asynchronous Analog-to-Digital Converter

Filipp Akopyan, Rajit Manohar and Alyssa Apsel

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Grenoble, France

Motivation

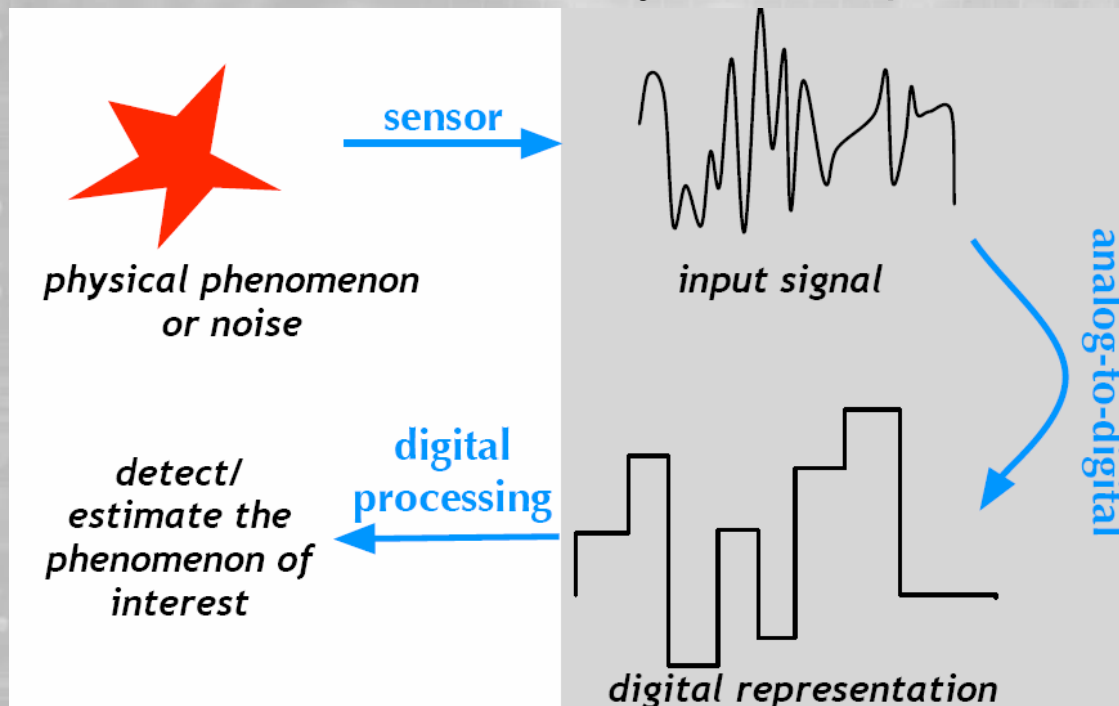
Ultra Low Power ADC will be beneficial in several areas:

- *Signal processing field*
 - data processing in sensor networks
 - increasing lifetime of cell phones
 - temperature, pressure, vibration sensors, etc.

- *Biomedical engineering field*
 - low-power implants to monitor human organs
 - process data that reflects changes in the body
 - signal if the body is not functioning properly

Design Goals

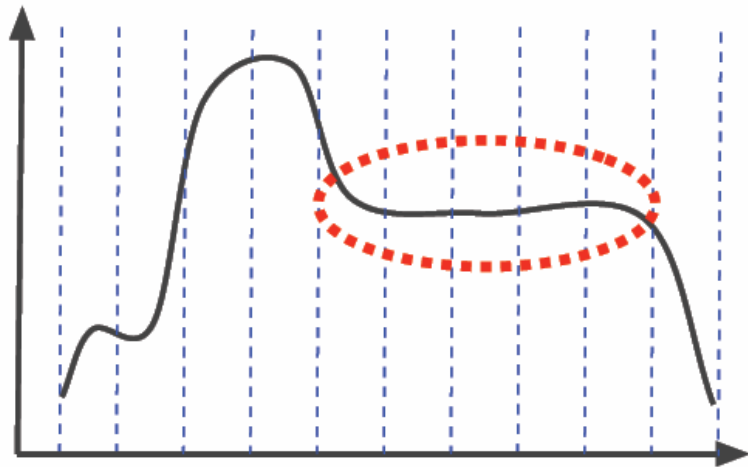
- ❑ Exploit Signal Properties
 - Wide range of input frequencies
 - Real-world signal are often idle
- ❑ Asynchronous Design
 - Circuits adapt to input signal bandwidth (data-driven)
 - System shuts down automatically when input is stable



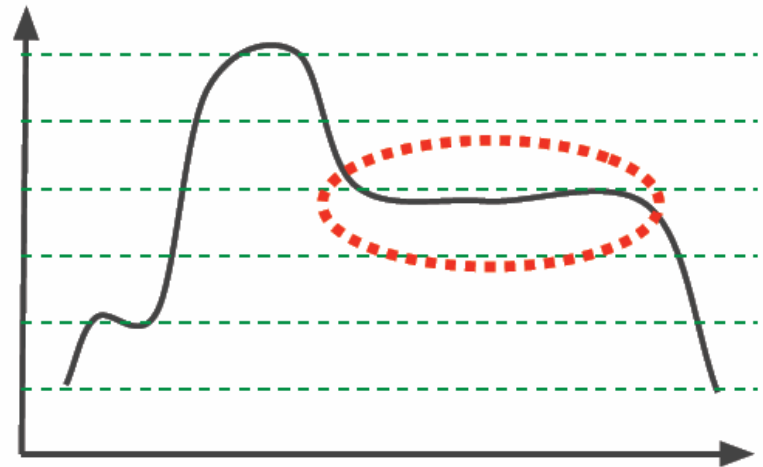
Asynchronous ADC for Low-Power Applications

- ❖ Design of the ADC
- ❖ Analysis
- ❖ Evaluation
- ❖ Conclusion

Level Crossing Scheme



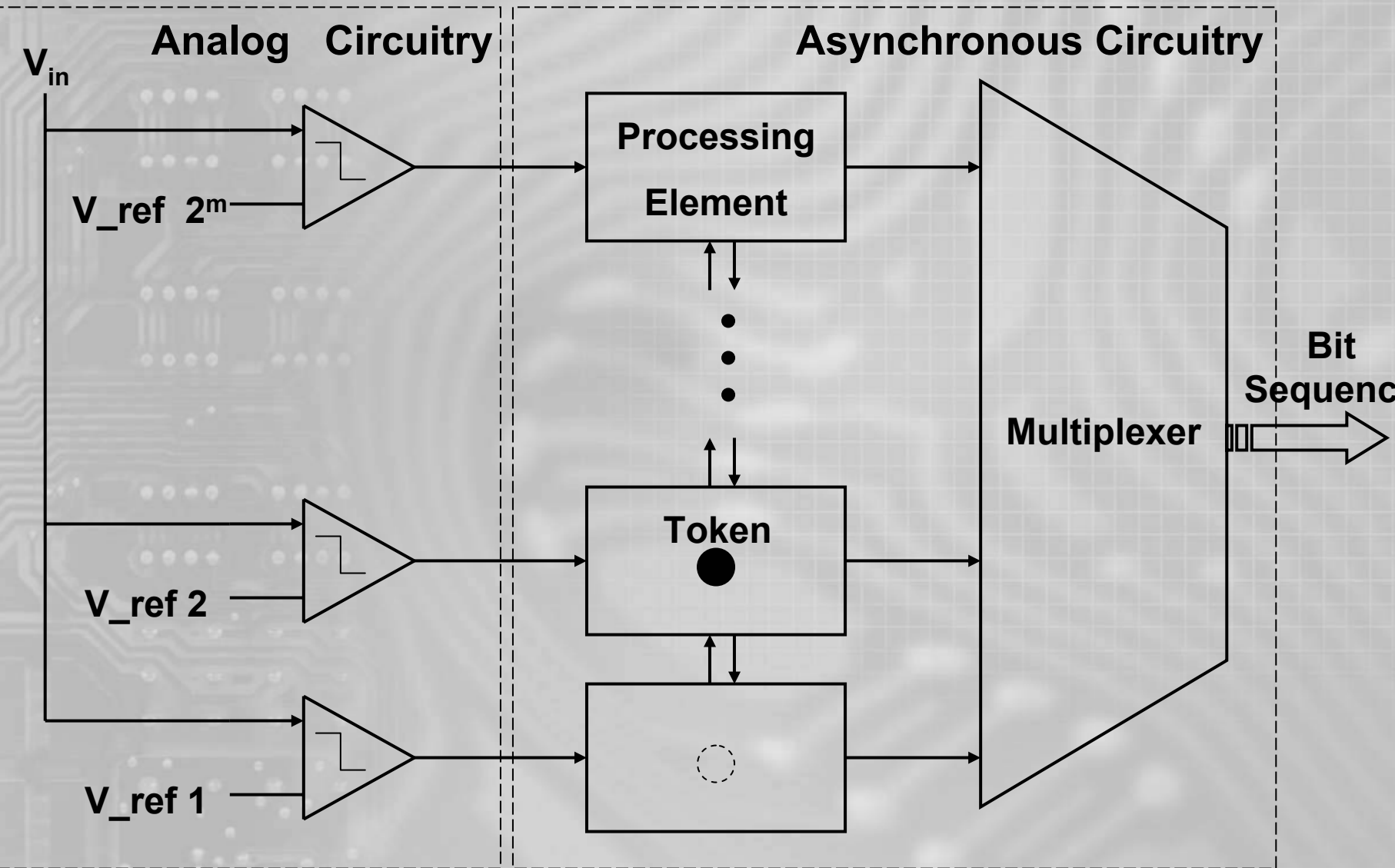
Conventional uniform Nyquist sampling



Non-uniform level-crossing sampling

- Low power consumption: no activity when signal is not changing
- Bandwidth adaptive: number of samples depends on signal BW

Proposed ADC Structure

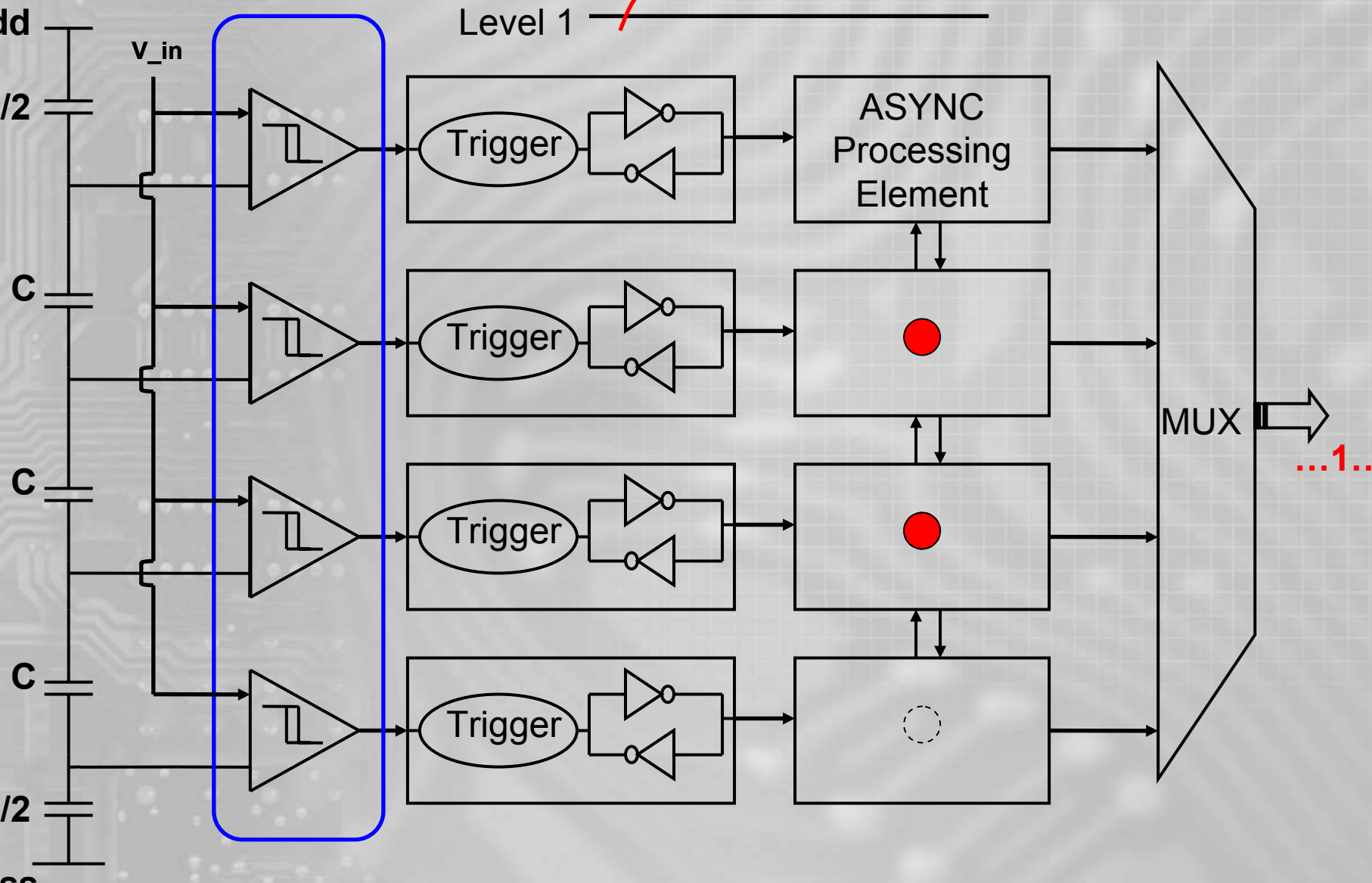


Design Overview

- Analog circuitry - comparators with hysteresis (for noise immunity)
- CHP (Communicating Hardware Processes) for all asynchronous circuits
- Quasi-Delay Insensitive design style with 4-phase communication protocols
- Data in the ASYNC-ADC is outputted by one channel
- Time is not tracked explicitly

Level 4
Level 3
Level 2
Level 1

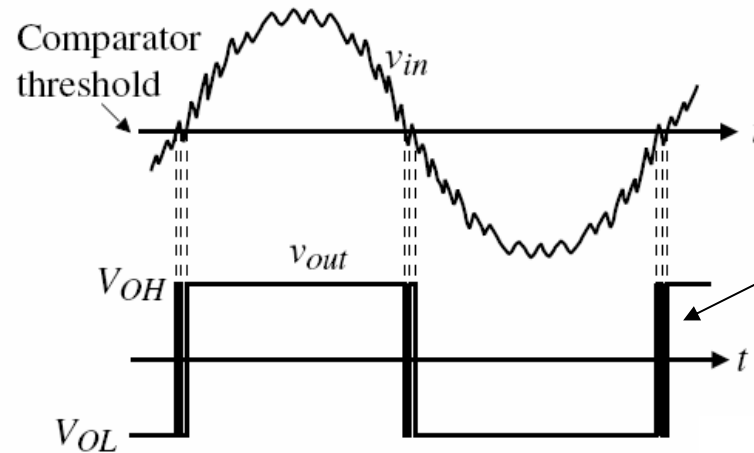
Operation



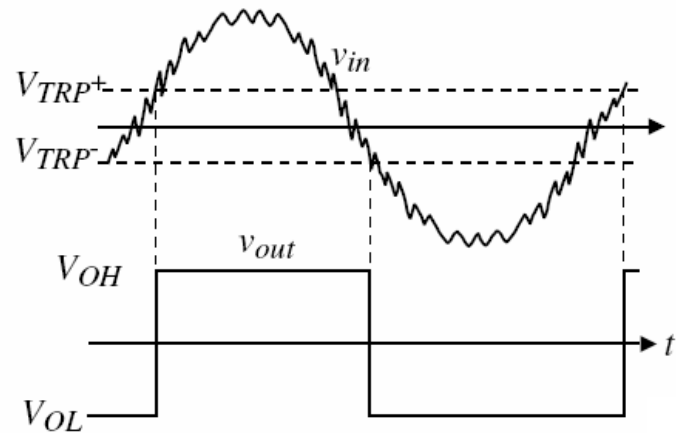
Analog Considerations

Influence of Input Noise on the Comparator

Comparator without hysteresis:

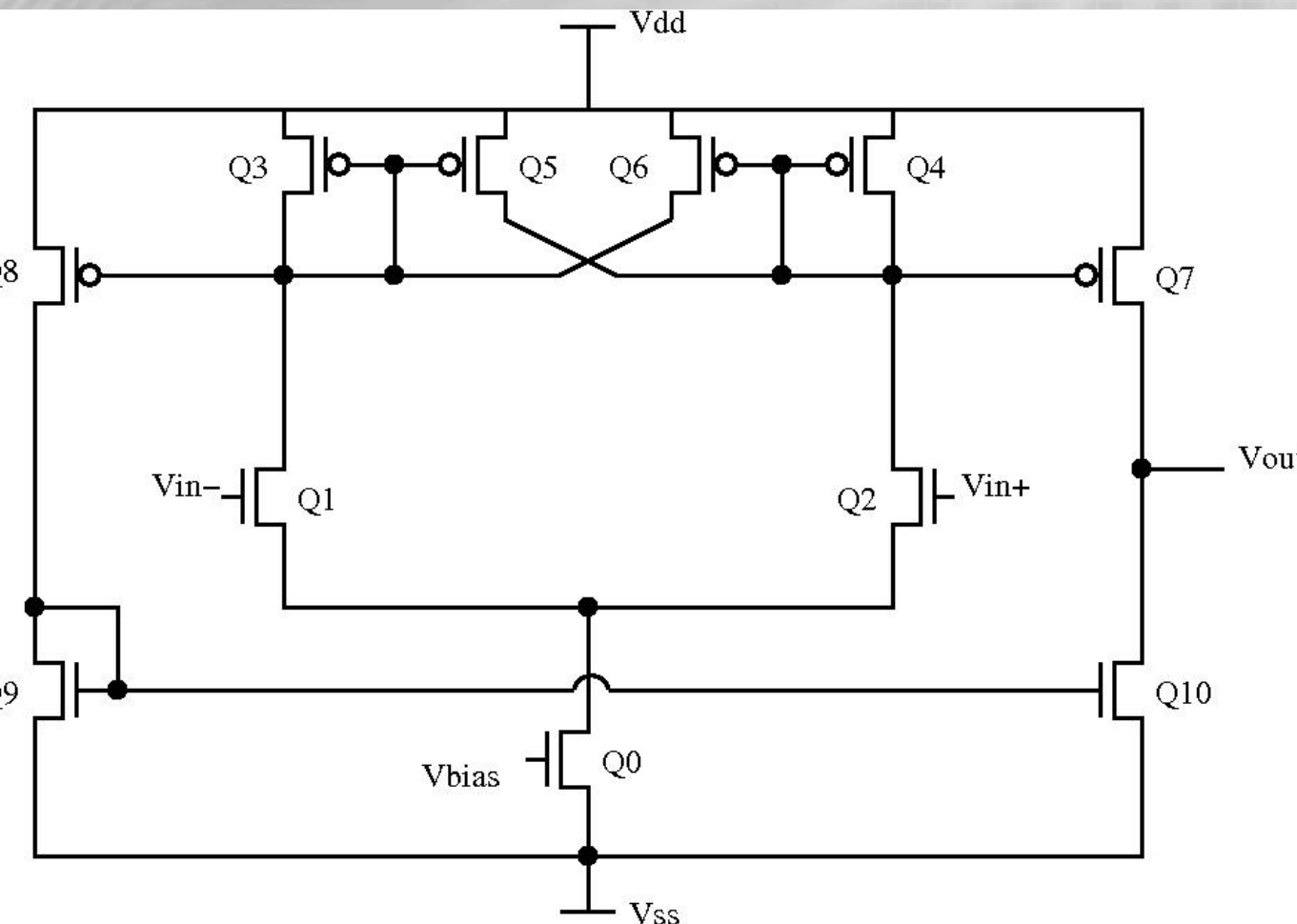


Comparator with hysteresis:



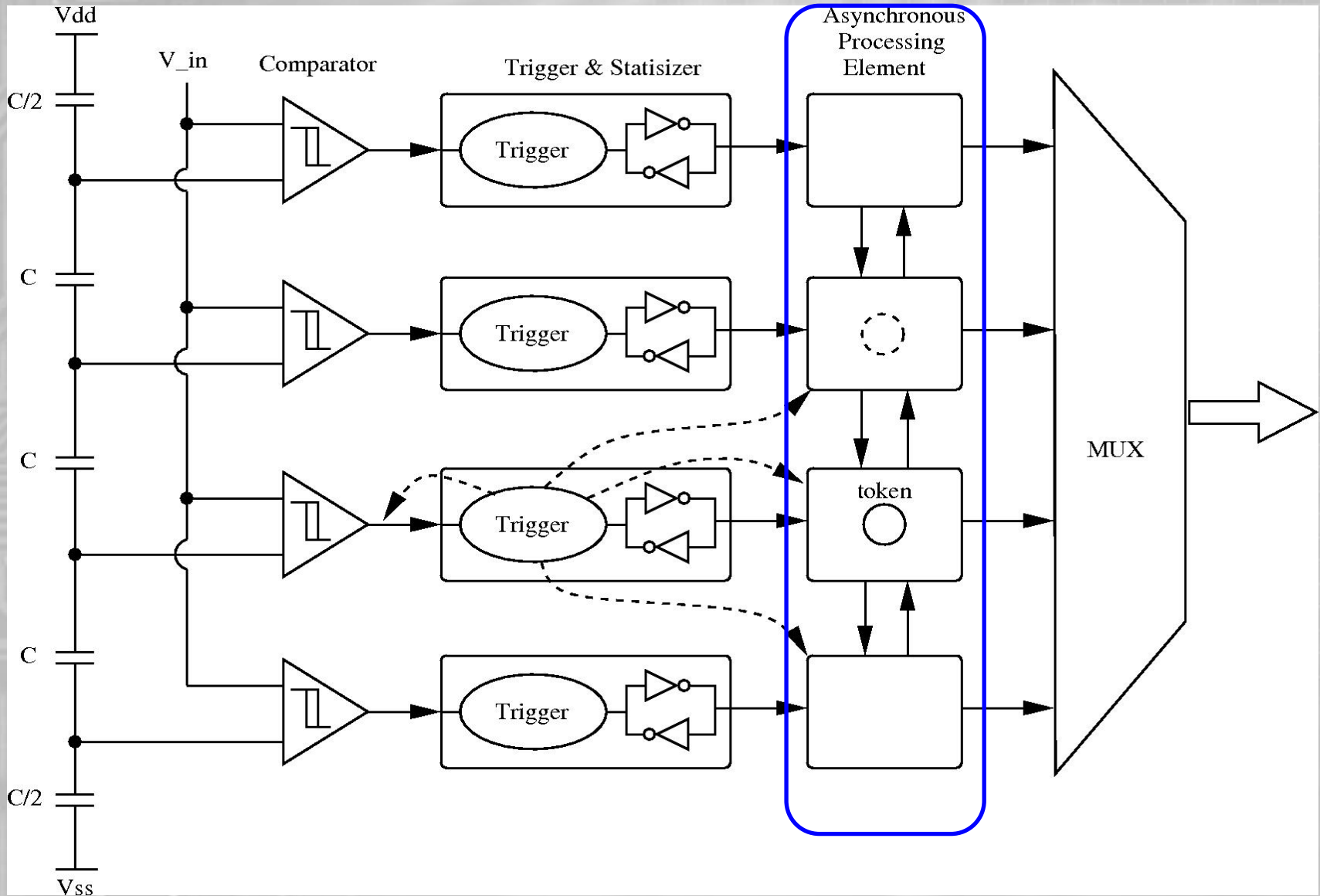
Implemented Analog Design

Differential Regenerative Comparator with hysteresis

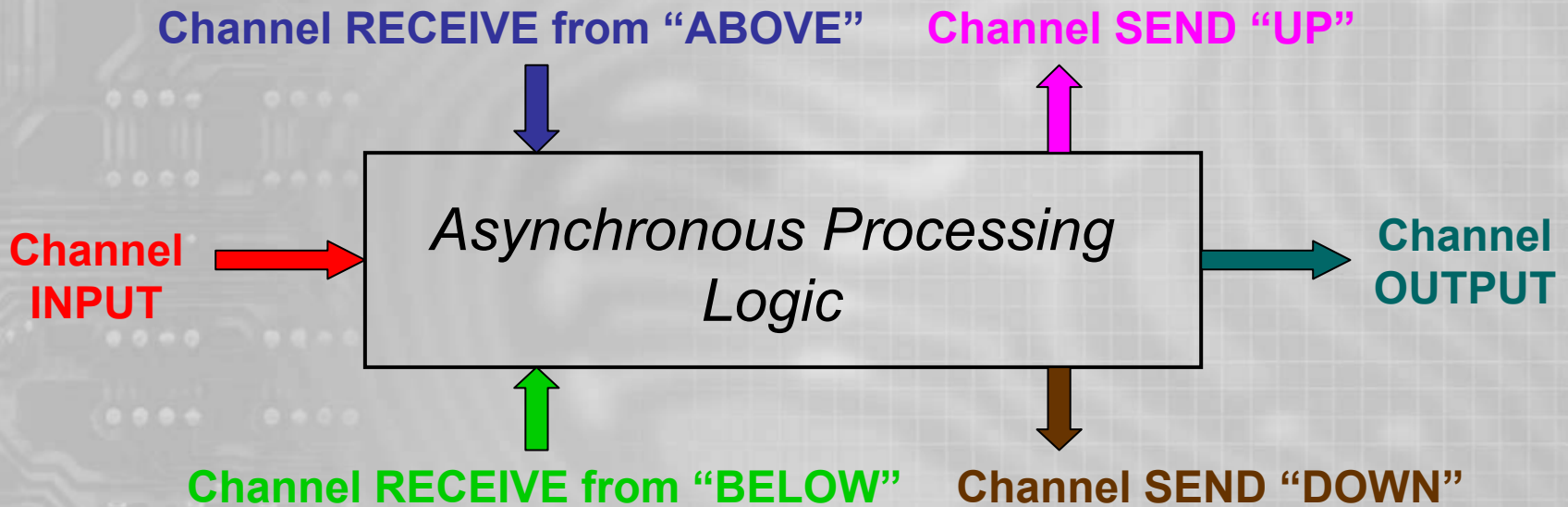
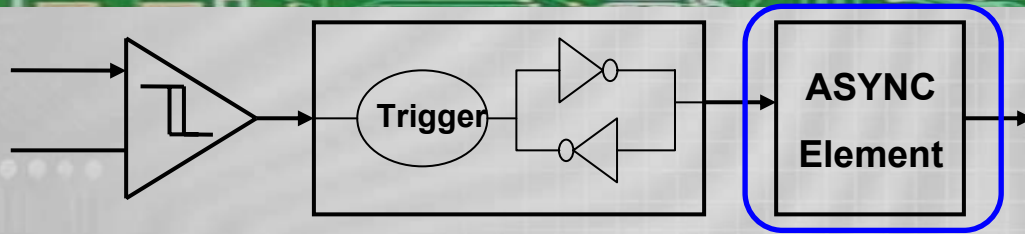


- Positive Feedback
- Tunable Bandwidth
- Variable trip voltage
- High differential gain
- Nonlinearities
- Transistor matching

Processing Element



Processing Element

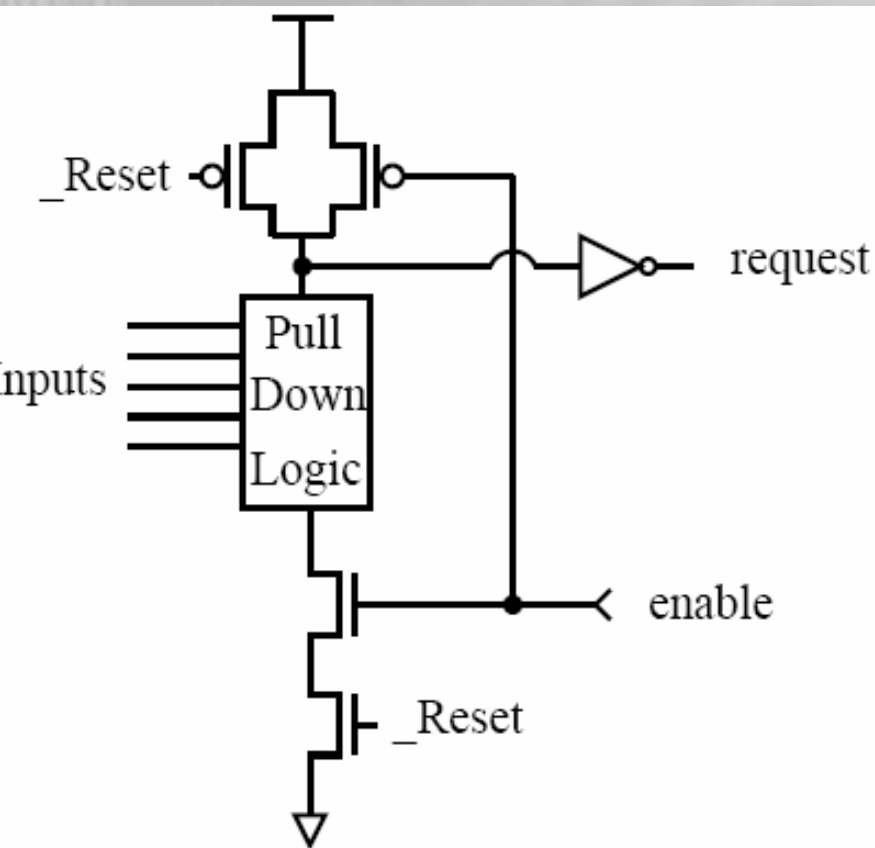
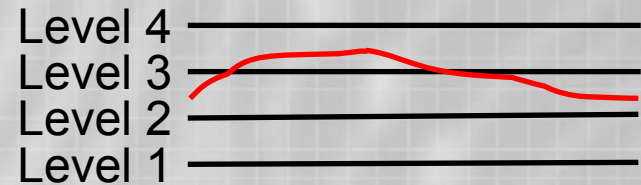
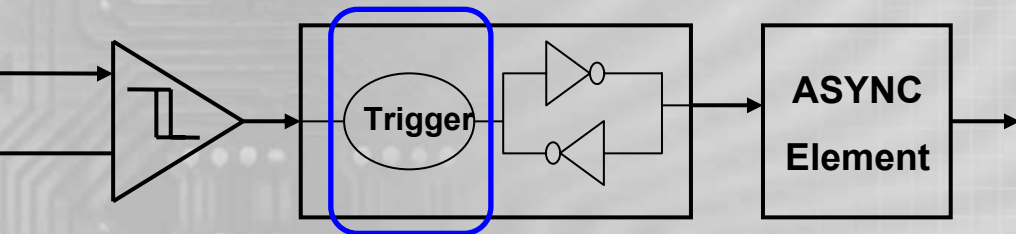


input → *TOKEN_CHECK*; **output** (1) or (0); indicate if signal is above or below

request from above → **pass token "above"**; {don't have token}; indicate that token is above

request from below → **pass token "down"**; {don't have token}; indicate that token is below

Digital Design



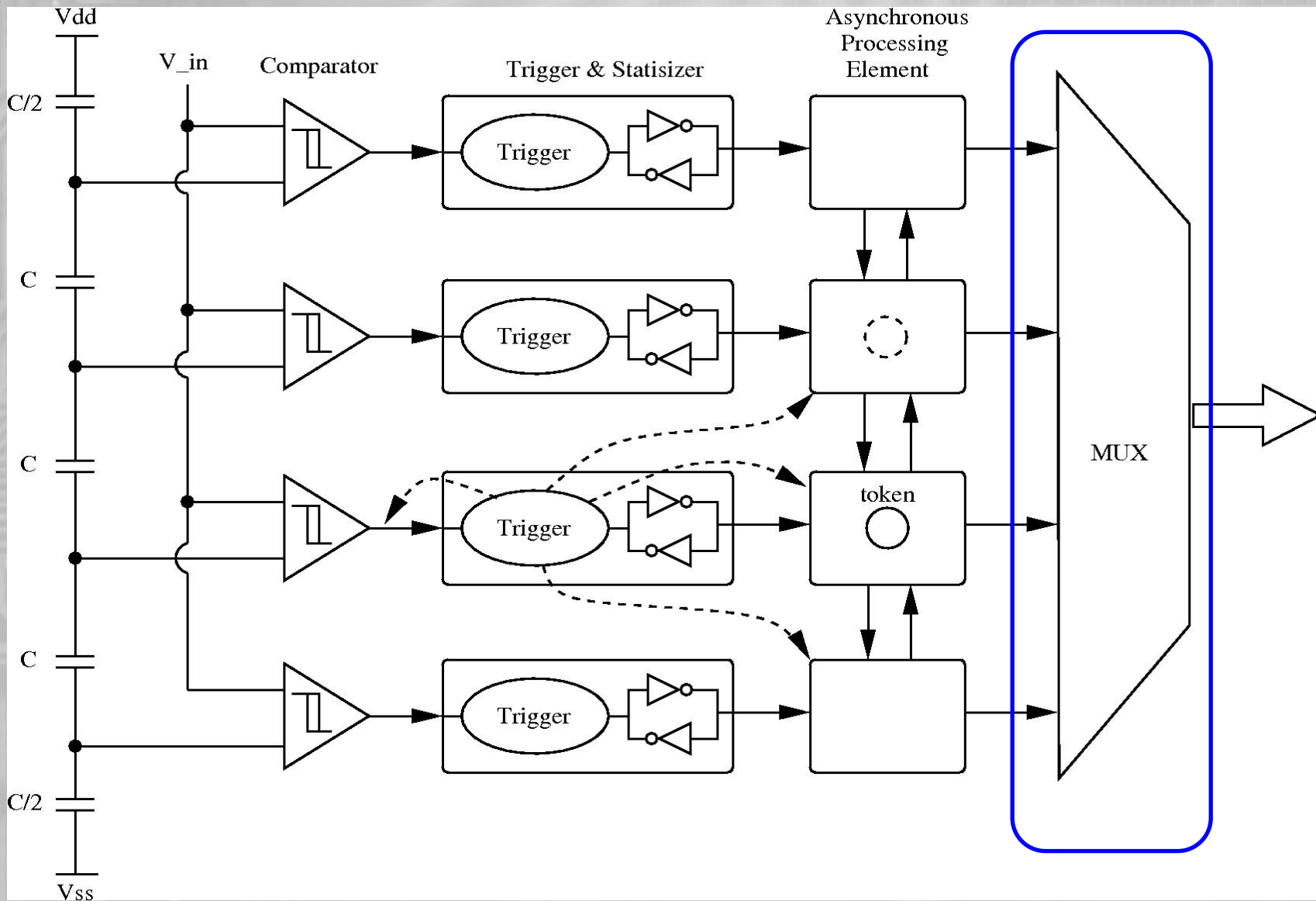
Trigger becomes active if one of the crossing conditions holds:

1. Upward Crossing

- the comparator output is high
- + the current level indicates that the signal was below before
- + the previous level indicates that the signal is above
- + the previous element has completed processing its request and sending its output

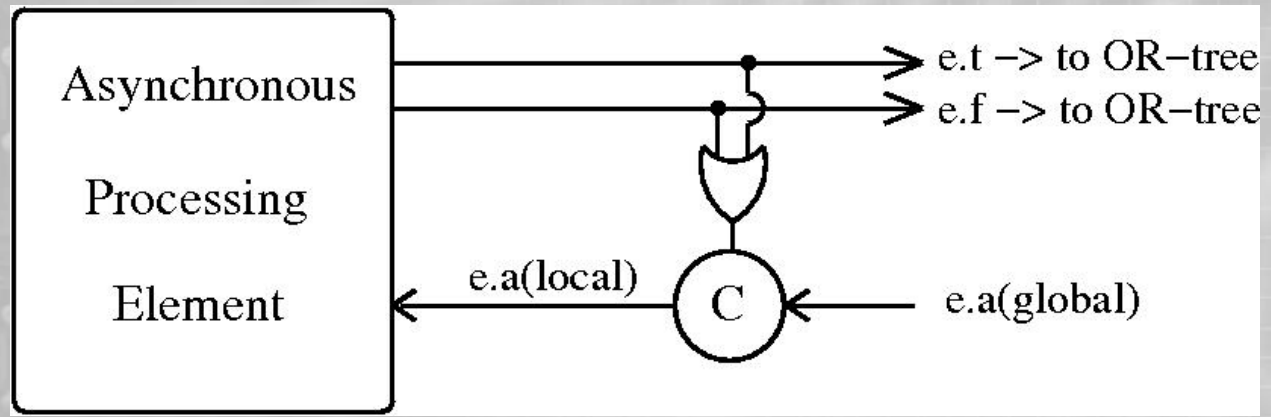
2. Downward Crossing

Multiplexer

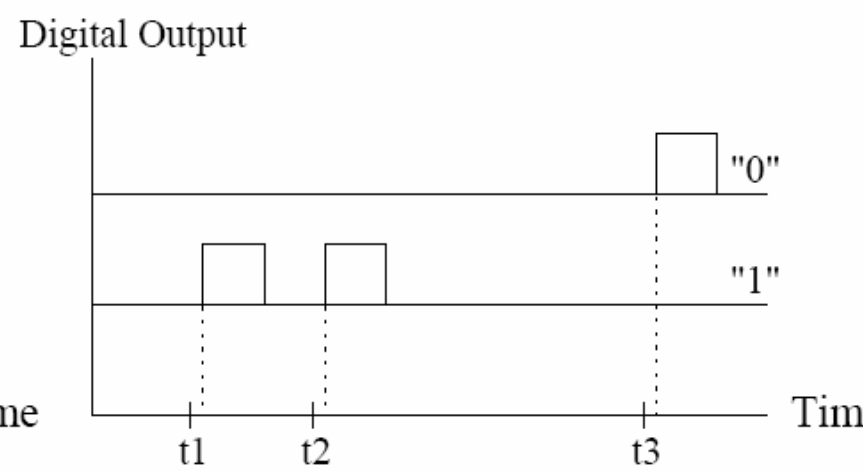
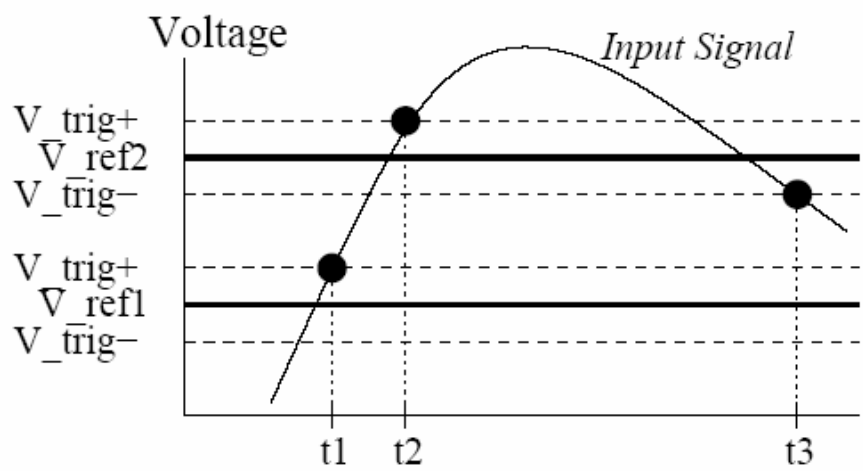


Multiplexer Design

Deterministic Merge



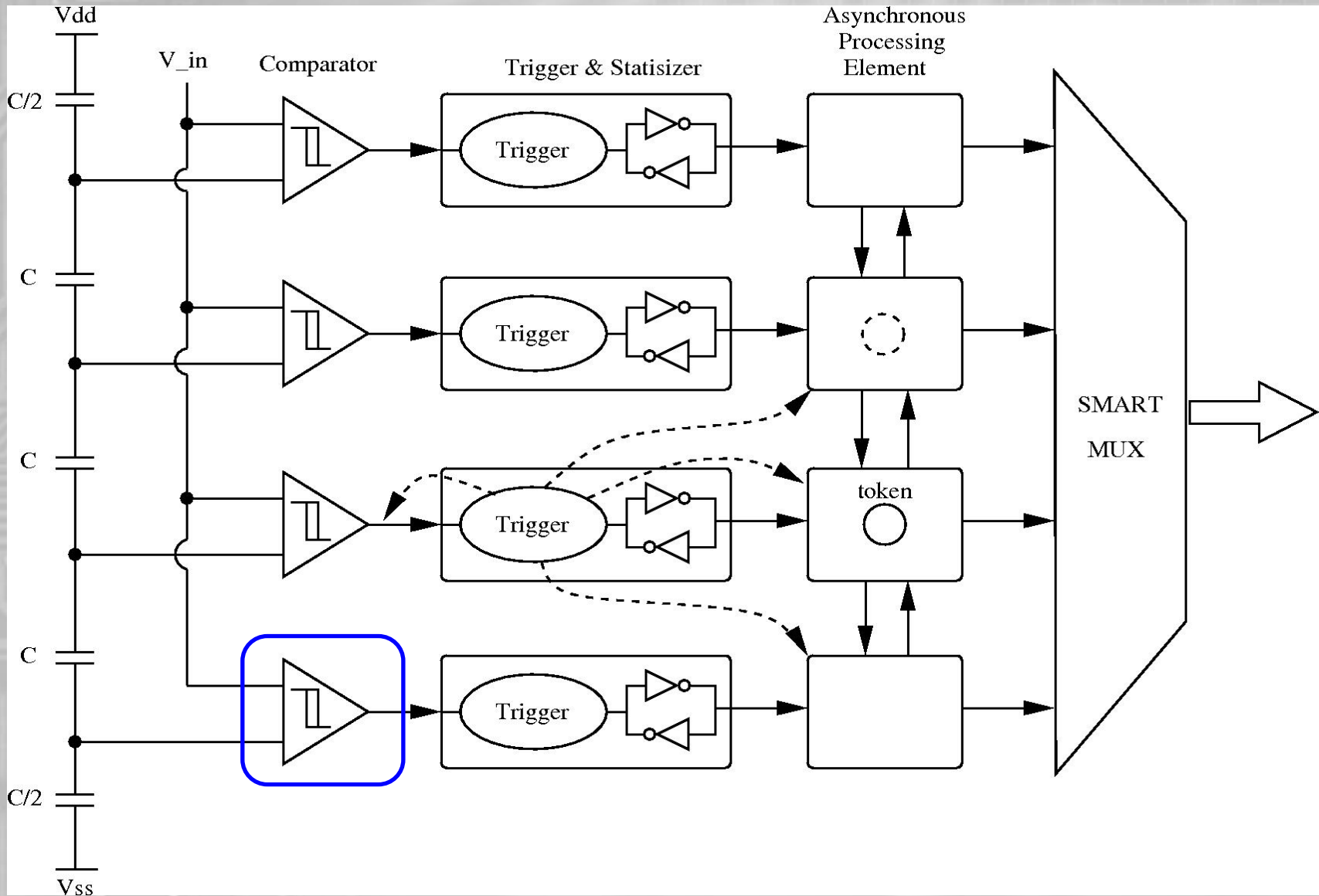
Sample Output



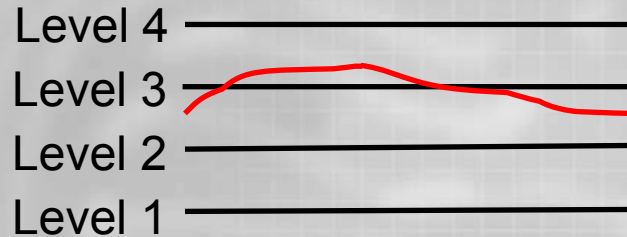
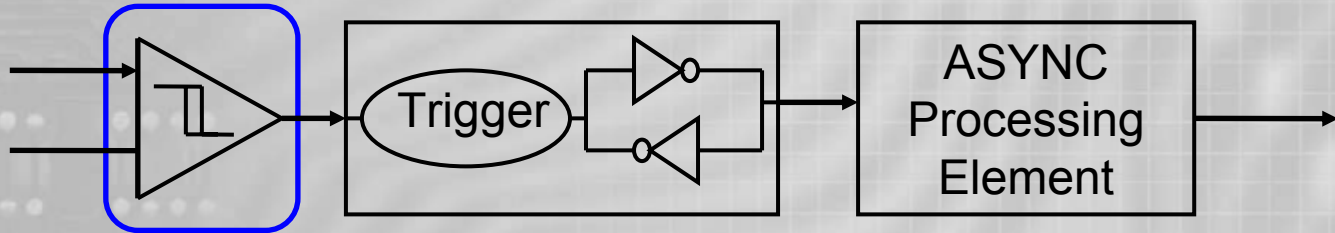
Asynchronous ADC for Low-Power Applications

- ❖ Design of the ADC
- ❖ **Analysis**
- ❖ Evaluation
- ❖ Conclusion

Power Analysis



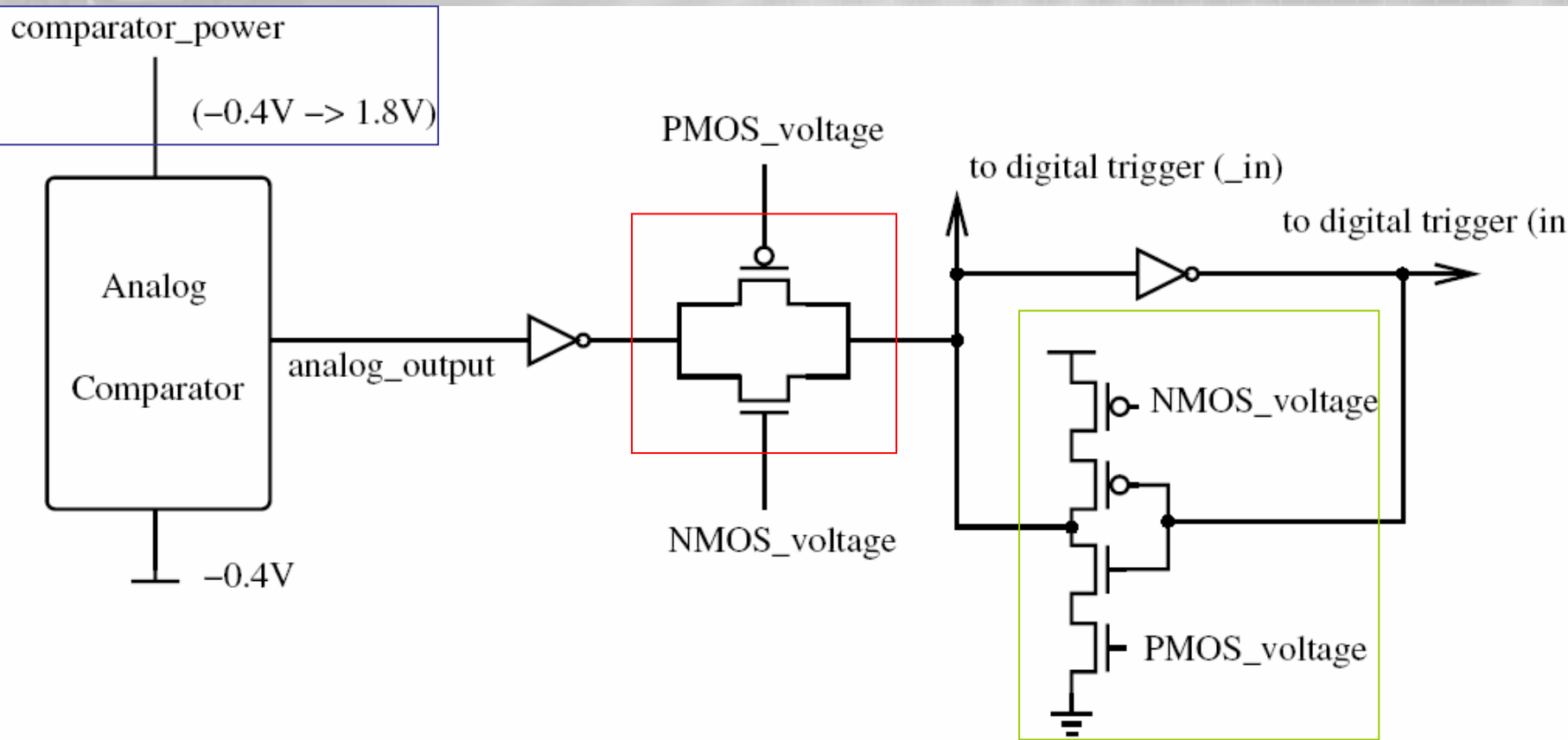
Power Analysis



Comparator power is **turned on** if one of the following holds:

- The signal is above i processing element and below $i+1$ processing element
- The signal is above $i-1$ processing element and below i processing element
- The request is being processed by the current (i) element

Power Analysis



Components added:

- *Transmission Gate*
- *Gated Staticizer*

Variable "Comparator_power" voltage source

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Simulation Setup

- 4-bit converter (16 levels)
- Input: sinusoids of various frequencies
- Transistor models for TSMC 0.18 micron process
- Minimal transistor sizing
- The capacitive divider was simulated as a resistive divider ($R = 1 \text{ MOhm}$)
- V_b on the comparators set to 0.25V
- No explicit time tracking

Simulation Data

LCF-ADC Simulation Data

Signal BW	Power (μW)	Energy/sample (nJ)
1 kHz	34.41	34.4
100 kHz	42.48	0.42
114 kHz	43.57	0.38
160 kHz	46.84	0.29
1 MHz	114.14	0.11
5 MHz	437.81	0.087

❖ Much lower power consumption than previous designs

Input Signal Consideration

Maximum number of crossings that can be correctly interpreted:

$$BW \cdot \frac{\text{number of crossings}}{\text{cycle}} \leq f_{\max}$$

f_{\max} - maximum throughput of the asynchronous circuitry

BW - input signal bandwidth (in MHz)

Periodic input with $2n$ crossings in one period: $BW \cdot 2n \leq f_{\max}$

f_{\max} for minimal power consumption is 220MHz
Maximum number of levels:

$$n \leq \frac{110}{BW}$$

1 kHz	110000 levels	($\sim 2^{16}$)
100 kHz	1100 levels	($\sim 2^{10}$)
1 MHz	110 levels	($\sim 2^6$)
5 MHz	22 levels	($\sim 2^4$)

Asynchronous ADC for Low-Power Applications

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Conclusion

- Applications: sensor networks, biomedical implants
- Level-Crossing Flash ADC approach
- Very low-power consumption
- Low-complexity design and ease of increasing precision
- Differential output on one dual rail channel

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QUESTIONS

FURTHER READING

Click any one of the following links to be taken to a website which contains the following documents.

The following are some recent examples of Asynchronous ADC activity off the web.

[6 bit Asynchronous December 2006](#)
[Asynchronous ADC In CAD Mentor Graphics](#)
[Asynchronous Data Processing System](#)
[ASYNCHRONOUS PARALLEL RESISTORLESS ADC](#)
[Flash Asynchronous Analog-to-Digital Converter](#)
[Novel Asynchronous ADC Architecture](#)
[LEVEL BASED SAMPLING FOR ENERGY CONSERVATION IN LARGE NETWORKS](#)
[A Level-Crossing Flash Asynchronous Analog-to-Digital Converter](#)
[Weight functions for signal reconstruction based on level crossings](#)
[Adaptive Rate Filtering Technique Based on the Level Crossing Sampling](#)
[Adaptive Level-Crossing Sampling Based DSP Systems](#)
[A 0.8 V Asynchronous ADC for Energy Constrained Sensing Applications](#)
[Spline-based signal reconstruction algorithm from multiple level crossing samples](#)
[A New Class of Asynchronous Analog-to-Digital Converters](#)
[Effects of time quantization and noise in level crossing sampling stabilization](#)

Here is some more background information on Analog to Digital converters.

[A 1-GS/s 6-bit 6.7-mW ADC](#)
[A Study of Folding and Interpolating ADC](#)
[Folding ADCs Tutorials](#)
[high speed ADC design](#)
[Investigation of a Parallel Resistorless ADC](#)

Here are some patents on the subject.

[4,291,299 Analog to digital converter using timed](#)
[4,352,999 Zero crossing comparators with threshold](#)
[4,544,914 Asynchronously controllable successive approximation](#)
[4,558,348 Digital video signal processing system using](#)
[5,001,364 Threshold crossing detector](#)
[5,315,284 Asynchronous digital threshold detector](#)
[5,945,934 Tracking analog to digital converter](#)
[6,020,840 Method and apparatus for representing waveform](#)
[6,492,929 Analogue to digital converter and method](#)
[6,501,412 Analog to digital converter including a quantizers](#)
[6,667,707 Analog to digital converter with asynchronous ability](#)
[6,720,901 Interpolation circuit having a conversio2](#)
[6,850,180 SelfTimed ADC](#)
[6,965,338 Cascade A D converter](#)
[7,133,791 Two mean level crossing time interval](#)

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dsauersanjose@aol.com
Don Sauer