

# 8-Bit 400 Ms/s Folding ADC

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# Overview

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- Folding Architecture
- Implementation
  - Top Level Diagram
  - Folder
  - Interpolation
  - Comparator
  - Course ADC
  - Synchronization
- Performance
- Conclusion



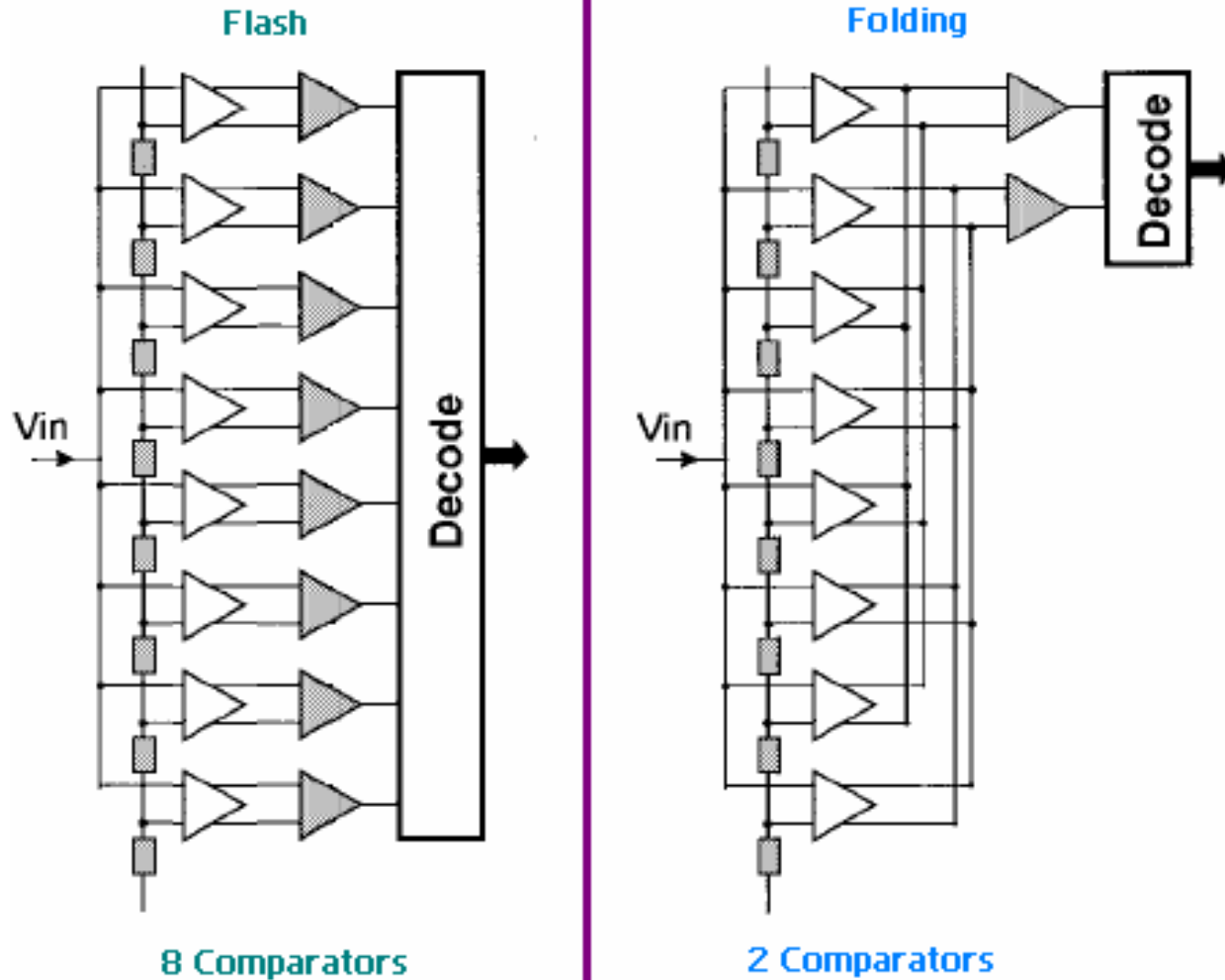
# Folding Architecture

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- Moderate Resolution 6-12 Bits
- High Speed
- Fewer Comparators than Flash
  - Less Area
  - Lower Power Consumption
- Applications: Communications, LANs, Flat Panel Displays

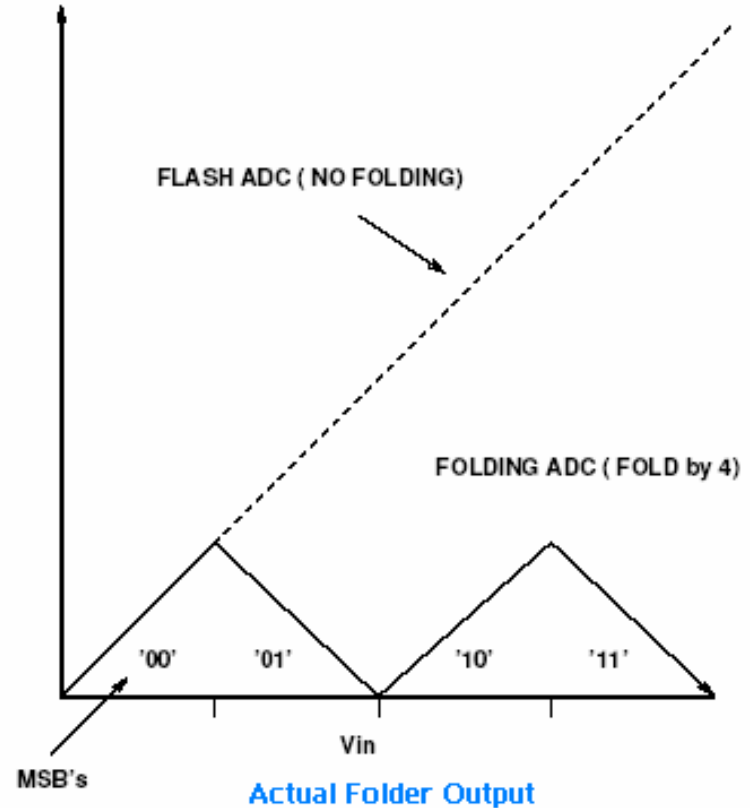
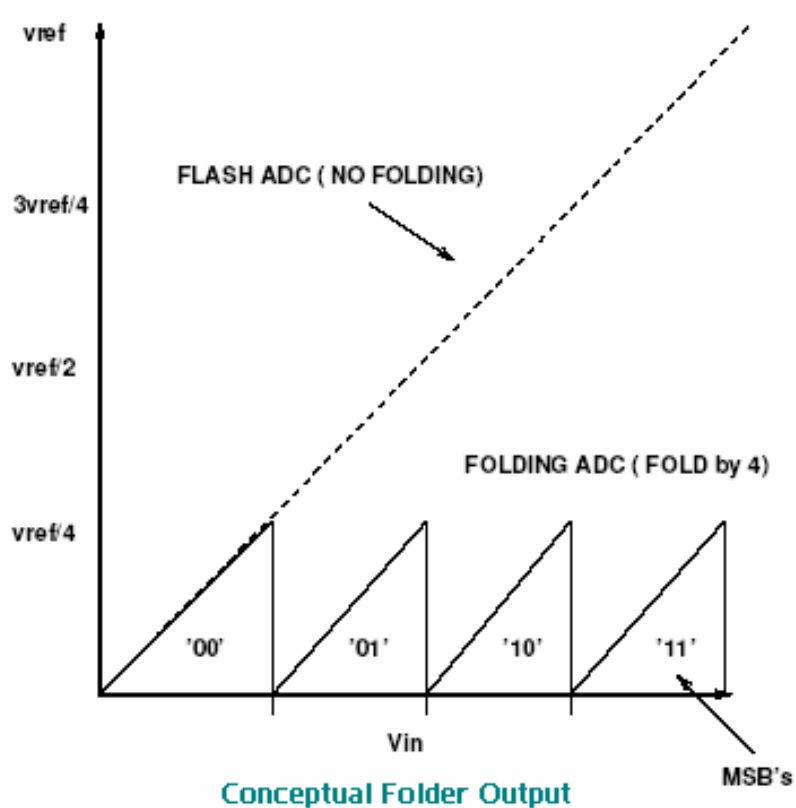


# Flash vs. Folding





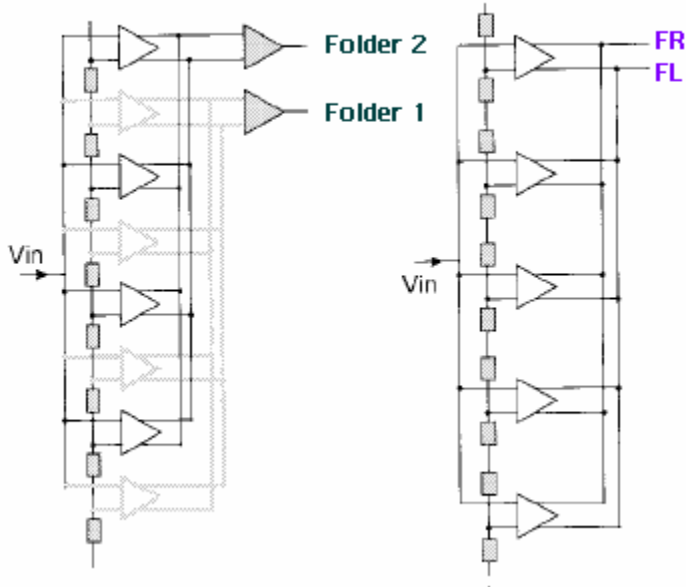
# Folding Concepts



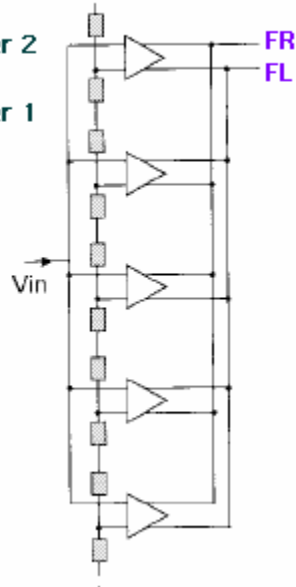


# Folding Concepts

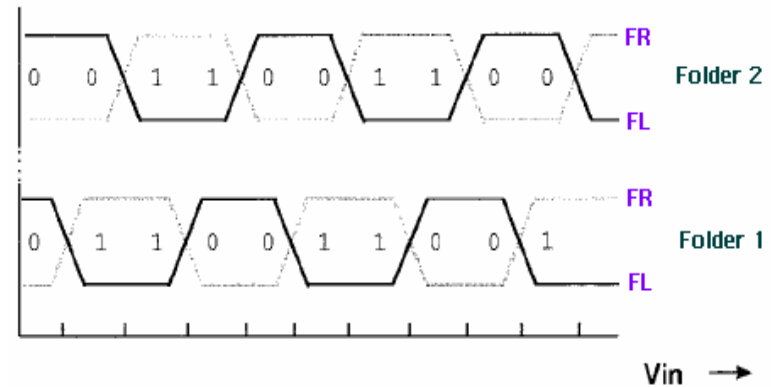
1) Full Folder Array



2) Single Folder

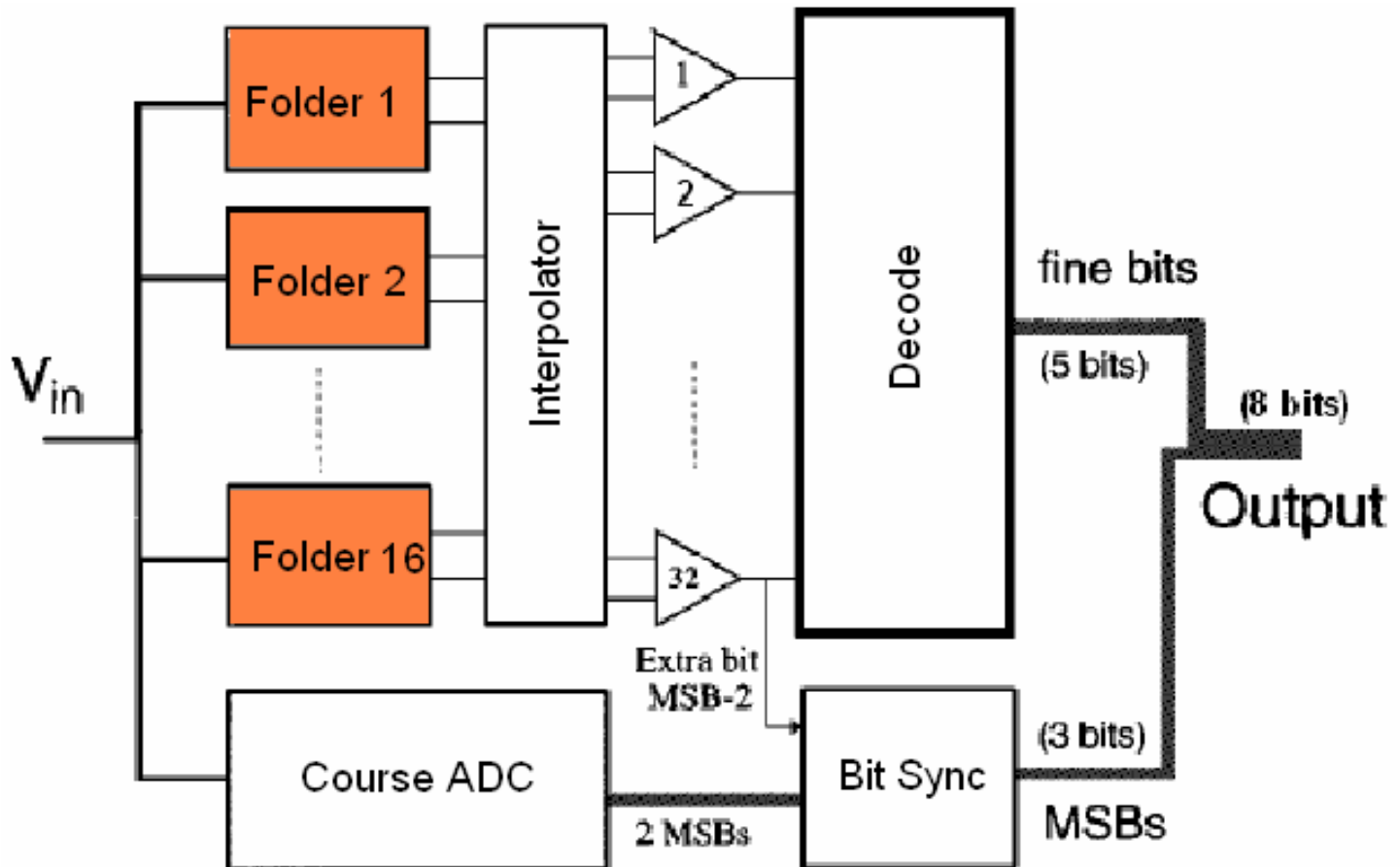


3) Cyclic Code



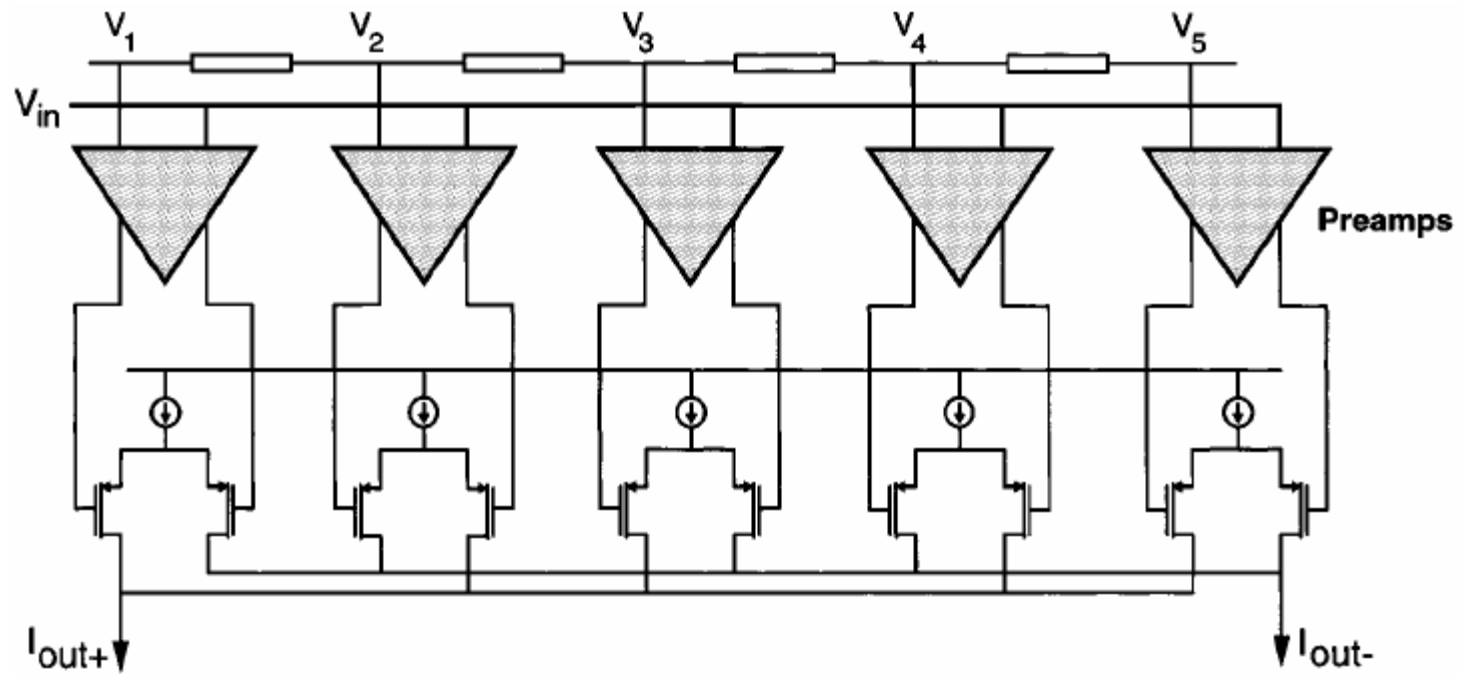


# Top Level Diagram





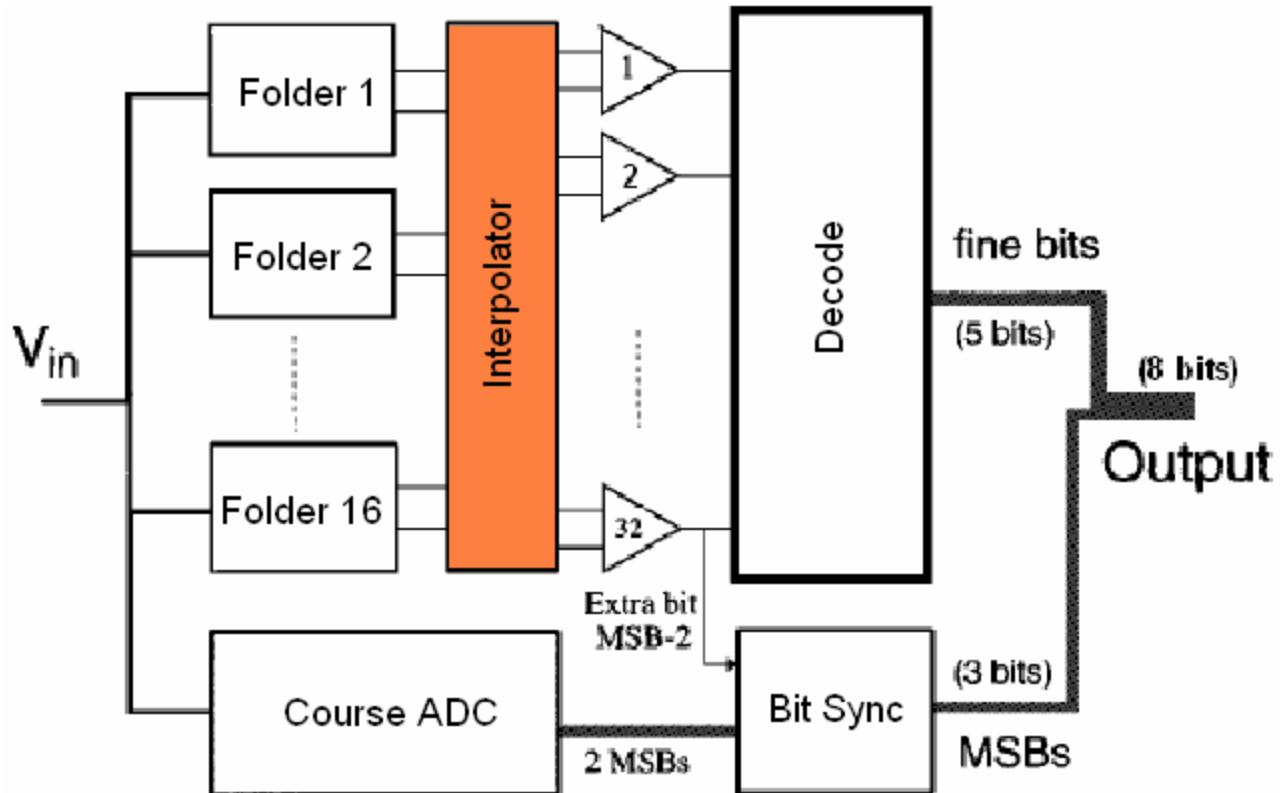
# Folders





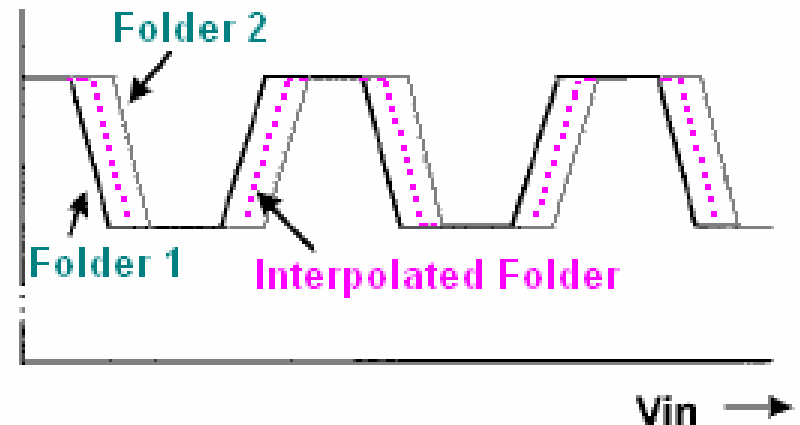
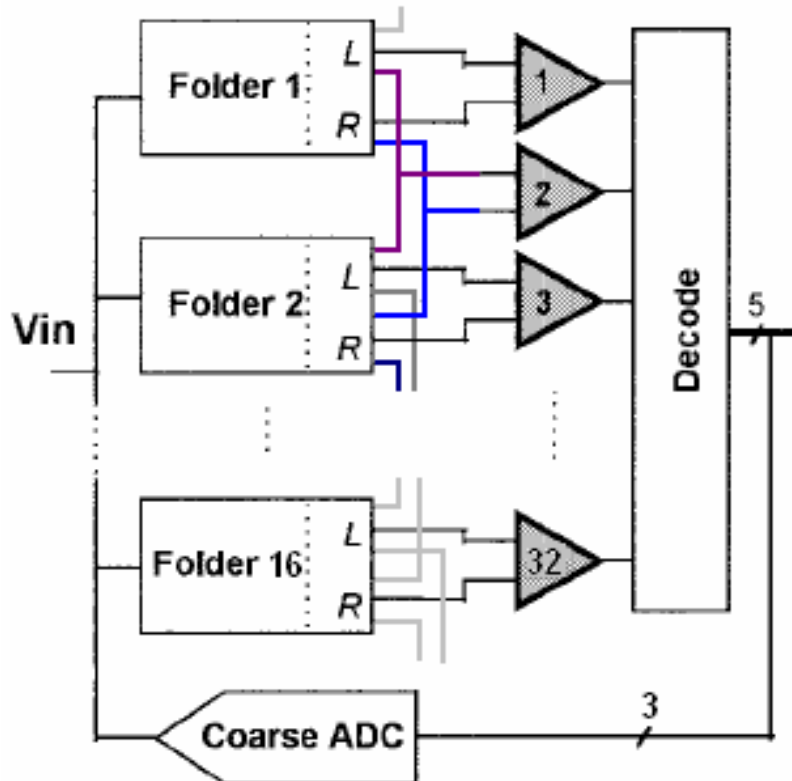


# Interpolation



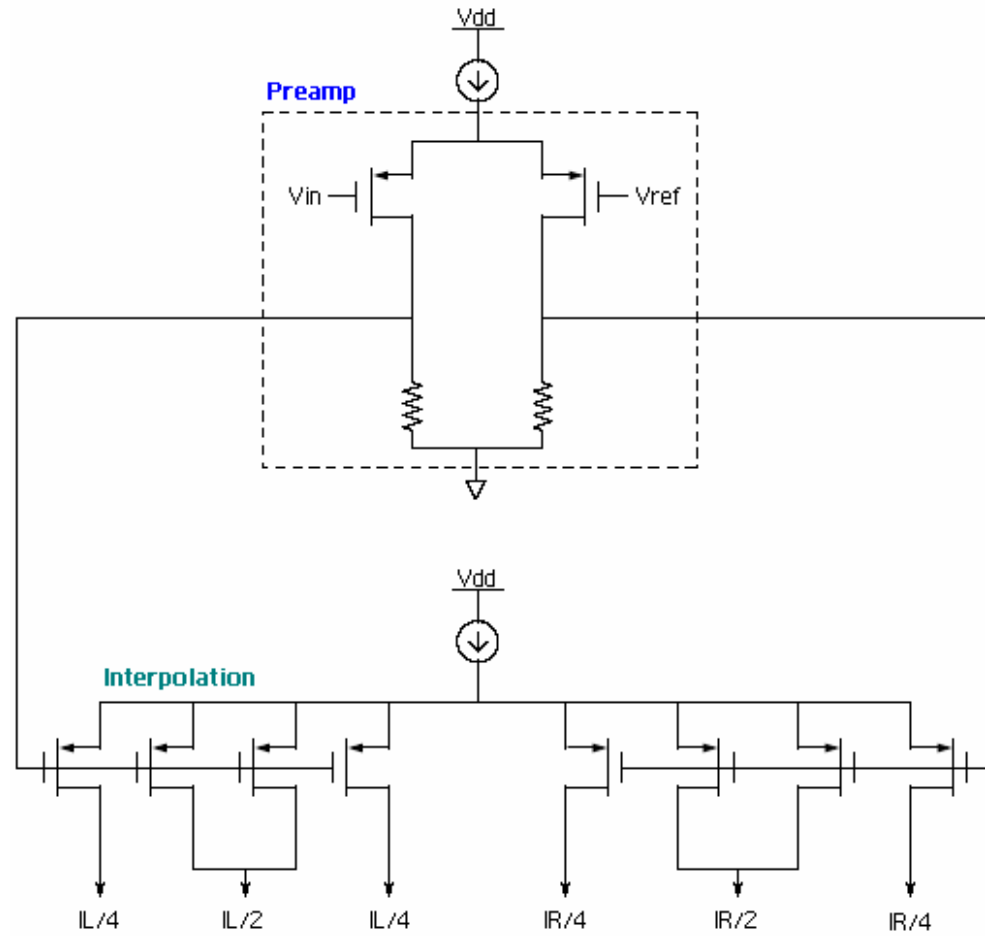


# Interpolation



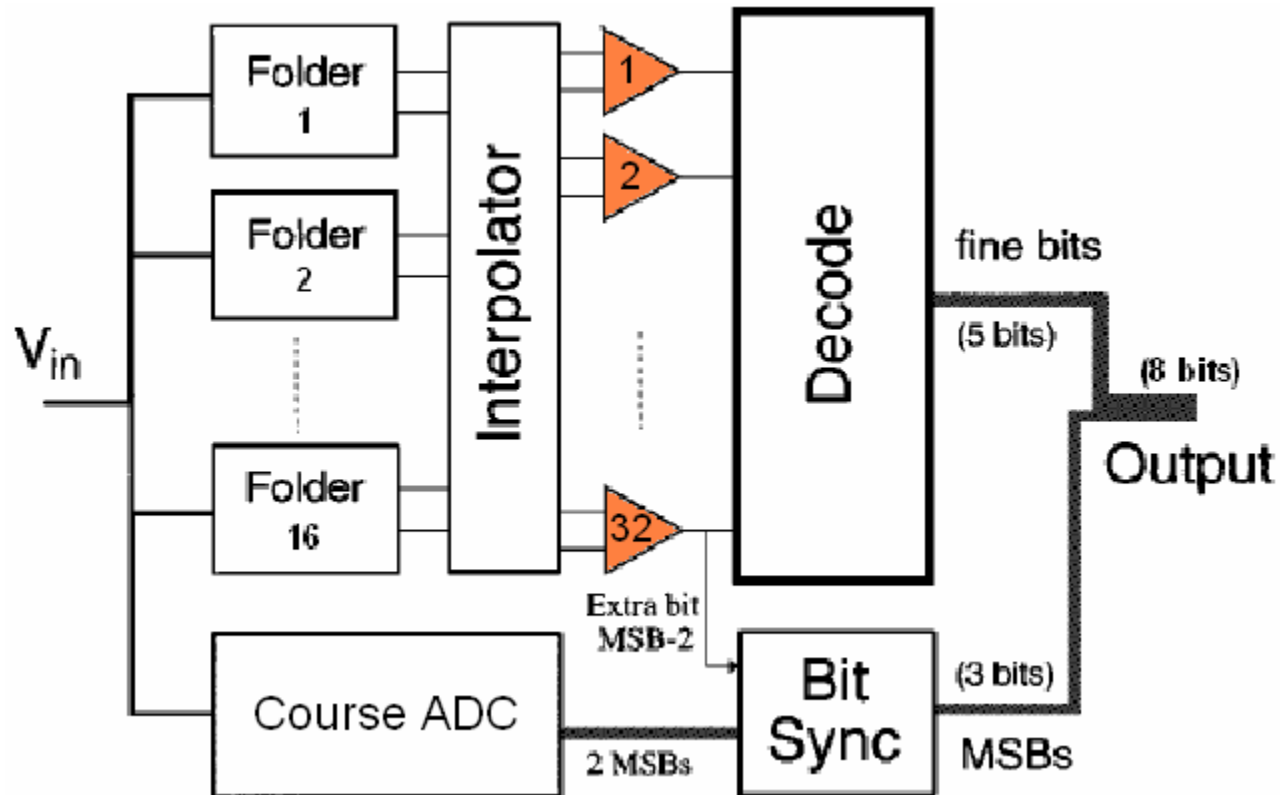


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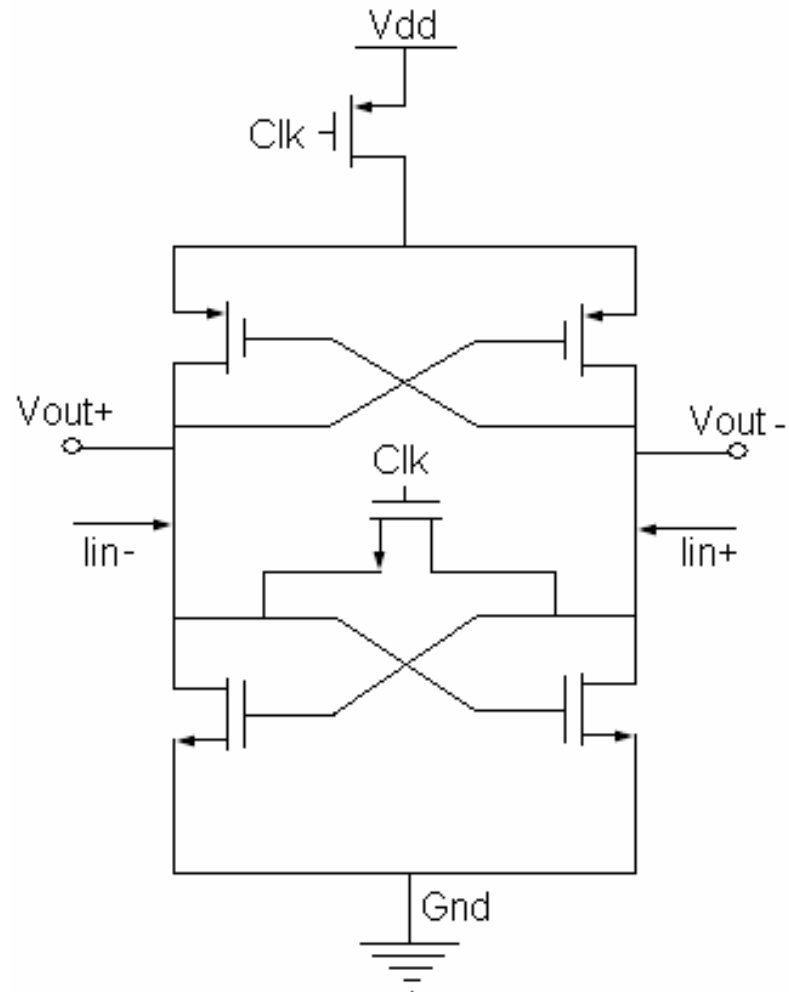


# Comparator



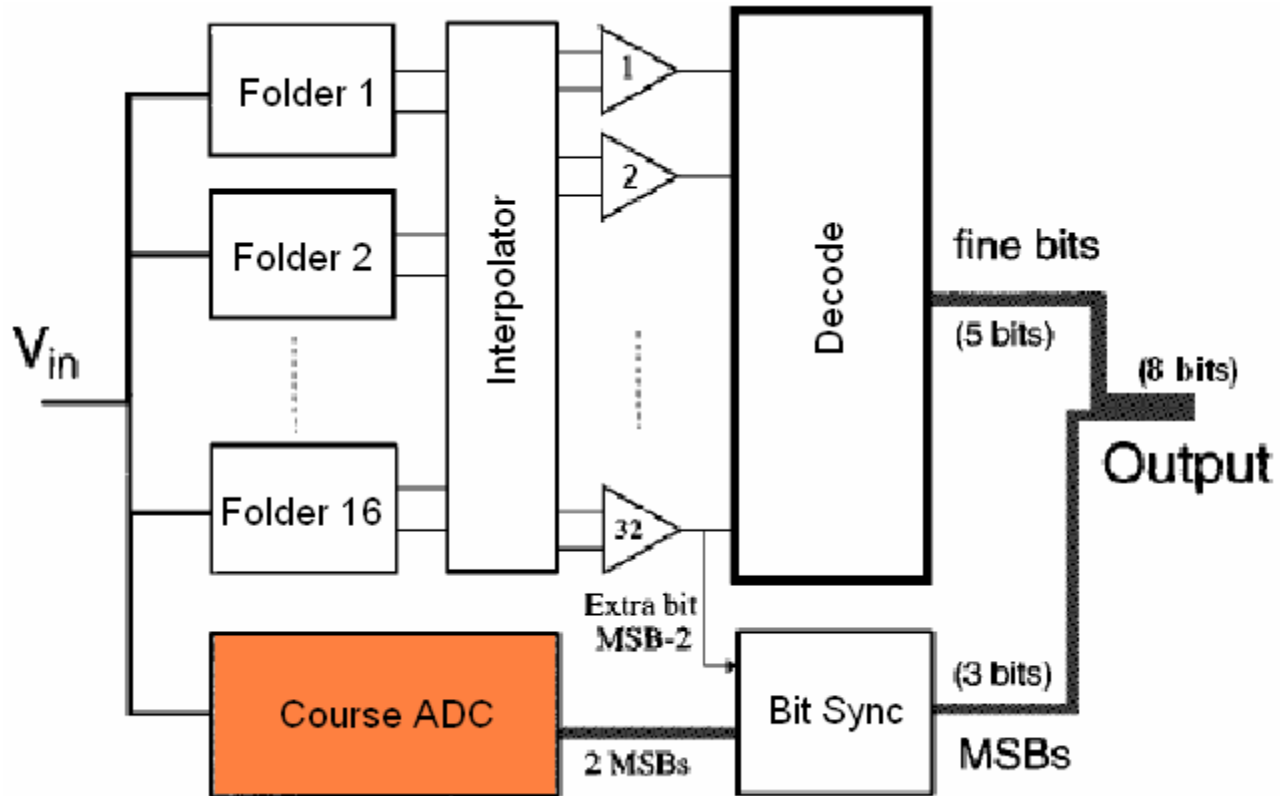


# Comparator



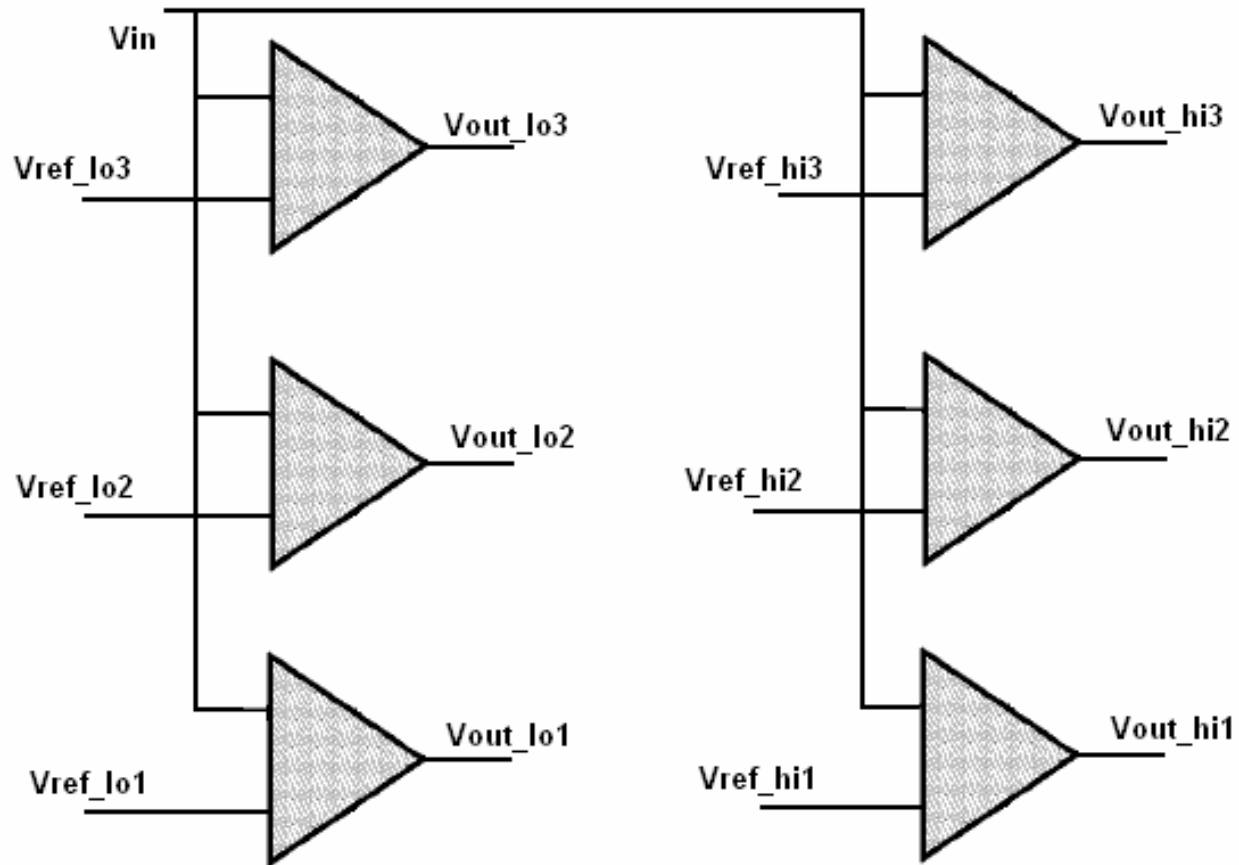


# Course ADC



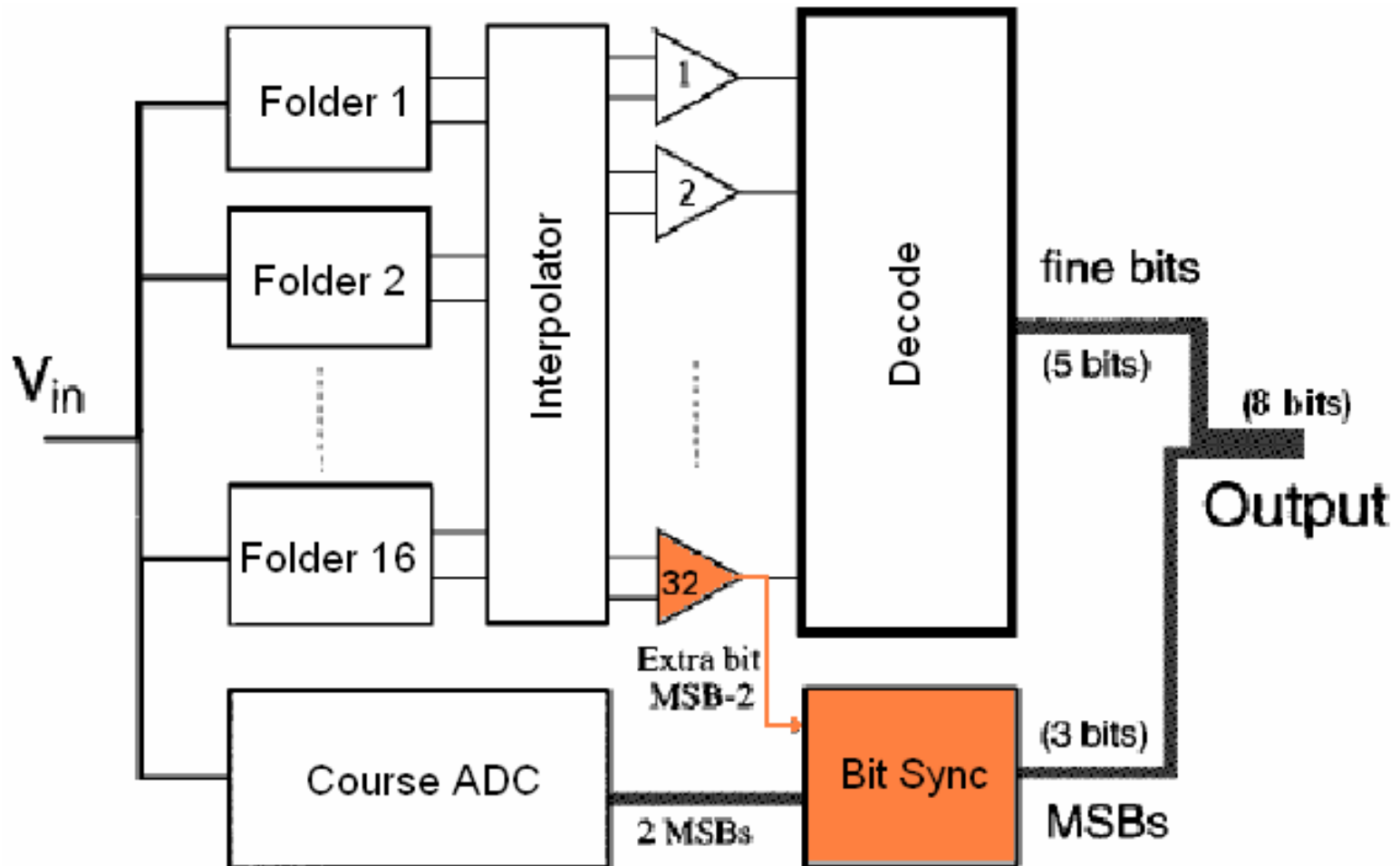


# Course ADC





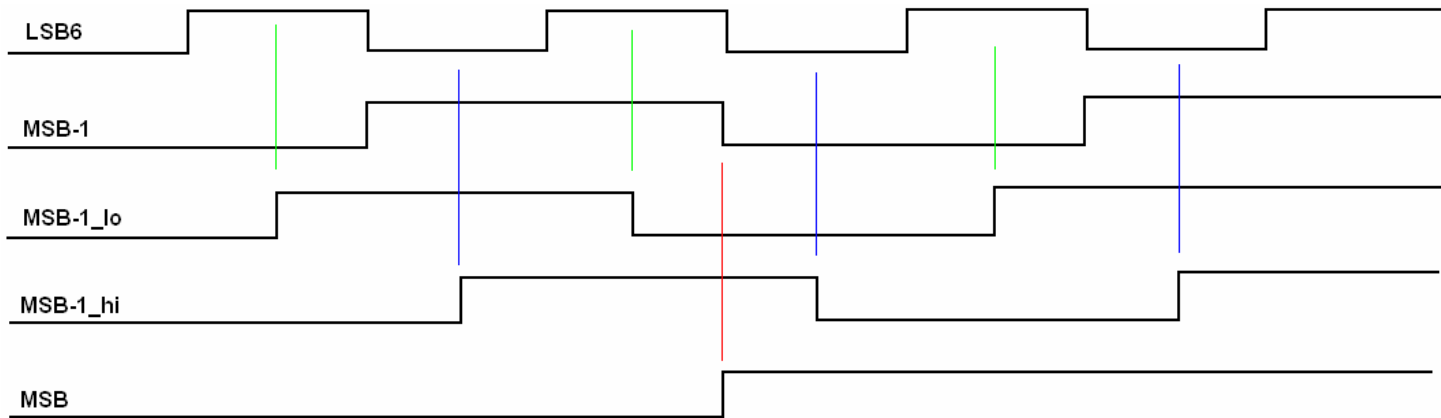
# Synchronization



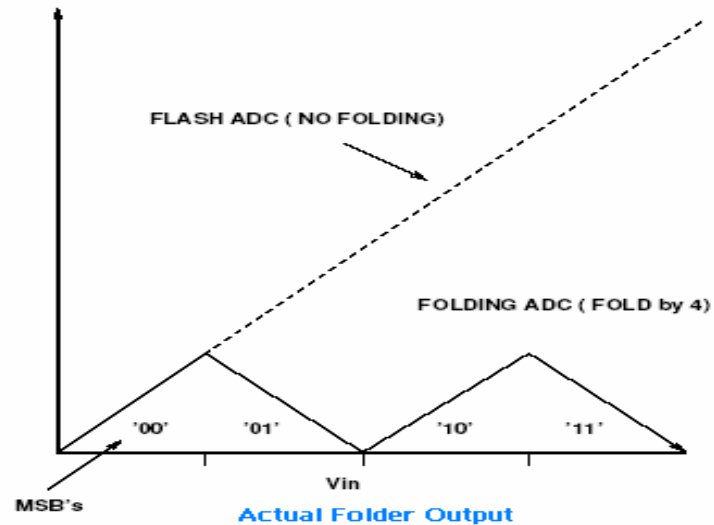




# Synchronization



$V_{in}$  →



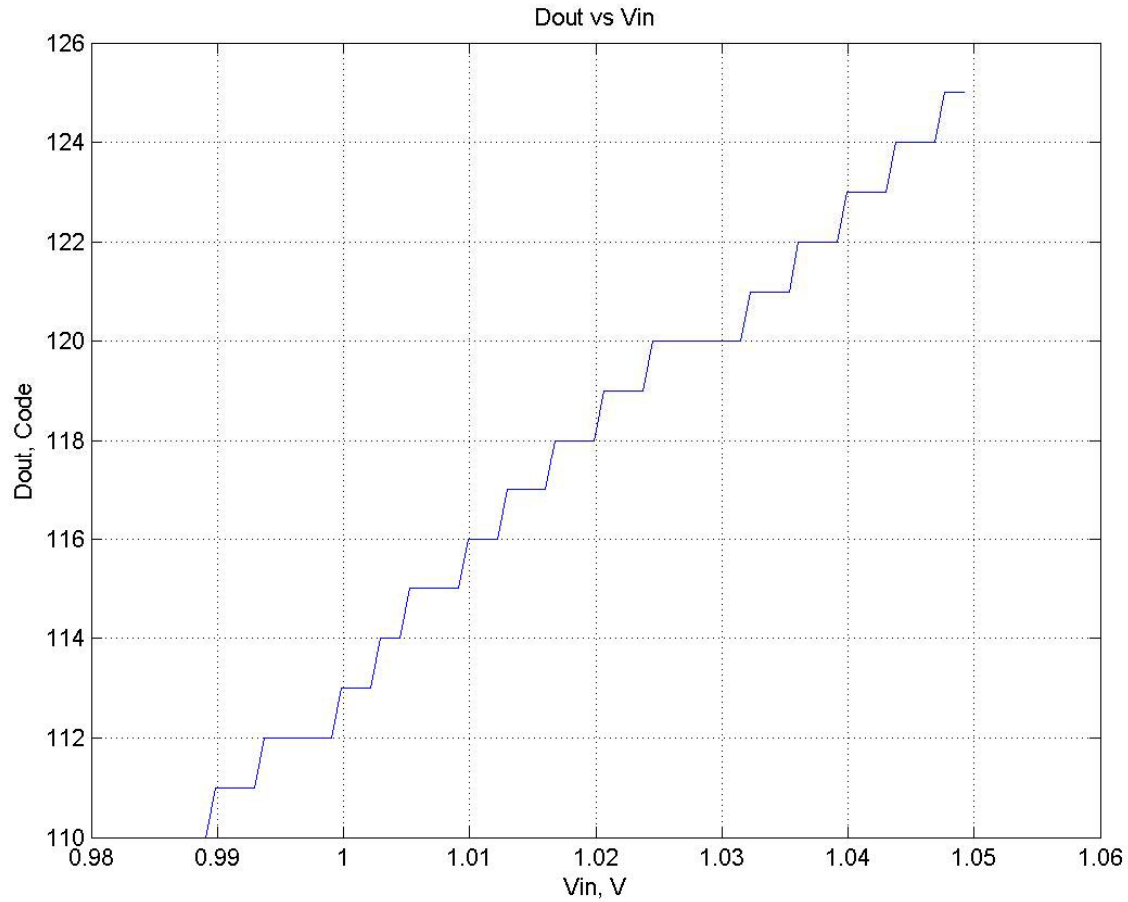


# Performance

Resolution	8 bits
Sampling Freq	400 MHz
Input Range	0.5V – 1.5V
SNDR	n/a
ENOB	n/a
DNL	0.87 LSB
INL	-.60 LSB
Power	238 mW

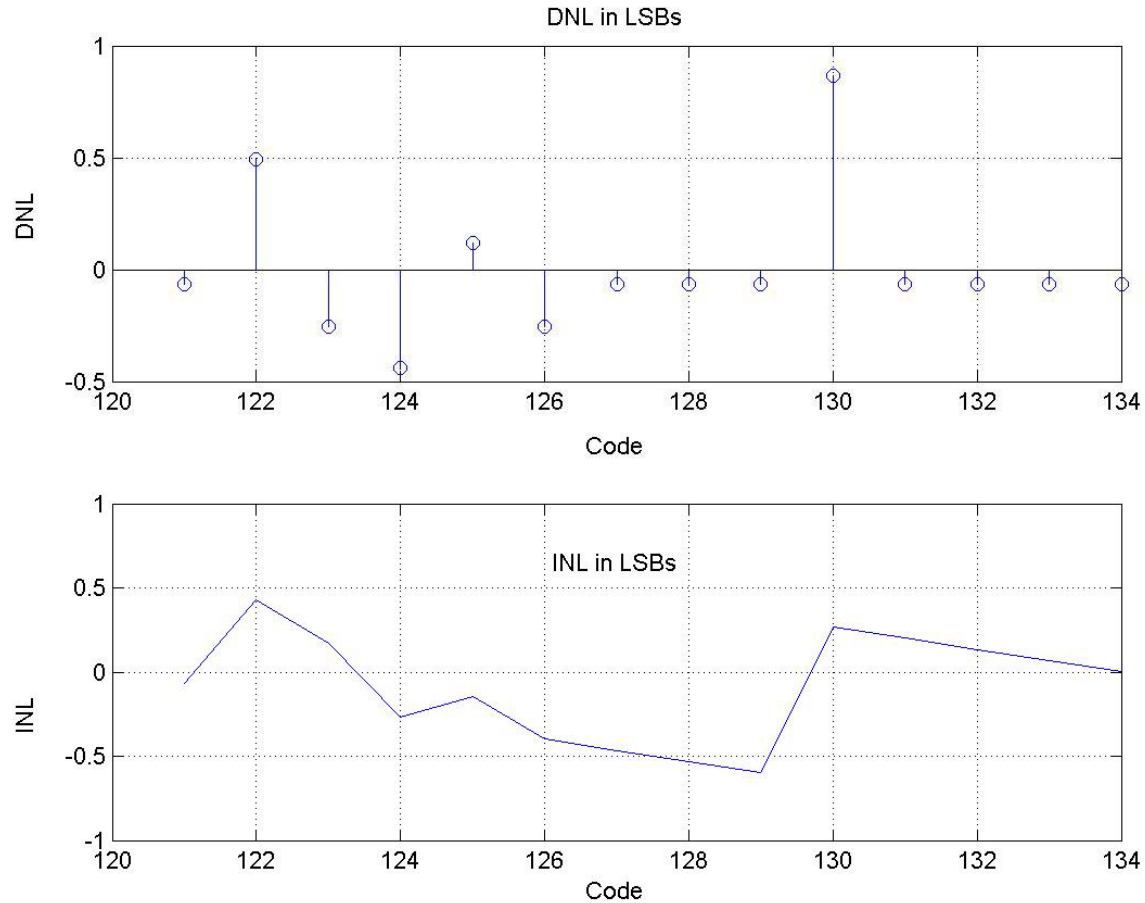


# Performance





# Performance





# Conclusion

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- Folding technique greatly reduces the number of comparators.
- Interpolation eliminates half of the folders.
- Synchronization between course and fine removes errors caused by metastability.
- Folding architecture is very effective for achieving a good resolution at low power and high speed.