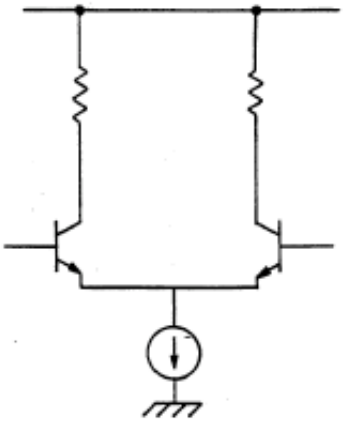
FIELD OF THE INVENTION

This invention relates to a linear differential amplifier and more particularly to a linear amplifier having three differential pairs of bipolar transistors, the gain characteristic being linearized by an offset voltage created by ratioed emitters, wherein the ratio is an integer.



PRIOR ART

FIG. 1

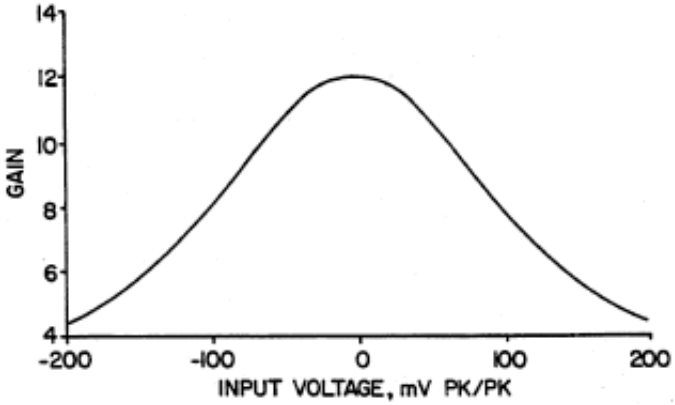
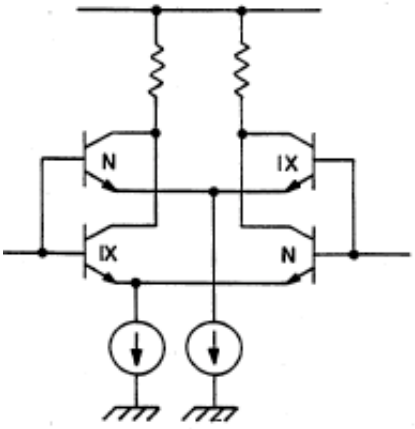


FIG. 2

BACKGROUND OF THE INVENTION

Bipolar junction transistors are non-linear transconductors and for this reason their use in linear amplifiers requires the use of special techniques such as negative feedback. Without feedback, a simple differential pair as shown in FIG. 1 has a very non-linear gain as illustrated graphically in FIG. 2. Negative feedback can be applied to a single stage amplifier in shunt mode, as in a transimpedance amplifier, or in serial mode, as in the application of emitter degeneration, or, sometimes in both shunt and serial feedback modes simultaneously. Such application of feedback generally requires the use of resistors as linear circuit elements to control the amplifier gain. In low noise amplifier applications, the use of resistors can be a disadvantage since they are a well known source of thermal noise and this impairs the amplifier noise figure. A further disadvantage of series negative feedback is that the amount of feedback depends upon the transistor bias level and in the case of a variable transconductance amplifier, the amount of feedback varies also and consequently so does the amplifier linearity. As a result, series negative feedback can be inappropriate for variable transconductance amplifiers.



PRIOR ART

FIG. 3

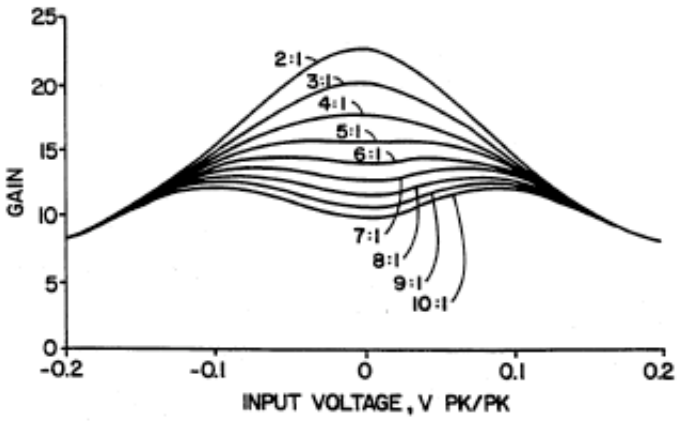


FIG. 4

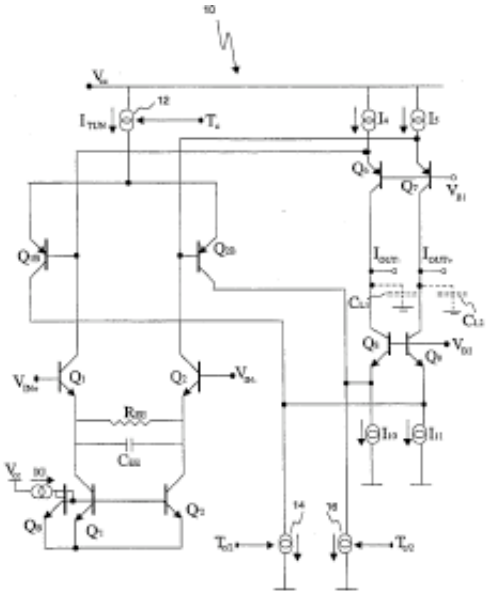
PRIOR ART

One solution to the problem of transconductor non-linearity of bipolar junction transistors was proposed by Okanobu in U.S. Pat. No. 4,965,528 issued Oct. 23, 1990. In the '528 patent the single differential pair is replaced with a pair of differential transistor pairs having ratioed transistors. According to one aspect of the patent the emitter sizes are ratioed such that in one of the pairs the emitter of one of the transistors is larger than the other by a set factor, e.g., four; while in the second pair the opposite transistor has the larger emitter based on the same ratio. Each pair of transistors is supplied with the same tail current and their inputs and outputs are connected in parallel. As a result of the ratioed emitters, the peak gain for each differential pair is offset from the centre of the input/output characteristic (in comparison to a conventional differential pair whose gain is maximized at the centre of its input/output characteristic). For emitter size ratios greater than five the combination of the two differential pairs with ratioed emitters results in the combined input/output characteristic having two maxima in the gain characteristic, either side of the centre of the range and a substantially linear characteristic in between the two maxima. This improvement in the BJT transfer characteristic is sufficient for many applications.

In U.S. Pat. No. 5,006,818 which issued Apr. 9, 1991 to Koyama et al, variations on the two differential pairs concept are disclosed. In applications where amplifier linearity is critical, however, some attempts have been made to improve the linearity by incorporating additional series negative feedback as well as attempting to

SUMMARY OF THE INVENTION

The present invention seeks to provide a linear differential amplifier which overcomes the limitation of the prior art, by utilizing three differential pairs, of which two pairs have ratioed transistor emitters, the ratios being integers. This is consistent with microwave transistor requirements since identical microwave transistors can be matched with a statistical collector current distribution having a sigma of 1 percent and ratios can be achieved by connecting transistors in parallel, or by employing multiple emitters on a single transistor.



[57] **ABSTRACT**

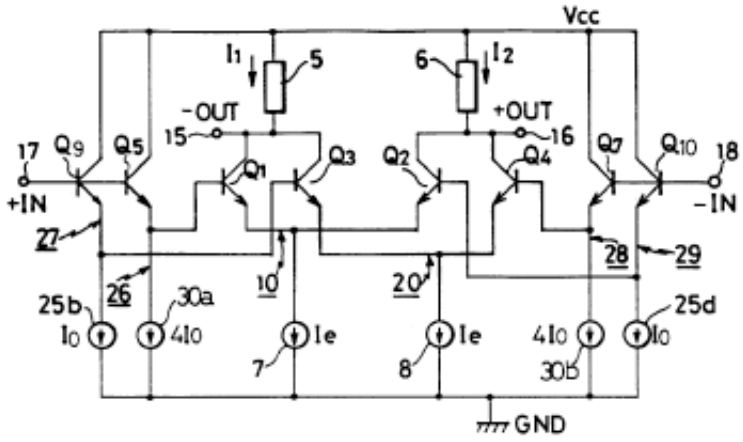
An amplifier capable of being tuned to provide linear gain over a selected input signal range is disclosed herein. The amplifier includes an input stage for receiving an input signal. The amplifier further includes a tuning circuit, connected between the input stage and an amplifier output stage, for controlling gain of the amplifier by adjusting a tuning current supplied to the amplifier output stage. The tuning circuit may be realized with a differential transistor pair connected to a pair of transistors within the output stage. In a preferred implementation the input and output stages are arranged in a folded-cascode configuration so as to improve the output impedance and input common-mode signal range of the amplifier.

FIELD OF THE INVENTION

This invention relates generally to an operational transconductance amplifier and, more particularly, to an operational transconductance amplifier in which a tuning circuit is employed to control transconductance through adjustment of an amplifier tuning current.

BACKGROUND OF THE INVENTION

Interest has recently arisen in developing wideband continuous-time filters for use in high-definition television (HDTV) systems, as well as within high-speed analog to digital converters (ADCs). High-speed, low distortion, and a wide linear tuning range are several of the desired characteristics of continuous-time filters suitable for employment in such applications.



BACKGROUND OF THE INVENTION

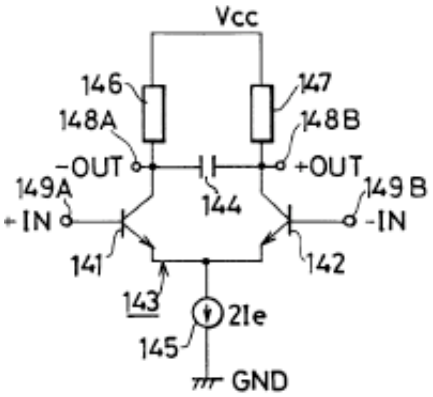
1. Field of the Invention

The present invention relates to a linear differential amplifier which constitutes a part of an electric filter or a similar device to be incorporated, for example, in an IC.

2. Description of the Prior Art

Recently, it has become a common practice to incorporate electric filters comprised of differential amplifiers in an IC. But, a differential amplifier of the operational amplifier type with double amplification stages does not possess a satisfactory frequency characteristic in the high-frequency range such as the video frequency range. Because of this, an electric filter is often realized by constructing a gyrator or a biquad filter with a differential amplifier including a capacitor as a load, which is regarded as a single stage integrator. Such a differential amplifier is shown in FIG. **1**, where it is comprised of a pair of bipolar transistors **141** and **142** which form an emitter-coupled pair **143**, a capacitor **144** connected between collectors of the transistors **141** and **142** as a load, a constant current source **145** connected between the round and emitters of the transistors **141** and **142** as a load, a constant current source **145** connected between the ground and emitters of the transistors **141** and **142** for supplying emitter currents $2I_e$, load resistors or their equivalents **146** and **147** connected to the collectors of the transistors **141** and **142**, output terminals **148**A and **148**B connected to the collectors of the transistors **141** and **142**, and input terminals **149**A and **149**B connected to bases of the transistors **141** and **142**. In FIG. **1**, V_{cc} stands for the power source voltage.

FIG. 1
PRIOR ART



However, an emitter-coupled pair formed by bipolar transistors like the one shown in FIG. **1** possesses poor linearity and changes its transconductance depending on the level of input signals. Consequently, an electric filter comprised of a differential amplifier of this type changes its characteristic depending on the level of input signals, and therefore is not satisfactory in this respect.

FIG. 2
PRIOR ART

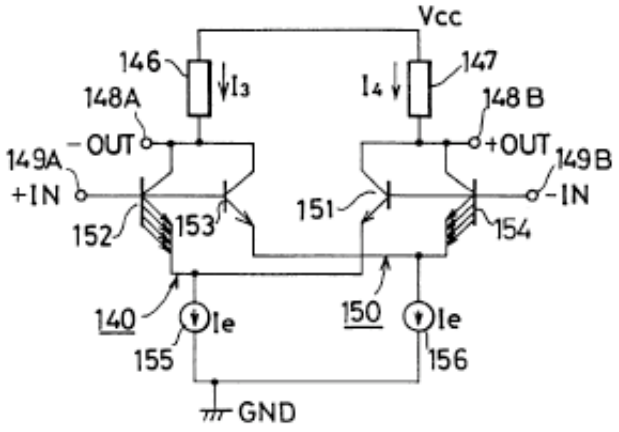
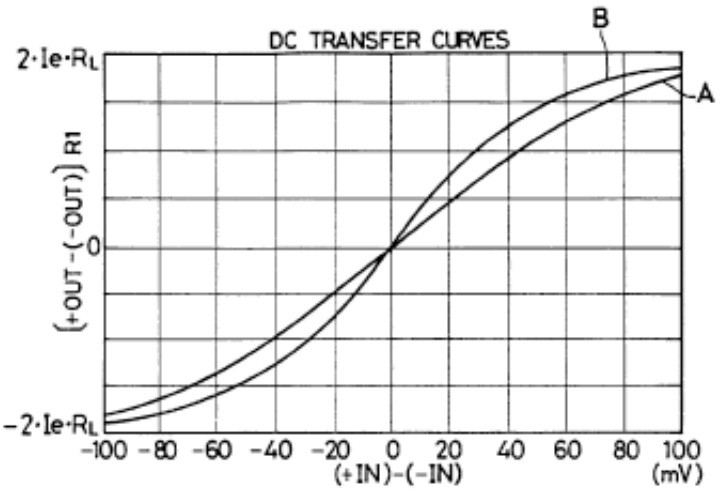


FIG.3
PRIOR ART



There has been proposed, a differential amplifier with an improved linearity, such as the one shown in FIG. **2**, which has been disclosed by J. O. Voorman et al. in "Bipolar integration of analog gyrator and Laguerre type filters" Proc. ECCTD '83, Stuttgart, pp. 108–110. This differential amplifier is comprised of two emitter-coupled pairs **140** and **150** formed by a pair of transistors **151** and **152**, and **153** and **154**, respectively, where each of the transistors **152** and **153** has an emitter area four times larger than that of the transistors **151** and **153**. Collectors of the transistors **152** and **153** are connected with each other as well as with a load resistor **146** which converts output current I_3 of these two transistors, while collectors of transistors **151** and **154** are connected with each other as well as with a load resistor **147** which converts output currents I_4 of these two transistors. It further includes a constant current source **155** for the emitter-coupled pair **140** for supplying emitter current I_e, and a constant current source **156** for the emitter-coupled pair **150** for supplying emitter currents I_e, output terminals **148**A and **149**B connected to the collectors of the transistors

FIG. **3** shows the input-output characteristic of this differential amplifier contrasted with that of the conventional one. In FIG. **3** curve A is the characteristic curve of the differential amplifier of FIG. **2** while curve B is the characteristic curve of the differential amplifier of FIG. **1**, and R_L is the resistance of the load. By comparing these two characteristic curves, it can be seen that the range of input levels with the output distortion up to 1% has been increased from ±17 mVpp for the differential amplifier of FIG. **1** to ±48 mVpp for that of FIG. **2**.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a differential amplifier capable of achieving an improved linearity, a good high-frequency characteristic, a good S/N ratio, a high direct current gain, and a high-speed operation, all at once.

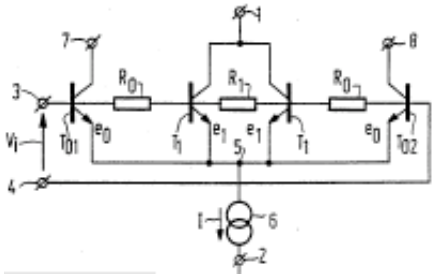
DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. **5**, there is shown a first embodiment of a linear differential amplifier according to the present invention.

It should readily be understood that the specific ratio such as 1:4 or 1:2 has been used in the preceding descriptions for the sake of definiteness, but they only need to be followed approximately, and practically the same advantages can be obtained with such approximation.

It can also be seen that a linear differential amplifier of the present invention can be utilized not only in an electric filter, but anywhere where the improved linearity of an amplifier is desirable such as, for example, an initial stage for an amplifier of the operational amplifier type.

Furthermore, many modifications and variations of the embodiments explained may be made without departing from the novel and advantageous features of this invention. Accordingly, all such modifications and variations are intended to be included within the scope of the appended claims.



[57] **ABSTRACT**

A transconductance amplifier comprising a voltage divider including two identical resistors (R_o) connected between the bases **(3, 4)** of two first transistors (T_{o1}, T_{o2}) arranged as a differential pair, each having a first emitter area (e_o). The junction point of said resistors (R_o) is connected to the base of a second transistor (T_1) having a second emitter area ($2e_1$), whose emitter, like that of the first transistors (T_{o1}, T_{o2}), is connected to a current source **(6)**. For a ratio between the second and the first emitter areas ($2e_1$; e_o) equal to 4:1 the difference between the output currents (I_1, I_3) of the first transistors (T_{o1}, T_{o2}) increases as a linear function of the input voltage over a range which is as large as possible.

TRANSCONDUCTANCE AMPLIFIER

BACKGROUND OF THE INVENTION

The invention relates to a transconductance amplifier comprising two transistors T_o each having an emitter area e_o, their bases constituting inputs for receiving an input voltage and their emitters being connected to a current source, and further comprising at least a first output for an output current.

Such transconductance amplifiers, briefly referred to as transconductors, are suitable for general uses and in particular for use in filter circuits, multipliers and oscillators.

A transconductor is a voltage-controlled current source in which the proportionality factor between the output current and the input voltage is given by the transconductance. The simplest transconductor is a differential amplifier, by means of which a voltage applied between the bases is converted into two collector signal currents of opposite phase. In a differential amplifier these signal currents increase as a linear function of the input voltage over a small range only, so that the transconductance is only constant over a very small range of input voltage. The article "Bipolar Integration of analog gyrator and laguerre type filters (transconductor-capacitor filters)" in Proceedings ECCTD'83, September 1983, pages 107–110 describes a linearised transconductor which comprises two parallel-connected differential amplifiers, the transistors of each amplifier having different emitter areas and the bases and the collectors of two transistors having different emitter areas being interconnected. In the case of a suitable choice of the ratio between the emitter areas of the transistors, the linear range of this transconductor is approximately five times as large as that of a single differential amplifier. In addition, this known transconductor may be arranged to form a square-law transconductor, in which the output current increases as a square-law function of the input voltage over a specific range. In this case the collectors of the transistors whose bases are interconnected are not coupled to each other but are cross-coupled to the collector of the corresponding transistor of the other differential amplifier.

SUMMARY OF THE INVENTION

It is an object of the invention to provide a transconductor which makes it possible to obtain both a linear and a square-law transconductor with a larger useful output-voltage range. In accordance with the invention a transconductor of the type defined in the opening paragraph is characterized in that

The manner in which the collectors of the transistors T_o and $T_1, \ldots, T_N, T_N, \ldots, T_1$ are connected depends on whether the circuit is to be used as a linear transconductor, in which the output current increases, as far as possible, as a linear function of the input voltage, or as a square-law transconductor, in which the output current increases, as far as possible, as a square-law function of the input voltage. In the case of a linear transconductor a distinction should be made between class AB and class A operation of the transconductor. A class AB transconductor is to be understood to mean a transconductor whose bias current increases as the input voltage V_i increases, and a class A transconductor is to be understood to mean a transconductor whose bias current is independent of the input voltage V_i.

A class AB linear transconductor in accordance with the invention may be characterized in that the collectors of the transistors $T_1, \ldots, T_N, T_N, \ldots, T_1$ are connected to a power-supply terminal and in that the collectors of the transistors T_o constitute the outputs of the transconductance amplifier. The difference between the collector currents of the transistors T_o then increases as a linear function of the input voltage over a specific range. As a result of the class AB operation of the circuit the bias current is comparatively small for low input voltages. As a result of this the noise level and the d.c. offset at low input voltages are small.

It is to be noted that apparently the construction of such a class AB transconductor for which $N=1$, and the resistance value $W_1=0$ bears some resemblance to the differential amplifier shown in FIG. 1 of European Patent Application No. 0157447. In said differential amplifier the bias current also increases as the input voltage increases. However, this step is not aimed at increasing the linear range but at increasing the slew rate, i.e. the maximum rate at which the output signal of the amplifier can vary in the case of capacitive loading. Moreover, the amplifier is a negative-feedback differential amplifier in which the emitters, in contradistinction to the transconductor in accordance with the invention, are not connected directly to the bias-current source but via a resistor. A transconductor in accordance with the invention maintains its linearity over a wide range of bias current, whereas the circuit for increasing the slew rate only operates in a small current range around the value for which the circuit has been designed.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** is the circuit diagram of a class-AB linear transconductor in accordance with the invention. Between a first power-supply terminal **1** and a second power-supply terminal **2** the transconductor comprises two transistors T_{o1} and T_{o2} whose bases **3** and **4** constitute the inputs for receiving an input voltage V_i and whose emitters are connected to the output **5** of a current source **6** which can supply a current I. A voltage divider is arranged between the bases **3** and **4** and comprises $2N+1$ resistors $R_o, R_1, \ldots, R_{N-1}, R_N, R_{N-1}, \cdot$

The properties of the class AB linear transconductor in accordance with the embodiments shown in FIGS. **4** to **8** are given in the following Table. The Table also gives the properties of a normal differential amplifier and the transconductor in accordance with the aforementioned article in the Proceedings ECCTD'83.

TABLE

Type of transconductor	$\Delta = 1\%$ (mV)	C.E. (%)	S
Differential amplifier (prior art)	6	6	I
Proc. ECCTD'83 (prior art)	30	40	I
FIG. 4	60	40	I/3
FIG. 5	142	47	I/6
FIG. 6	255	51	I/10
FIG. 7	400	53	I/15
FIG. 8	575	55	I/21

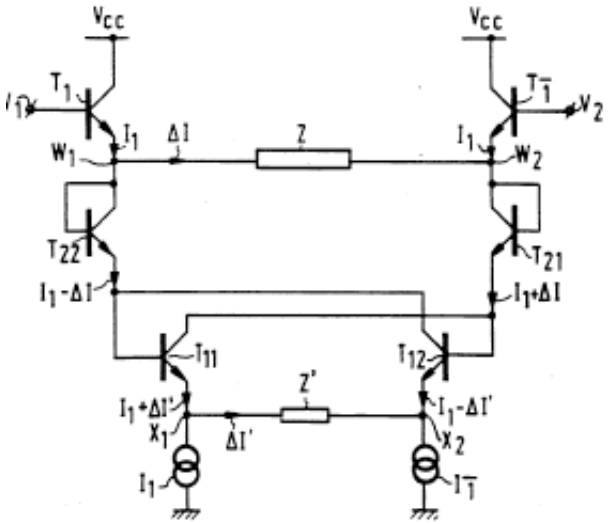
For each transconductor the above Table consecutively gives: the voltage for which the departure from the linear characteristic has increased to 1%; the current efficiency (C.E.) which indicates the fraction of the current I to which the signal current is equal when the

1% linearity deviation is reached, and the effective bias current (S) for low input voltages.

It follows from the Table that the simplest embodiment of the class AB transconductor (FIG. **4**) already has a linear voltage range which is $2\times$ as large as that of the known transconductor and a linear voltage range which is $10\times$ larger than that of a normal differential amplifier. This linear range becomes increasingly larger for the consecutive embodiments. The effective bias current S then decreases, which means that the noise level and the d.c. offset are also further reduced.

[57] **ABSTRACT**

A distortion compensated differential circuit. One embodiment of the circuit includes a differential follower stage comprising first (T_1) and second ($T_{\bar{1}}$) transistors having their respective collectors connected to a supply voltage source (V_{cc}). The bases of these transistors receive a first (V_1) and a second (V_2) input signal and their emitters are coupled together by a first impedance (Z) and are further connected to a first (I_1) and a second ($I_{\bar{1}}$) current source, respectively. The connections between the emitters of the first and the second transistors and the first and the second current sources, respectively, are made via the base-emitter paths of third (T_{11}) and fourth (T_{12}) transistors, respectively. The collectors of the third (T_{11}) and the fourth (T_{12}) transistors are connected to the bases of the fourth (T_{12}) and the third (T_{11}) transistors, respectively. The emitters of the third (T_{12}) and the fourth (T_{12}) transistors are coupled to one another by at least a second impedance (Z') of a nominal value which is less than that of the first impedance.



BACKGROUND OF THE INVENTION

This invention relates to a distortion-compensated differential circuit which comprises a differential stage comprising a first and a second transistor whose emitters are coupled by a first impedance, and input terminals for an input signal source, and which also comprises a distortion compensation circuit comprising in series between the emitter of the first transistor and a first current source, a first diode as well as the main current path of a third transistor, and also comprising, in series between the emitter of the second transistor and a second current source, a second diode as well as the main current path of a fourth transistor, which third and fourth transistors have their respective bases and collectors interconnected and have their emitters coupled by a second impedance.

Such a differential circuit is known from U.S. Pat. No. 4,682,098 in the form of a voltage-current converter comprising a voltage source V, the first impedance being constituted by a resistor which converts said voltage into a current which is amplified by a translinear circuit comprising four transistors. The first and the second transistor have their collectors as well as their bases interconnected. In order to compensate for conversion non-linearity caused by the non-linearity of the emitter resistance of the first and the second transistor, U.S. Pat. No. 4,682,098 couples a resistor of the same value as the first resistor between the emitters of the third and the fourth transistor.

This compensation provides very remarkable results in the case of small signals.

However, in particular in the case of flash-type fold and interpolation analog-to-digital converters, there is a need to provide compensation over a very wide dynamic range, up to levels of several volts at the output of a differential amplifier.

SUMMARY OF THE INVENTION

It is an object of the invention to provide such a compensation.

To this end the second impedance has a nominal value smaller than that of the first impedance.

As will be demonstrated hereinafter, this very simple modification enables the distortion figures to be improved by providing compensation for the base currents of the third and the fourth transistor, at least to a specific degree.

In a preferred embodiment the circuit is characterized in that the ratio between the second impedance and the first impedance is within the range of values from 0.65 to 0.85.

In a first modification, derived from said U.S. Pat. No. 4,468,098, the differential stage is adapted to form a voltage-current converter, said input terminals being arranged in series with the first impedance.

In a second modification the differential stage is adapted to form a differential follower, the bases of the first and the second transistor forming said input terminals.

The invention also relates to a multiple follower circuit, in particular for use in flash-type folding and interpolation analog-to-digital converters.

Such a multiple follower circuit comprises a plurality of differential follower circuits as defined above, the

first, the second, the third and the fourth transistor of the differential follower circuit of the rank i being denominated T_i^A, $T_{\bar{i}}^A$, T_i^C and $T_{\bar{i}}^C$ respectively. This multiple follower circuit, comprises first impedances connected between the emitters of at least some of the transistors of a first group comprising the first and the second transistor, the admittance of said first impedances being designated Y followed by two indexes corresponding to those of the two transistors of said first group between whose emitters said impedance is connected, and second impedances connected between the emitters of at least some of the transistors of a second group comprising the third and the fourth transistor, the admittance of said second impedances being designated Y' followed by two indexes corresponding to those of the two transistors of said second group between whose emitters said impedance is connected, and regardless of i, j, $\bar{i}$ and $\bar{j}$ the following is valid

$$Y_{ij} = Y_j - > Y'_{i\bar{j}} = Y_j -$$

$$Y_{\bar{i}\bar{j}} = Y_j - > Y'_{i\bar{j}} = Y -$$

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In FIG. **1** a voltage-current converter comprises a source I'_1 of current (value $2I_o$) coupled to a terminal **1**, which is at a reference potential, by means of a diode-connected transistor Q_1 and to a terminal **2** by means of a diode-connected transistor Q_2. The bases of the transistors Q_3 and Q_4 are connected to the terminals **1** and **2**, respectively. The emitters of the transistors Q_3 and Q_4 are coupled to a source I'_2 of current (value $2I_x$). A voltage source V and a resistor R_1 are arranged in series between the terminals **1** and **2**, the resistor R_1 producing a voltage-to-current conversion. The current is amplified by the translinear circuit (Q_1, Q_2, Q_3 and Q_4) and is supplied to the output by the transistors T_9 and T_{10}. A compensation circuit **5** provides correction for the nonlinearity of the emitter resistance R_eQ_1 and $R_{e\,Q2}$ of the transistors Q_1 and Q_2 respectively.