======NMOS Noise Voltage Test=======

HOW TO DO CMOS NOISE MODEL VERIFICATION.

Graph 5 – noise58: NMOSNoiseVoltage

Units — unknown.V10u, unknown.V1000u, unknown.V100u

10^-5, 10^-6, 10^-7, 10^-8, 10^-9

1, 10, 100, 10^3, 10^4, 10^5, 10^6

frequency Hz

NMOS Noise Voltage Test

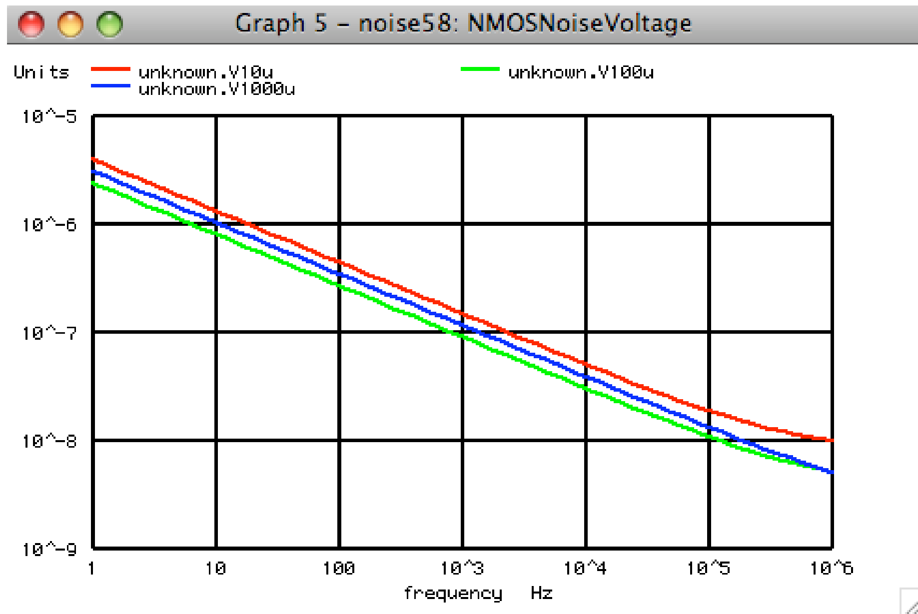
```
*
*       _|_______|_             Tox = 160Angs
*      ///      /_|_\
*               \/ \/ I1
*               /\_/\           Glass is 10e10 to 10E14 Ohms-m
*               \___/           10Ee10*160E-10/(.8e-6*40e-6) = 5e12 Ohms to 5e16 Ohms
*                 |             At Vtox = 1V   expect  .5pA to .05fA
*        |_______|
*        |_____||_|             .5pA   = 3,125,000 electrons/sec
*       VG     || ->            .05fA   =        32.5 electrons/sec
*               _|_  VS
*              /VIN\
*              \___/            1 electron @ 40fF = 4uV
*               _|_
*               ///
*
*
*         SPICE MODEL
*                                 __/\  ______|(D)|  Drain
*           CGD                  |    \/ RD   |___|
*       1.2fF _________________|__________
*            _|_      _|_      _|_    _|_
*      Gate  ___     /___\ I_ds  ^     ___  CBD
*             |      \/ \/      /_\     |  90fF   <- (Caps for L/W .8u/40u)
*     |(G)|___|      /\_/\  |    |______|
*     |___|   |___    \___/  V  __|     |_________|___|   Bulk
*             |   |     |        |      _|_ 90fF  |___|
*            _|_  |__/ \___||_|  \ /    ___
*      1.2fF ___        40fF||     V_    |  CBS     \(B)/SUB=gnd!
*             |_________|________|_______|           \ /
*            CGS        CGS  |                        V
*                            |__/\  ______|(S)|
*                                 \/ RS   |___|  Source
*
*        BiCMOS typical noise    IDS =20uA @3V    tox=160A
*        Hz          nV/rt_Hz        nV/rt_Hz
*        freq       NMOS 40/.8      PMOS 40/.8
*        10            800             150
```

```
*       100           400             60
*       1000          150             30
*       10000          50             20
*       100000         10             15

vin                 VS   0   DC    0.0  ac  1.0u
I1                  0    VG  10uA
m1                  VG   VG  VS    0    N1   W=40u     L=.8u

.model              N1                NMOS
+ Level=  8         Tnom=27.0
*-------------------Process-----------------------------------------------
+ tox=160e-10       xj=0.25e-06       nch=0.5e+17
*-------------------V_threshold-------------------------------------------
+ vth0=0.72         nlx=0.12e-06
*-------------------Bulk--------------------------------------------------
+ k1=1.04           k2=-1.209E-01
+ cdsc=-2.4E-4      cdscd=-1.506E-04   cdscb=-2.219E-04
*-------------------mobility----------------------------------------------
+ u0=678            ua=8.964e-10
+ ub=1.472e-18      uc=-4.441E-17      vsat=86000
*-------------------Subthresshold-----------------------------------------
+ nfactor=1.8
+ cit=-5.0E-04      voff=-7.862E-02
+ eta0=4.441e-16    etab=-2.E-01       dsub=0.7
*-------------------Hot electrons-----------------------------------------
+ alpha0=1.61e-05   beta0=36.68
*-------------------VAF---------------------------------------------------
+ lint=.12e-06      pclm=.19           pscbe1=3.79e+08   pscbe2=9.4e-05
+ delta=0.01655     pvag=0.4484
*-------------------Bulk_diode--------------------------------------------
+ js=5.858e-08
*-------------------Resistance--------------------------------------------
+ rsh=70            rdsw=375
+ wr=0.7586         prwb=0             prwg=-4.441E-17
*-------------------Capacitance-------------------------------------------
+ cj=0.0002424      cjsw=2.73e-10      mj=0.3551           mjsw=0.3873
+ cgso=9e-13        cgdo=9e-13         cgbo=7e-10
+ pb=0.5614         pbsw=0.8           xpart=0
+ dlc=5e-08         dwc=1.5e-07
*-------------------BulkChargeEffect--------------------------------------
+ a0=0.7            a1=0                a2=1                ags=0.05583
+ b0=6.305e-08      b1=6.579e-08        keta=-1.531E-02
*-------------------ShortChannel------------------------------------------
+ dvt0=2.2          dvt1=0.53          dvt2=-1.521E-01      drout=0.76
+ pdiblcb=.4        pdiblc1=0.00886    pdiblc2=0.00029
*-------------------NarrowChannel-----------------------------------------
+ w0=2.6e-04        wint=0.16e-06
+ ww=-9.525E-14     wwn=1.0
+ dvt0w=0           dvt1w=5.3e6        dvt2w=-1.E-01
+ k3=2.53           k3b=-5             dwg=0                dwb=0
*-------------------Noise-------------------------------------------------
+ af=1              kf=5e-29           ef=0.95
*-------------------Temperature-------------------------------------------
+ pvsat=0           ute=-1.258E+00     kt1=-3.85E-01
+ kt1l=0            kt2=-3.098E-02     ua1=5.705e-09
+ ub1=-1.147E-17    uc1=-1.302E-01     at=20380
* prt=-3.287E+02    lk1=0              lk2=0
+ lvsat=0           la0=0              lags=0             lute=0
+ luc=0

.control
setplot             new
let                "V10u"    =     0*vector(61)
let                "V100u"   =     0*vector(61)
let                "V1000u"  =     0*vector(61)
op
noise              v(vg) vin dec 10 1 1000k 1
destroy
let                unknown.V10u = sqrt(v(onoise_spectrum))
```

```
alter            I1      dc   = 100u
op
noise            v(vg) vin dec 10 1 1000k 1
destroy
let              unknown.V100u = sqrt(v(onoise_spectrum))
alter            I1      dc   = 1000u
op
noise            v(vg) vin dec 10 1 1000k 1
destroy
let              unknown.V1000u = sqrt(v(onoise_spectrum))
set              pensize =  2
plot  unknown.V10u unknown.V100u unknown.V1000u vs frequency loglog title NMOSNoiseVoltage
echo             "     ... done."
.endcontrol
.end
```

===============END==================================

The intention here is more like a sanity check of an older BiCMOS process. The Actual lab data taken is listed below.

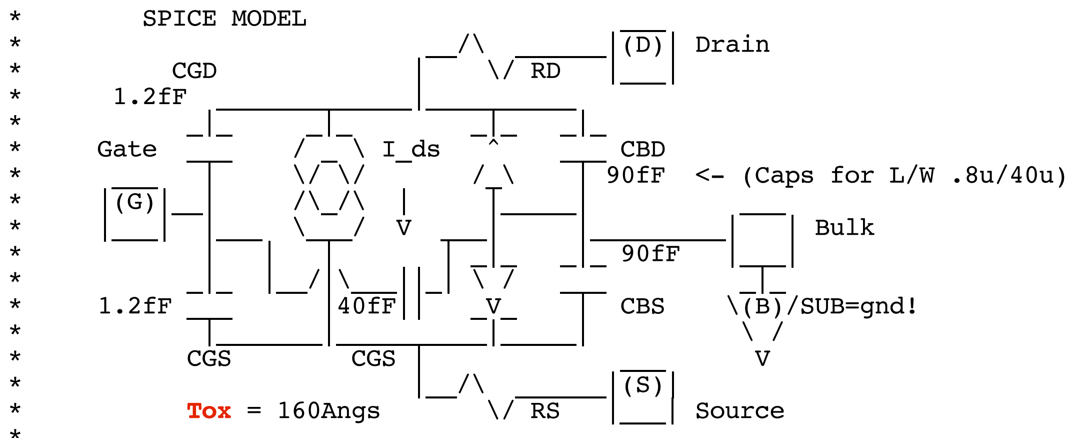



```
*       BiCMOS typical noise    IDS =20uA @3V    tox=160A
*       Hz           nV/rt_Hz       nV/rt_Hz
*       freq         NMOS 40/.8     PMOS 40/.8
*       10              800           150
*       100             400            60
*       1000            150            30
*       10000            50            20
*       100000           10            15
```

However it might be wise to look at the real silicon results with a little more details. Google list the resistivity for glass as being between...

Glass is 10e10 to 10E14 Ohms-m

The geometry the noise was taken off of is shown below.



Using Google's resistivity numbers the resistance of the gate oxide should be...

10Ee10*160E-10/(.8e-6*40e-6) = 5e12 Ohms to 5e16 Ohms

Assume the noise test was done using a 1Volt overdrive at the gate. The you would expect gate leakage to be...

At Vtox = 1V expect .5pA to .05fA

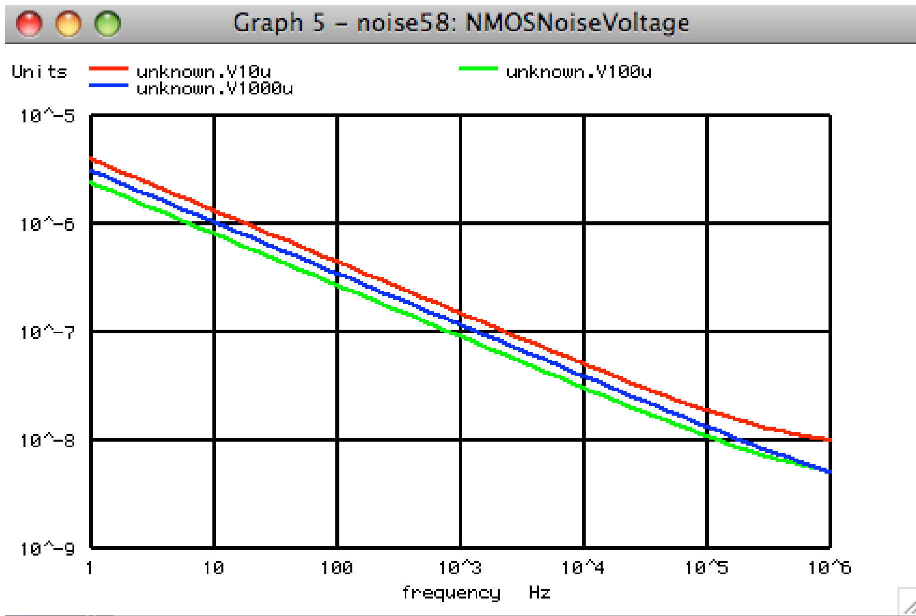
In Terms of electrons that is...

.5pA = 3,125,000 electrons/sec
.05fA = 32.5 electrons/sec

Lets assume only 32.5 electrons/sec. How much does the gate voltage change when only a single electron is added.

1 electron @ 40fF = 4uV

Looking at the simulation (close to real value) numbers, the gate voltage fluctuations appear to be at about the same order of magnitude as a single electron.



Yet Google's data says at best at least 32 electrons are flowing through the gate every second.

But this is for a gate oxide of 160 angstroms.

What happens when the gate oxide is a factor of ten thinner such that tunneling is increasing expotentially with gate voltage?

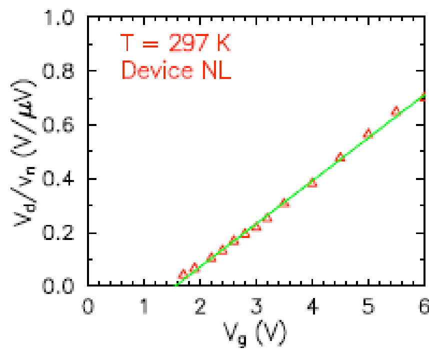


FIG. 6. Graph showing the room-temperature gate-voltage dependence of the 1/f noise for n-channel device NL, typical of that found for n-MOS devices. The symbols are data and the line is a least-squares fit to the data.

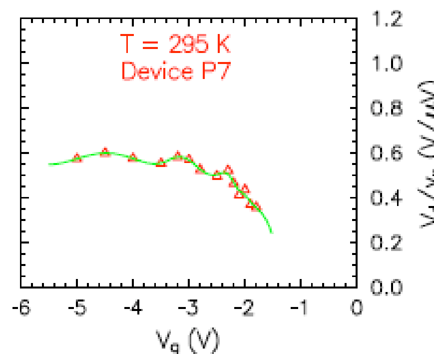


FIG. 7. Graph showing the room-temperature gate-voltage dependence of the 1/f noise for p-channel device P7. The symbols are data and the curve is a guide to the eye.

Some papers on 1/f noise for CMOS transistors have the 1/f noise changing or not changing as a function of gate voltage.

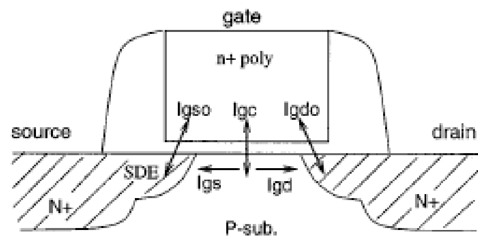


Fig. 1. Illustration of gate direct tunneling components of a very short-channel NMOSFET (I_{gso} and I_{gdo}) are EDT currents.

With smaller geometries come smaller gate oxides. Now tunneling is looking like such...

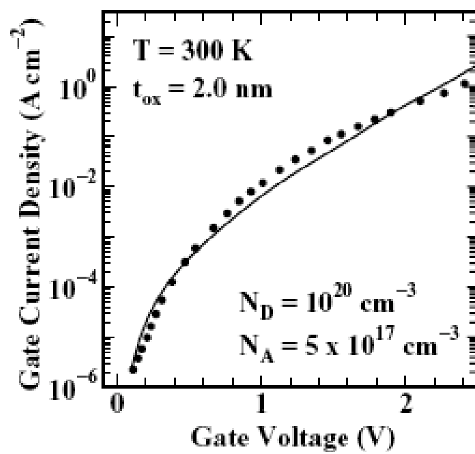


Figure 2: Calculated tunneling current density as a function of gate voltage in a poly-Si-gate capacitor (solid line). Closed circles show the experimental results reported in Ref. [3].

Do a little math with a 40u by 0.8u geometry.

(40e-6)(.8e-6)= 32e-12m^2 => 32e-8cm^2
@ 1V Gate current = (1e-2A/cm^2)*32e-8cm^2= 3.2nA
@ 1V 160A expecting Gate current .5pA to .05fA

And changes in the oxide thickness may be changing the tunneling current by orders of magnitude.

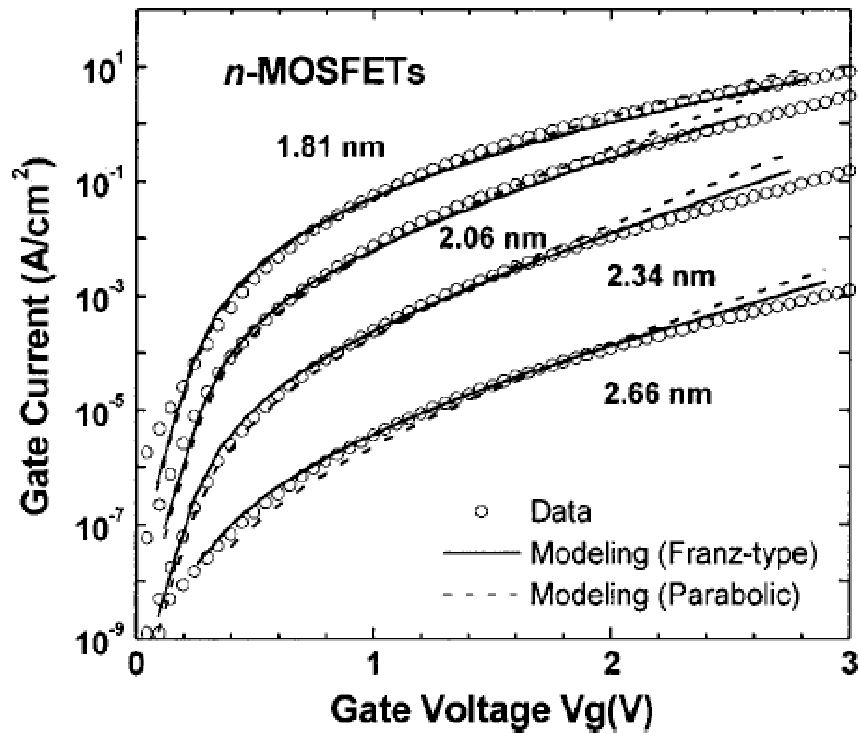


FIG. 5. The electron direct tunneling currents in n-MOSFETs. The open circles are the measurements. The solid and dashed lines are the calculations by assuming the electron dispersion in SiO_2 band gap to be Franz type ($m_{ox}=0.61m_0$) and parabolic ($m_{ox}=0.50m_0$), respectively (see Refs. 6 and 7).

Naturally this looks like it is encouraging some on going model developement. A paper titled "New 1/f noise model in MOS Model 9, level 903" by A.J. Scholten and D.B.M. Klaassen is an example of that effort.

www.nxp.com/acrobat_download/other/models/noise903.pdf

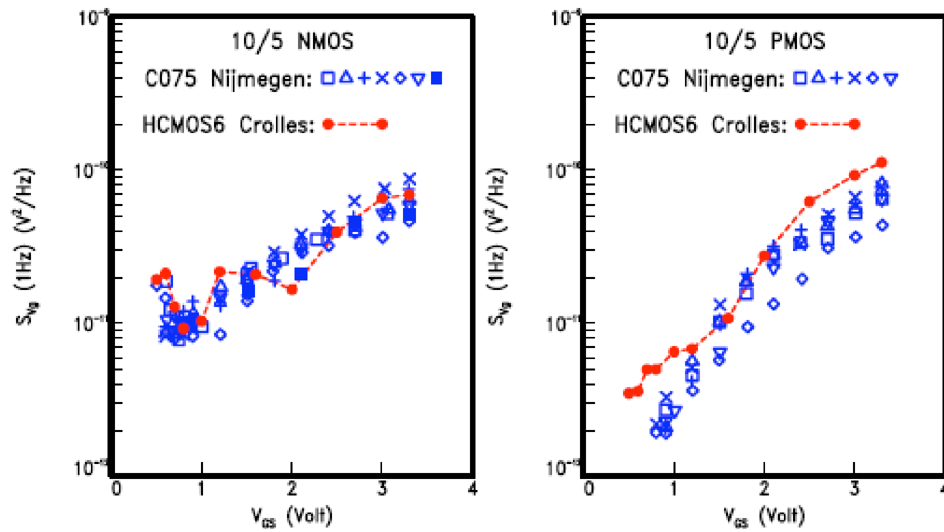


Figure 11: *Left:* Input-referred voltage noise in saturation ($V_{\mathrm{DS}} = 3.3$ V) as a function of gate-source voltage for various, nominally identical, 10/5 n-channel devices processed in C075. The measurements are compared with a measurement from HCMOS6 in Crolles. *Right:* Same, but now for a series of 10/5 p-channel devices.