more links at end

US006965338B2

(12) **United States Patent**
**Irie et al.**

(10) **Patent No.: US 6,965,338 B2**
(45) **Date of Patent: Nov. 15, 2005**

(54) **CASCADE A/D CONVERTER**

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(73) Assignee: **Yokogawa Electric Corporation**, Tokyo (JP)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/991,497**

(22) Filed: **Nov. 19, 2004**

(65) **Prior Publication Data**

US 2005/0162300 A1 Jul. 28, 2005

(30) **Foreign Application Priority Data**

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Jul. 15, 2004 (JP) ..... 2004-208528

(51) **Int. Cl.**[7] ..... **H03M 1/38**
(52) **U.S. Cl.** ..... **341/161**; 341/155
(58) **Field of Search** ..... 341/155, 141, 341/51, 110, 157, 166, 151; 704/213, 211; 370/268; 360/32, 48; 365/45

(56) **References Cited**

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* cited by examiner

*Primary Examiner*—Brian Young
(74) *Attorney, Agent, or Firm*—Westerman, Hattori, Daniels & Adrian, LLP

(57) **ABSTRACT**

A cascade A/D converter that has shorter settling time and enables high-speed operation is provided. A cascade A/D converter comprises fundamental constituent elements cascaded in plural stages, each fundamental constituent element comprising a first comparator for inputting an analog input signal, a D/A converter for converting an output of the first comparator to an analog signal again, and a subtractor for subtracting an output of the D/A converter from the analog input signal, the fundamental constituent elements comprising: a second comparator for inputting the analog input signal every least significant bit near a transition point of the first comparator; and an arithmetic operating unit for generating upper bits based on an output of the first comparator and interpolating lower bits based on an output of the second comparator.

**13 Claims, 18 Drawing Sheets**

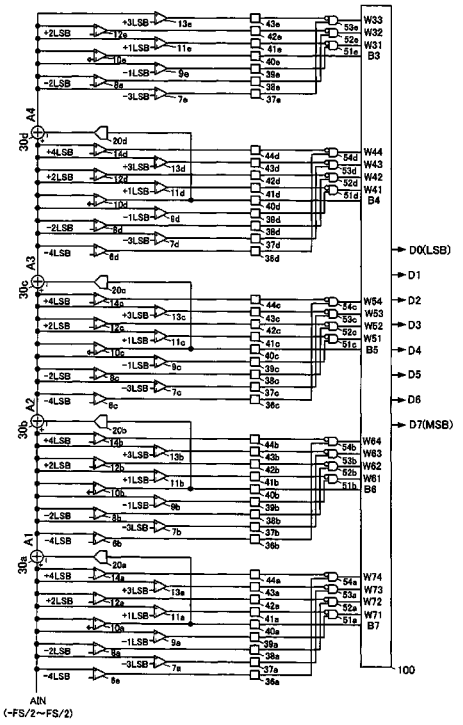


FIG. 1
Prior Art

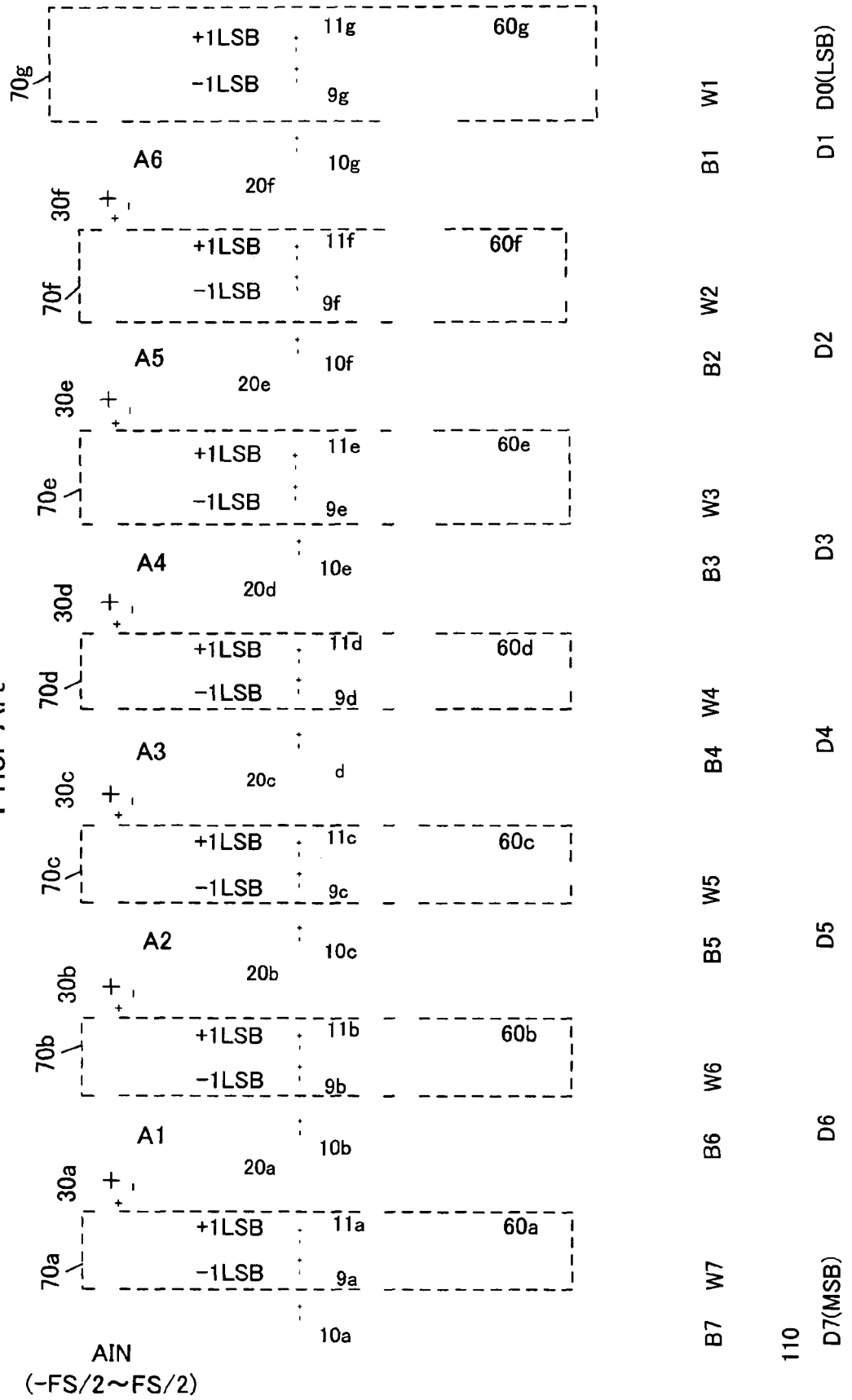


FIG. 2

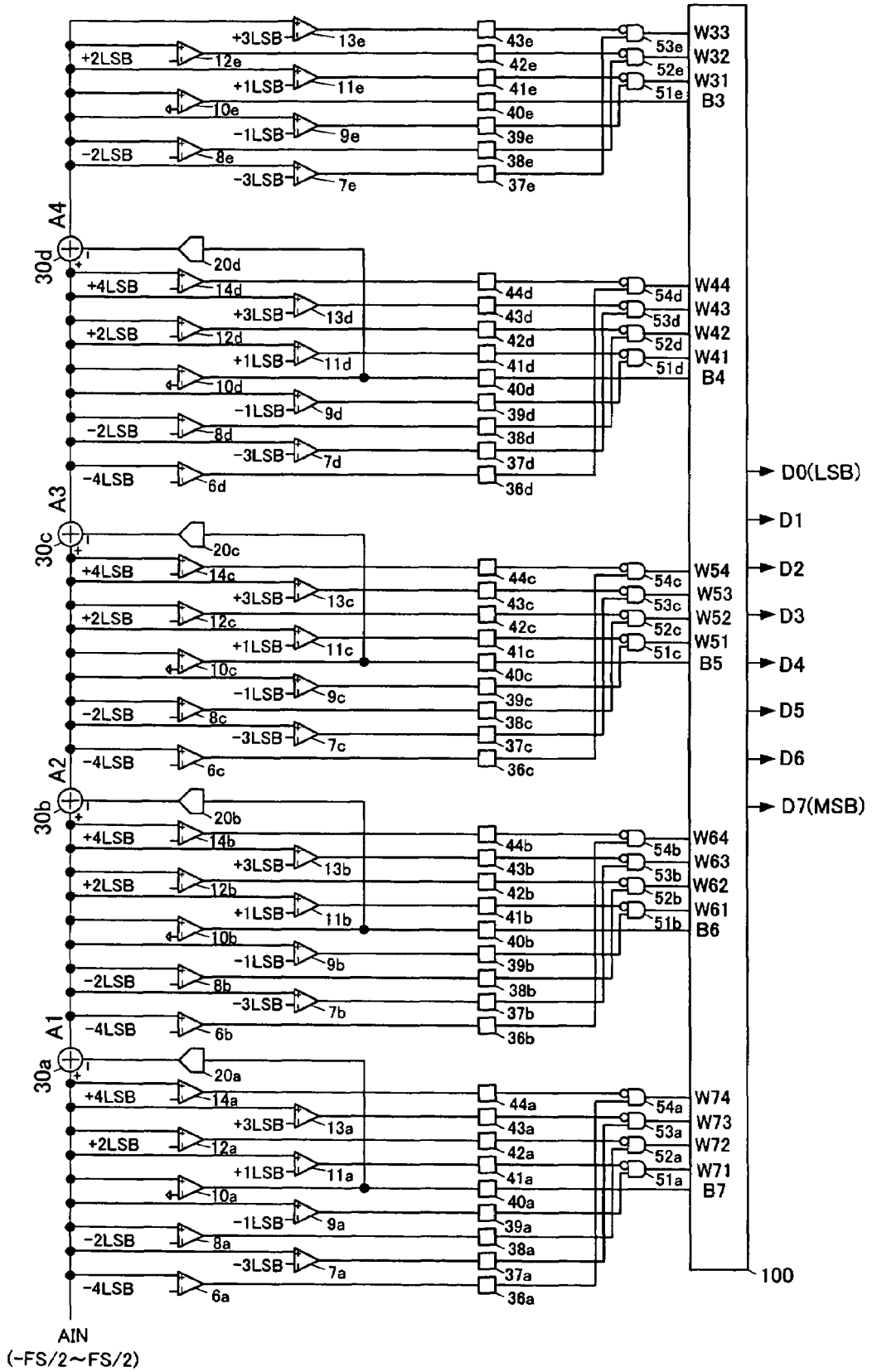

+3LSB
13e
+2LSB
12e
+1LSB
11e
10e
-1LSB
9e
-2LSB
8e
-3LSB
7e
43e
42e
41e
40e
39e
38e
37e
53e
52e
51e
W33
W32
W31
B3
A4
30d
20d
+4LSB
14d
+3LSB
13d
+2LSB
12d
+1LSB
11d
10d
-1LSB
9d
-2LSB
8d
-3LSB
7d
-4LSB
6d
44d
43d
42d
41d
40d
39d
38d
37d
36d
54d
53d
52d
51d
W44
W43
W42
W41
B4
A3
30c
20c
+4LSB
14c
+3LSB
13c
+2LSB
12c
+1LSB
11c
10c
-1LSB
9c
-2LSB
8c
-3LSB
7c
-4LSB
6c
44c
43c
42c
41c
40c
39c
38c
37c
36c
54c
53c
52c
51c
W54
W53
W52
W51
B5
A2
30b
20b
+4LSB
14b
+3LSB
13b
+2LSB
12b
+1LSB
11b
10b
-1LSB
9b
-2LSB
8b
-3LSB
7b
-4LSB
6b
44b
43b
42b
41b
40b
39b
38b
37b
36b
54b
53b
52b
51b
W64
W63
W62
W61
B6
A1
30a
20a
+4LSB
14a
+3LSB
13a
+2LSB
12a
+1LSB
11a
10a
-1LSB
9a
-2LSB
8a
-3LSB
7a
-4LSB
6a
44a
43a
42a
41a
40a
39a
38a
37a
36a
54a
53a
52a
51a
W74
W73
W72
W71
B7
D0(LSB)
D1
D2
D3
D4
D5
D6
D7(MSB)
100
AIN
(-FS/2~FS/2)

FIG. 3

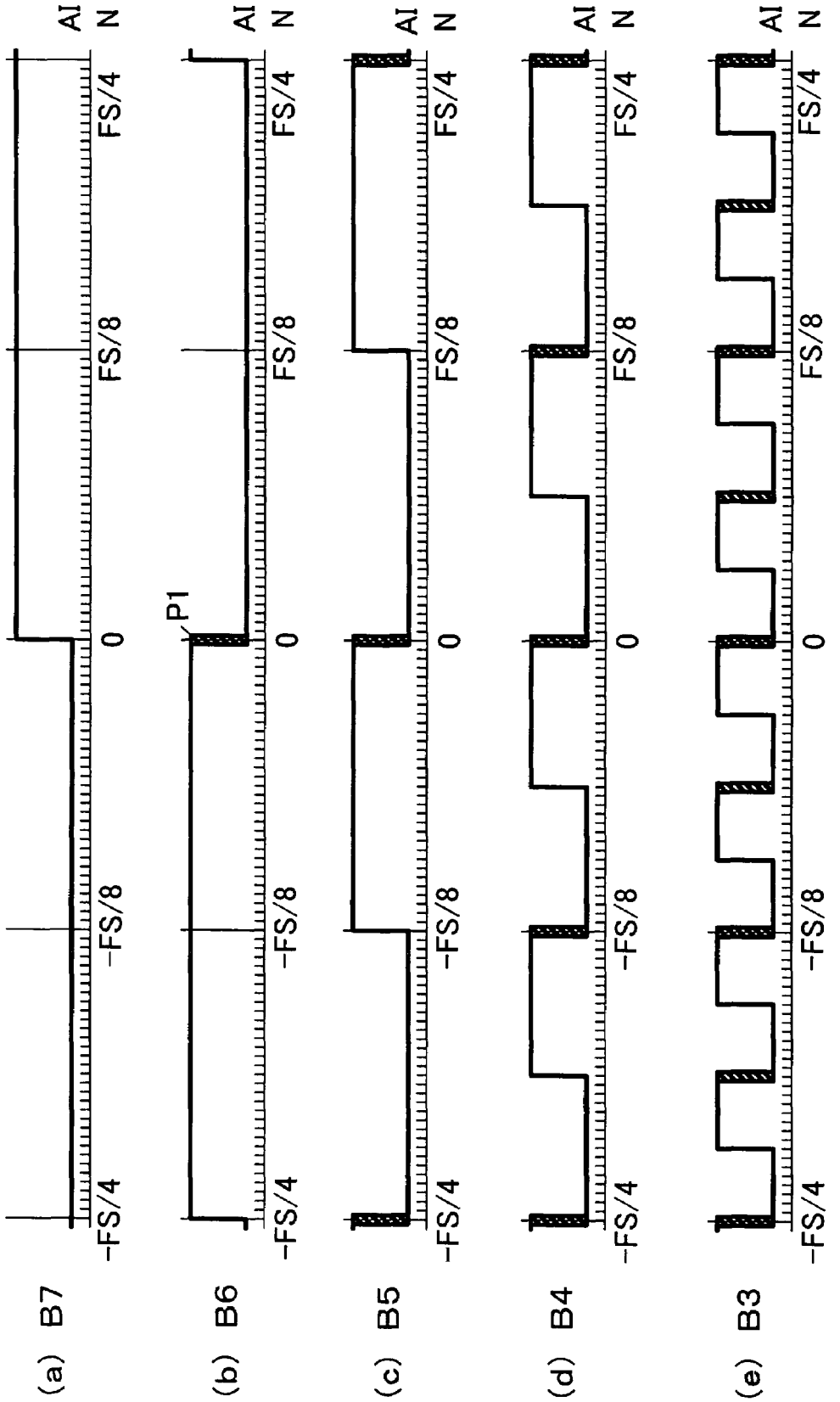
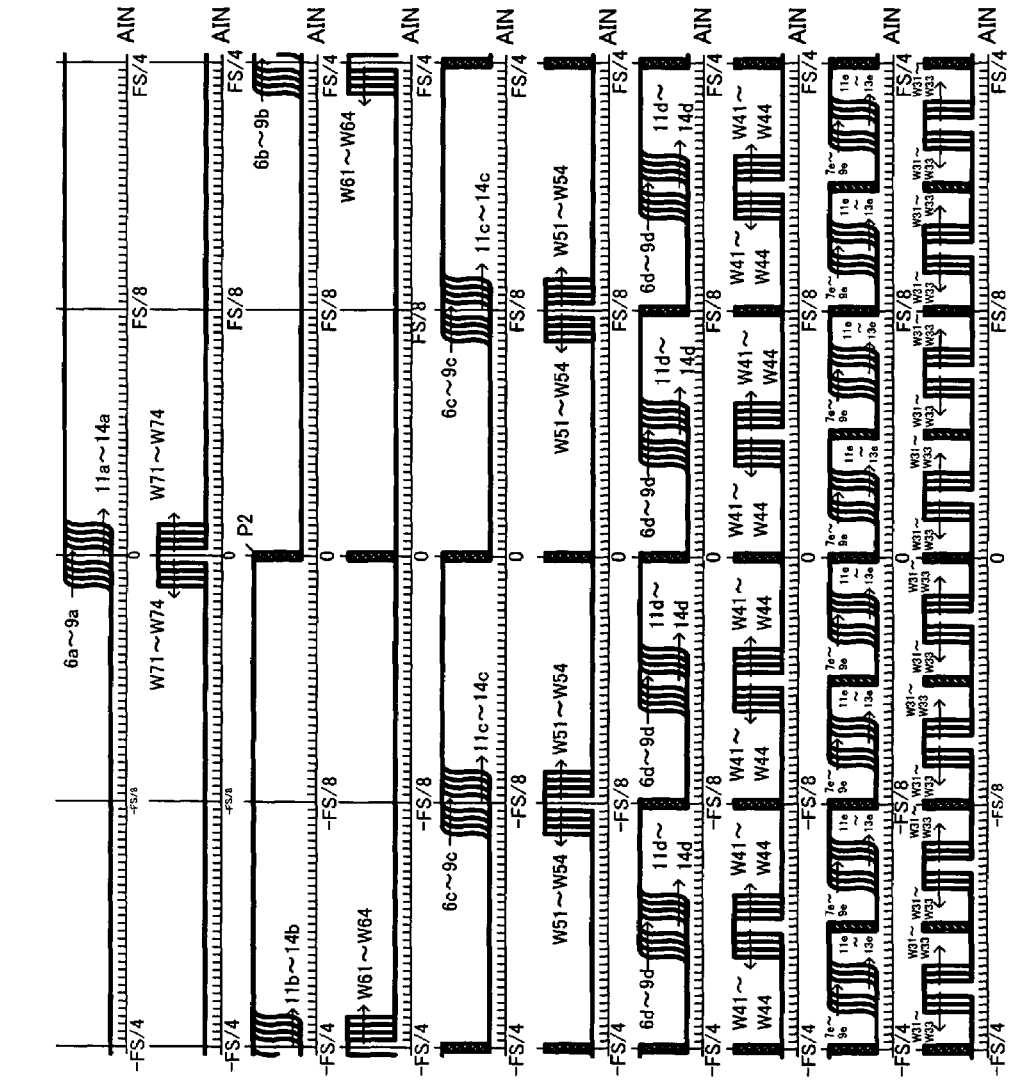


FIG. 4


(a)
(b) W71~W74
(c)
(d) W61~W64
(e)
(f) W51~W54
(g)
(h) W41~W44
(i)
(j) W31~W33
AIN
FS/4
FS/8
0
-FS/4
-FS/8
6a~9a
11a~14a
W71~W74
P2
6b~9b
11b~14b
W61~W64
6c~9c
11c~14c
W51~W54
6d~9d
11d~14d
W41~W44
7e~9e
11e~13e
W31~W33

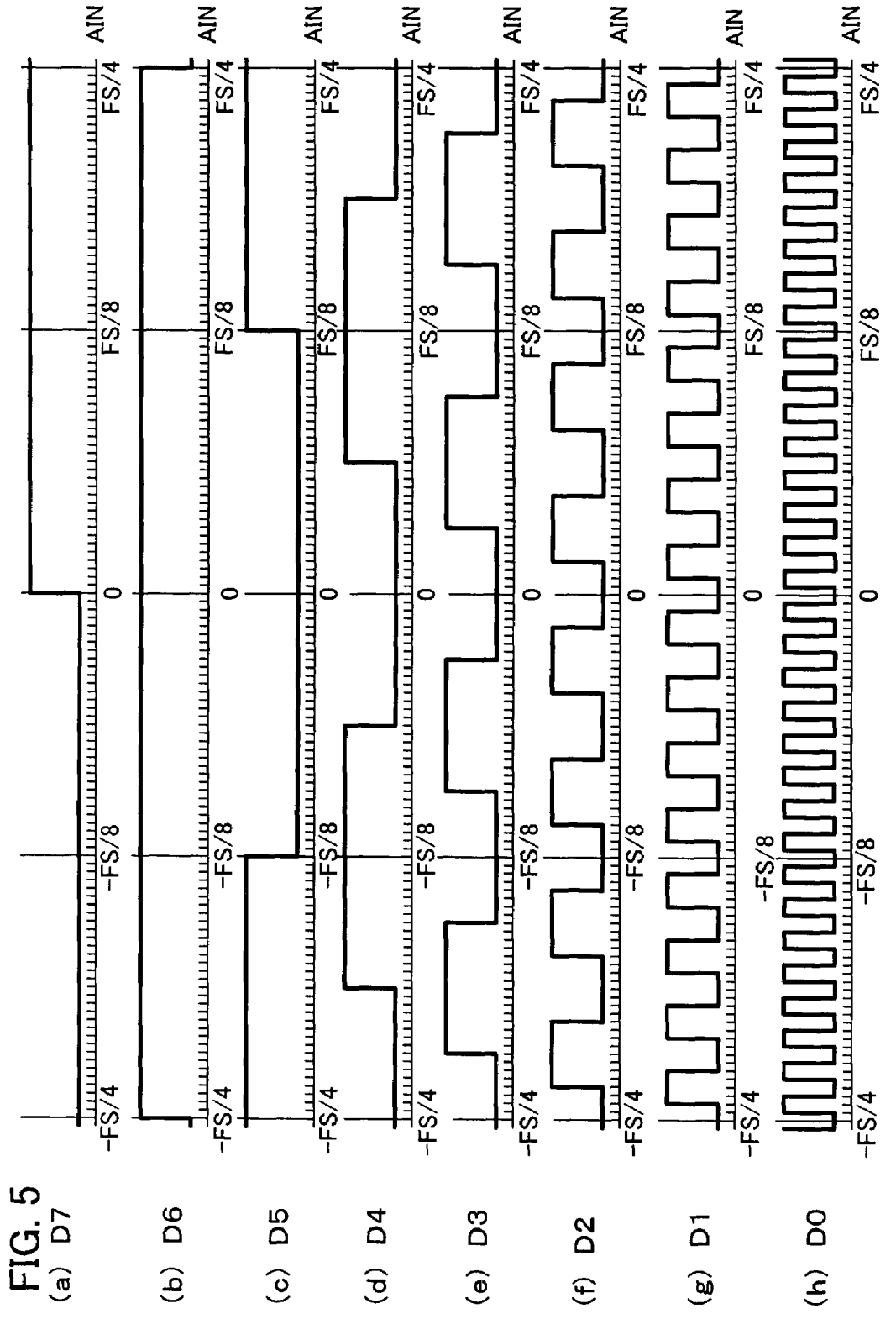



FIG. 5

FIG. 6

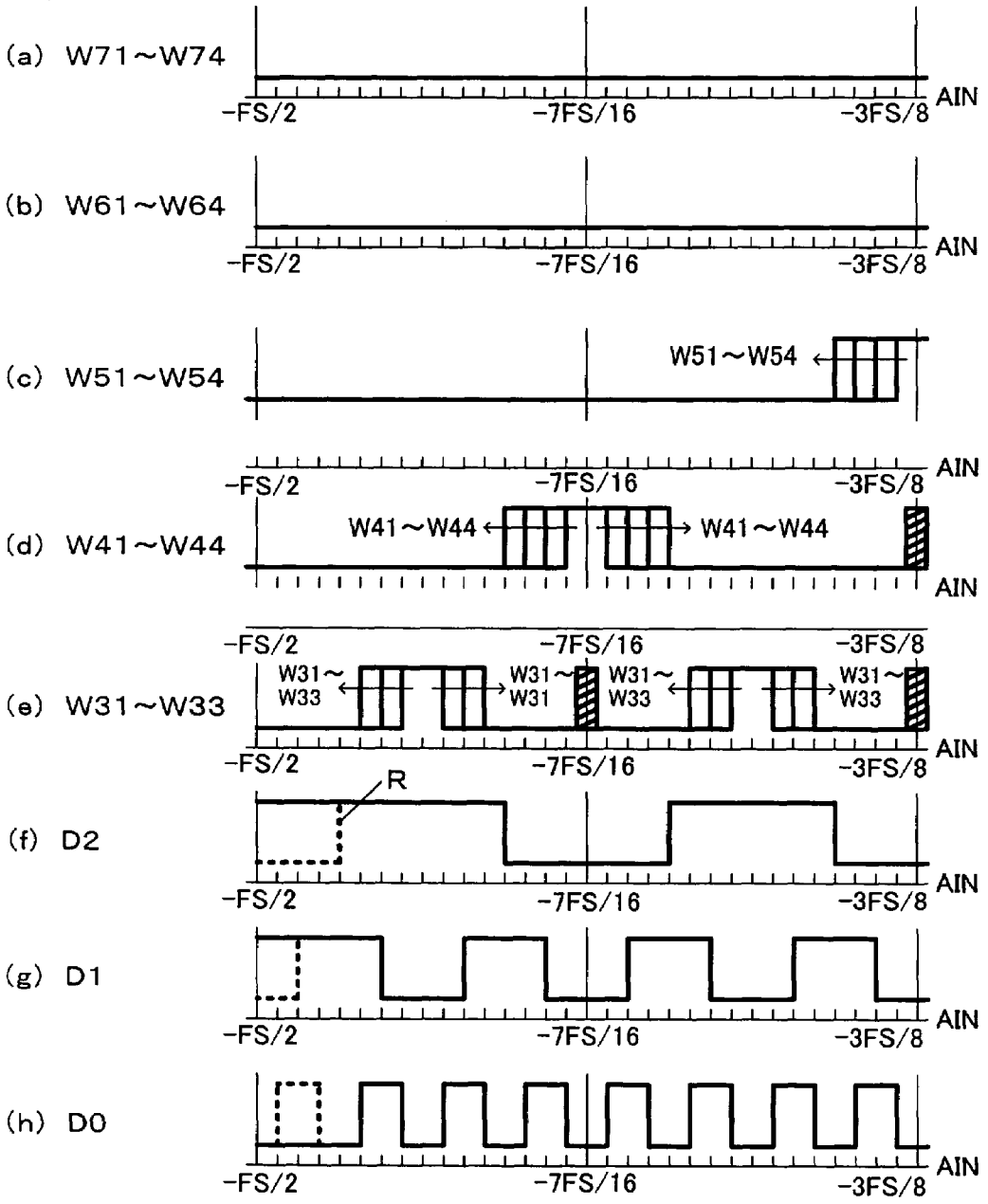

(a) W71~W74
(b) W61~W64
(c) W51~W54
(d) W41~W44
(e) W31~W33
(f) D2
(g) D1
(h) D0
-FS/2
-7FS/16
-3FS/8
AIN
W51~W54
W41~W44
W31~
W33
W31~
W31
R

FIG. 7

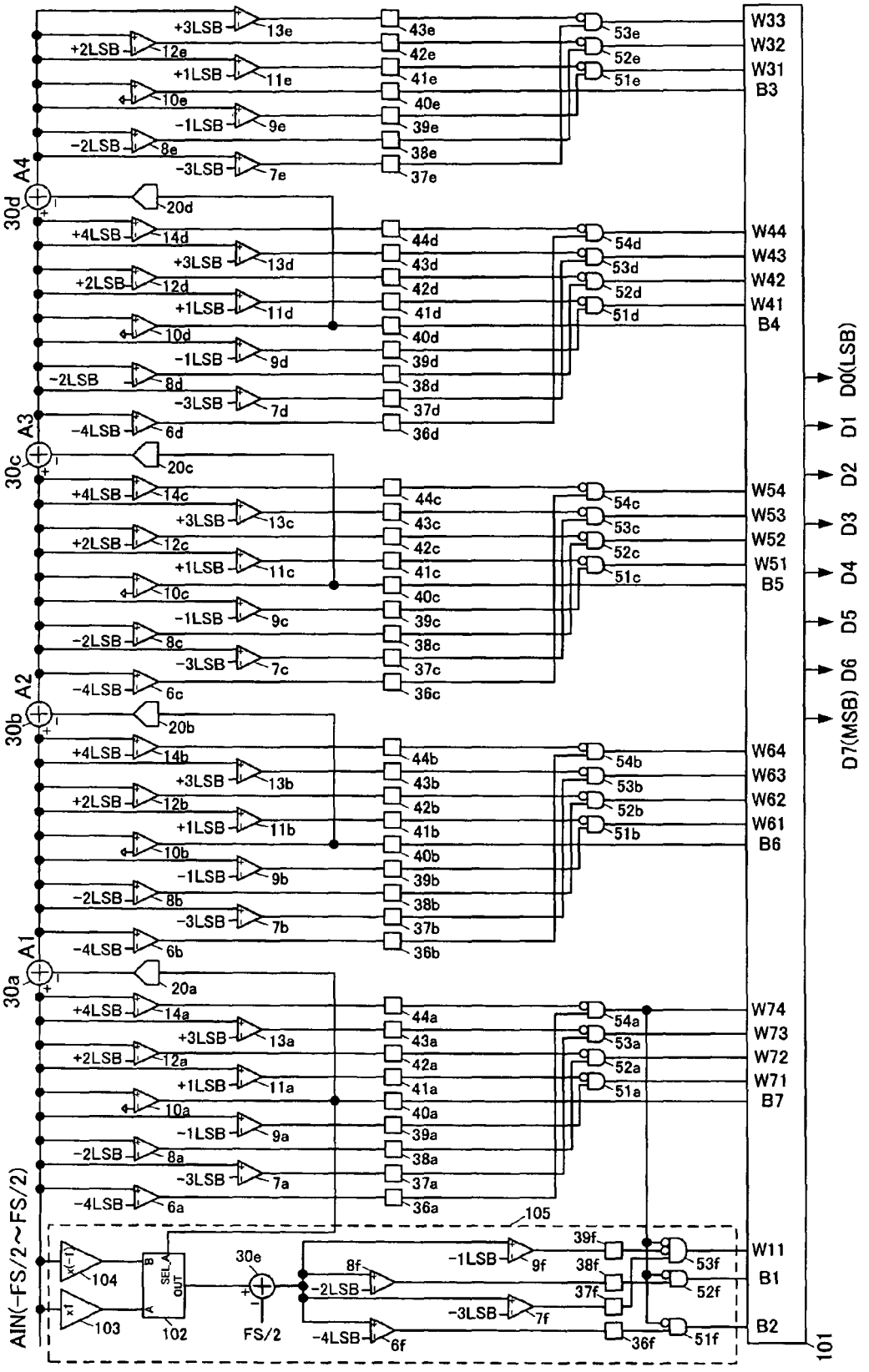

AIN(-FS/2~FS/2)
A4
A3
A2
A1
30d
30c
30b
30a
+3LSB
+2LSB
+1LSB
-1LSB
-2LSB
-3LSB
+4LSB
-4LSB
13e
12e
11e
10e
9e
8e
7e
20d
14d
13d
12d
11d
10d
9d
8d
7d
6d
20c
14c
13c
12c
11c
10c
9c
8c
7c
6c
20b
14b
13b
12b
11b
10b
9b
8b
7b
6b
20a
14a
13a
12a
11a
10a
9a
8a
7a
6a
43e
42e
41e
40e
39e
38e
37e
44d
43d
42d
41d
40d
39d
38d
37d
36d
44c
43c
42c
41c
40c
39c
38c
37c
36c
44b
43b
42b
41b
40b
39b
38b
37b
36b
44a
43a
42a
41a
40a
39a
38a
37a
36a
53e
52e
51e
54d
53d
52d
51d
54c
53c
52c
51c
54b
53b
52b
51b
54a
53a
52a
51a
W33
W32
W31
B3
W44
W43
W42
W41
B4
W54
W53
W52
W51
B5
W64
W63
W62
W61
B6
W74
W73
W72
W71
B7
105
39f
38f
37f
36f
-1LSB
-2LSB
-3LSB
-4LSB
9f
8f
7f
6f
53f
52f
51f
W11
B1
B2
101
D0(LSB)
D1
D2
D3
D4
D5
D6
D7(MSB)
104
103
102
SEL
OUT
30e
FS/2

FIG. 8

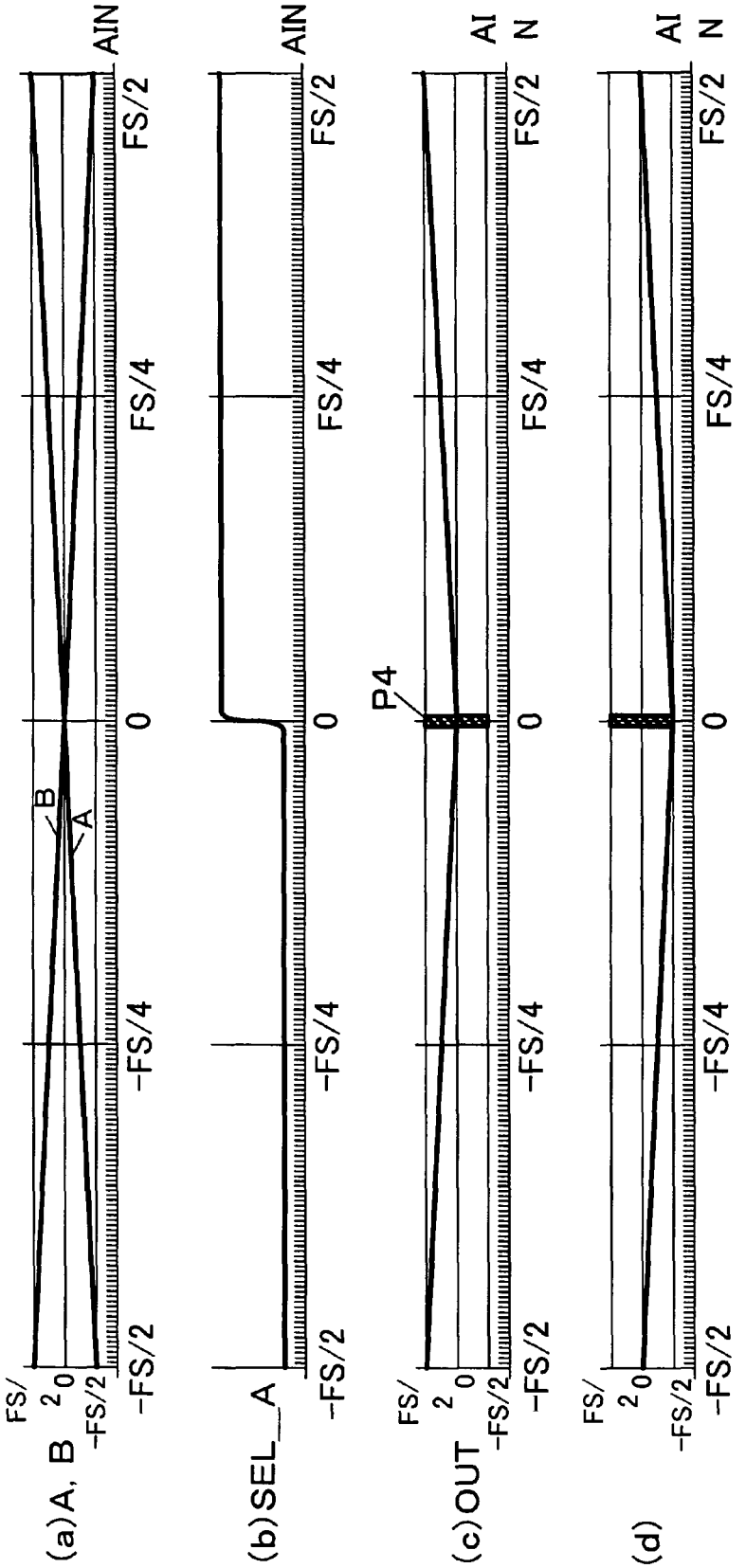


FIG. 9

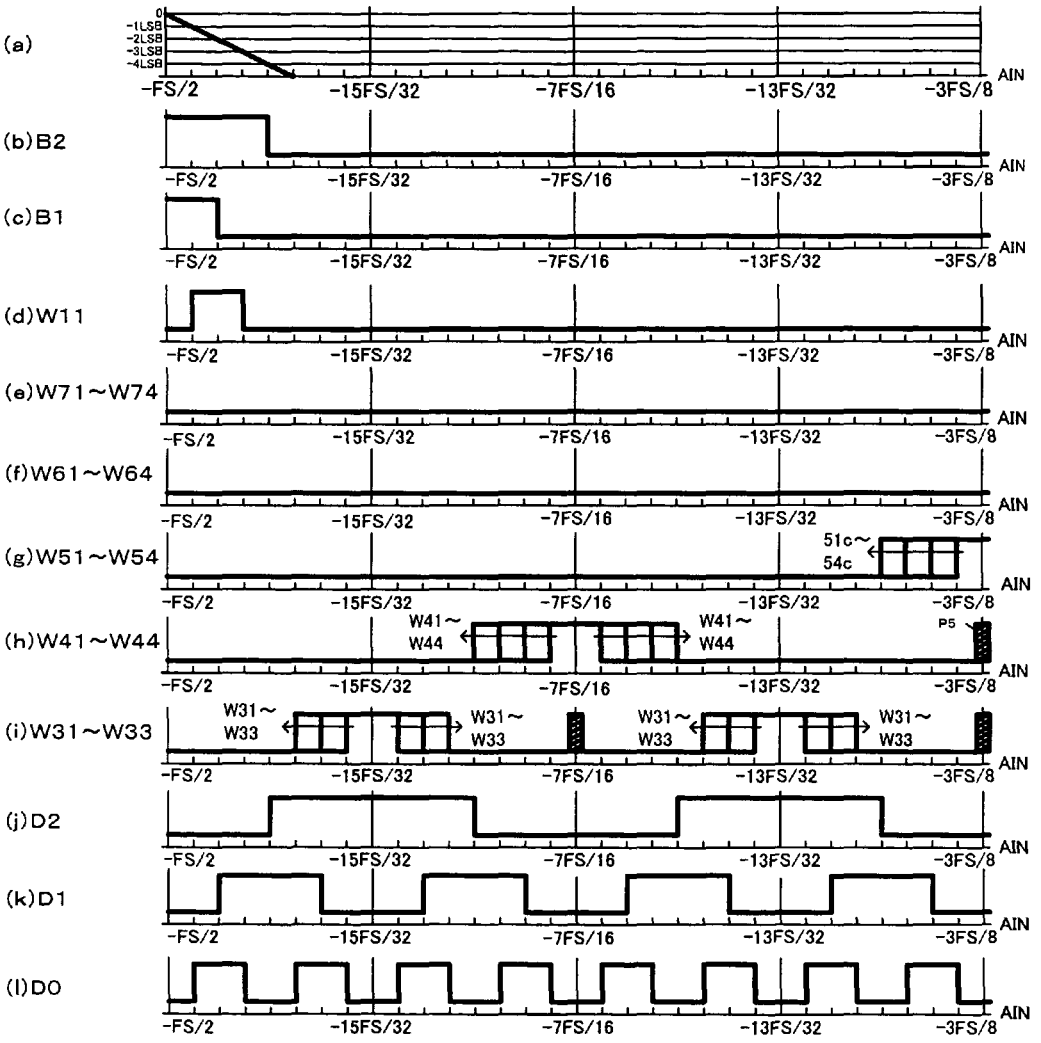

(a)
0
-1LSB
-2LSB
-3LSB
-4LSB
-FS/2
-15FS/32
-7FS/16
-13FS/32
-3FS/8
AIN
(b)B2
(c)B1
(d)W11
(e)W71~W74
(f)W61~W64
(g)W51~W54
51c~
54c
(h)W41~W44
W41~
W44
P5
(i)W31~W33
W31~
W33
(j)D2
(k)D1
(l)D0

FIG. 10

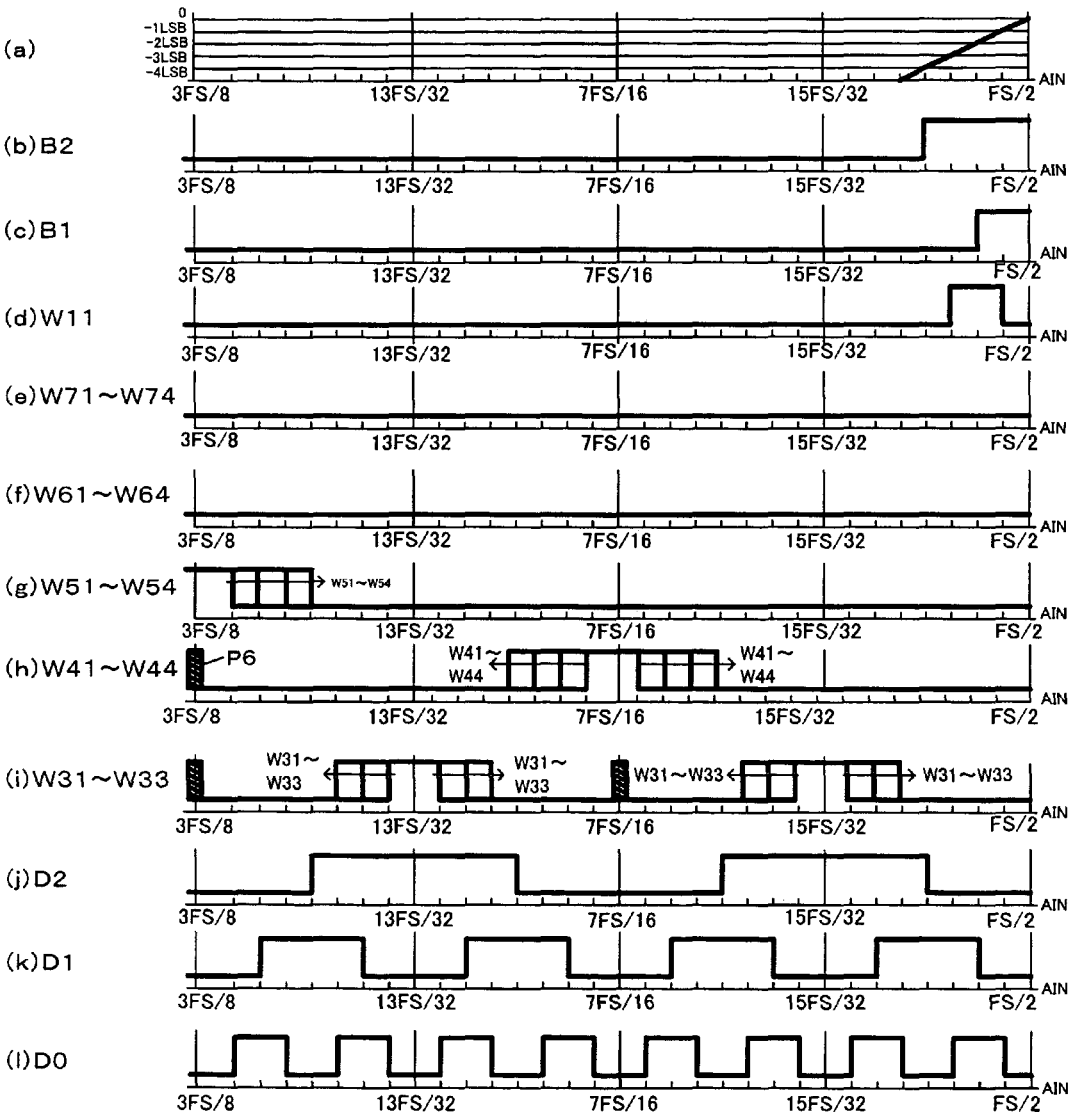

(a)
0
-1LSB
-2LSB
-3LSB
-4LSB
3FS/8
13FS/32
7FS/16
15FS/32
FS/2
AIN
(b)B2
(c)B1
(d)W11
(e)W71~W74
(f)W61~W64
(g)W51~W54
W51~W54
(h)W41~W44
P6
W41~
W44
(i)W31~W33
W31~
W33
W31~W33
(j)D2
(k)D1
(l)D0

FIG. 11

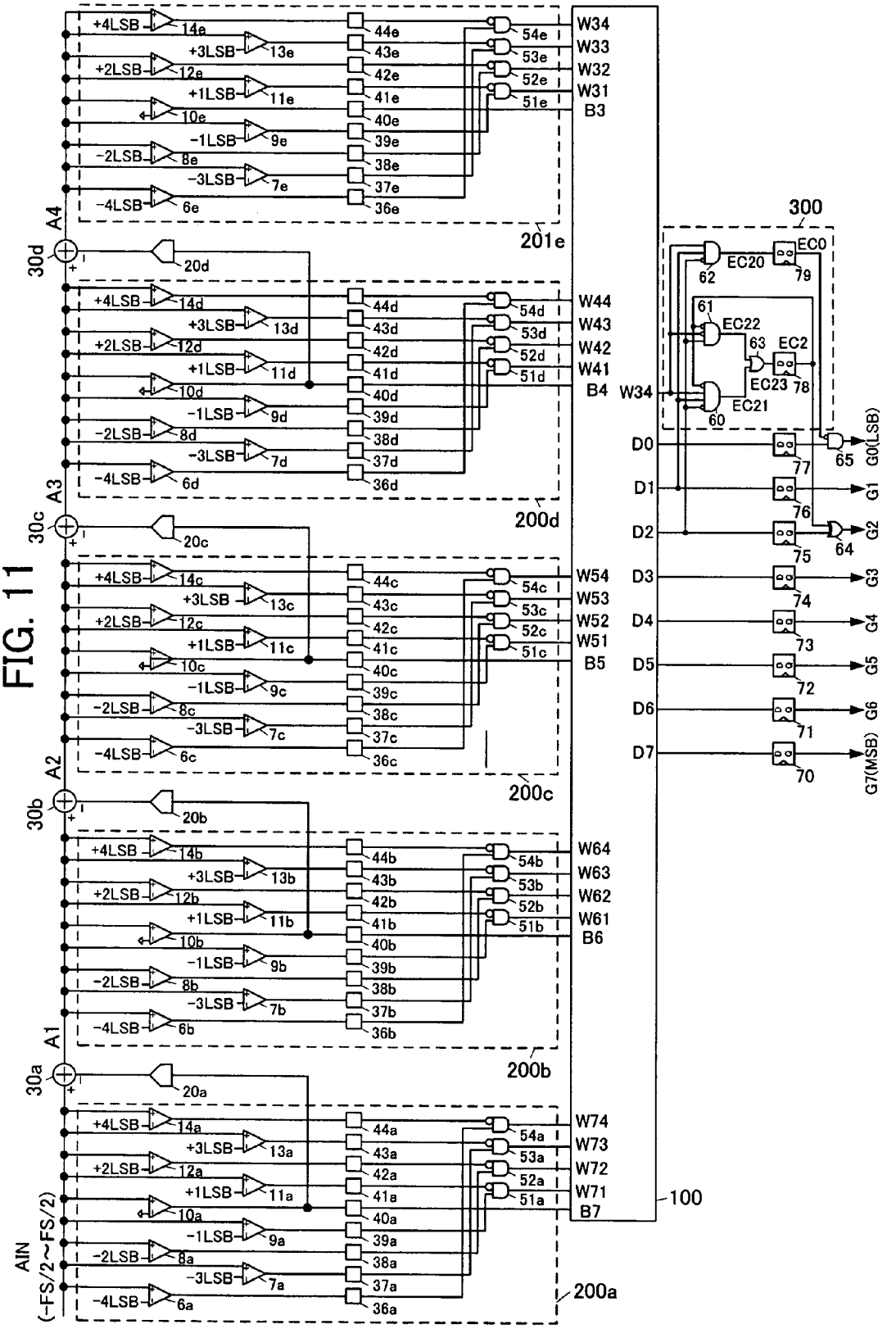

AIN
(-FS/2~FS/2)
A4
A3
A2
A1
30d
30c
30b
30a
20d
20c
20b
20a
+4LSB
+3LSB
+2LSB
+1LSB
-1LSB
-2LSB
-3LSB
-4LSB
14e
13e
12e
11e
10e
9e
8e
7e
6e
14d
13d
12d
11d
10d
9d
8d
7d
6d
14c
13c
12c
11c
10c
9c
8c
7c
6c
14b
13b
12b
11b
10b
9b
8b
7b
6b
14a
13a
12a
11a
10a
9a
8a
7a
6a
44e
43e
42e
41e
40e
39e
38e
37e
36e
44d
43d
42d
41d
40d
39d
38d
37d
36d
44c
43c
42c
41c
40c
39c
38c
37c
36c
44b
43b
42b
41b
40b
39b
38b
37b
36b
44a
43a
42a
41a
40a
39a
38a
37a
36a
54e
53e
52e
51e
54d
53d
52d
51d
54c
53c
52c
51c
54b
53b
52b
51b
54a
53a
52a
51a
W34
W33
W32
W31
B3
W44
W43
W42
W41
B4
W54
W53
W52
W51
B5
W64
W63
W62
W61
B6
W74
W73
W72
W71
B7
201e
200d
200c
200b
200a
100
300
EC0
EC20
EC22
EC2
EC23
EC21
62
79
61
63
78
60
W34
D0
D1
D2
D3
D4
D5
D6
D7
77
76
75
74
73
72
71
70
65
64
G0(LSB)
G1
G2
G3
G4
G5
G6
G7(MSB)

FIG. 12

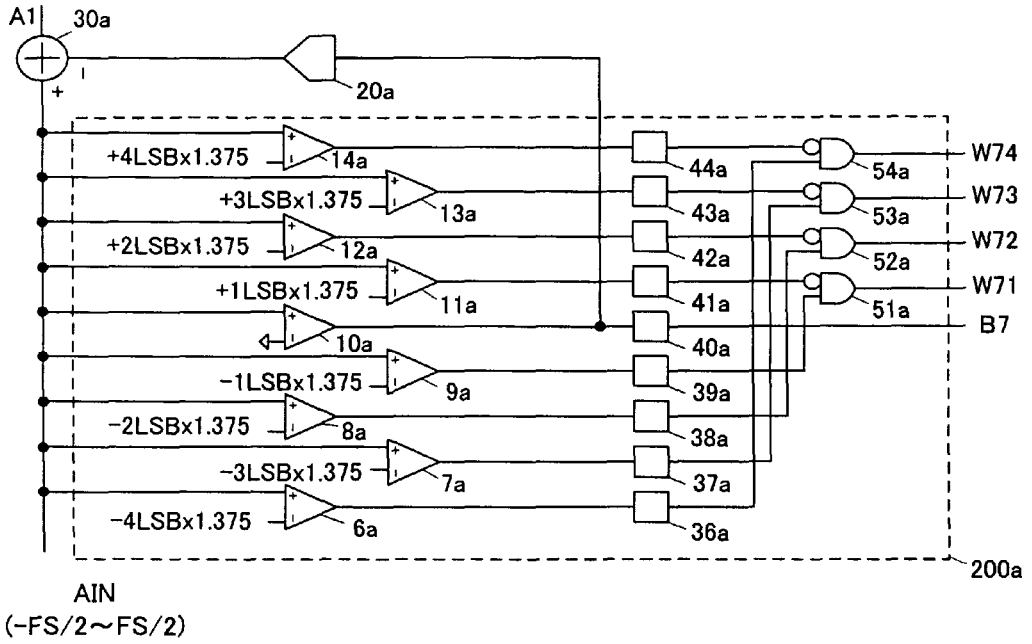

A1
30a
20a
+4LSBx1.375
14a
+3LSBx1.375
13a
+2LSBx1.375
12a
+1LSBx1.375
11a
10a
-1LSBx1.375
9a
-2LSBx1.375
8a
-3LSBx1.375
7a
-4LSBx1.375
6a
44a
43a
42a
41a
40a
39a
38a
37a
36a
54a
53a
52a
51a
W74
W73
W72
W71
B7
200a
AIN
(-FS/2~FS/2)

FIG. 13

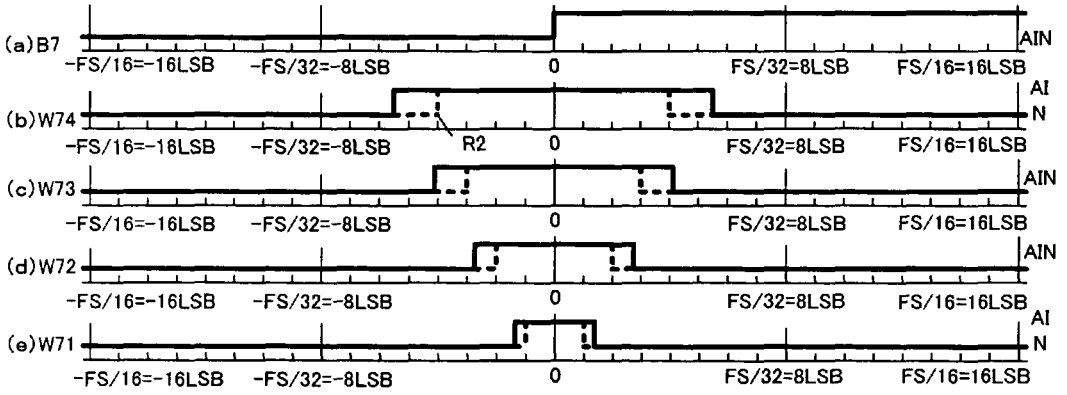

(a)B7
AIN
-FS/16=-16LSB
-FS/32=-8LSB
0
FS/32=8LSB
FS/16=16LSB
(b)W74
R2
(c)W73
(d)W72
(e)W71

FIG. 14

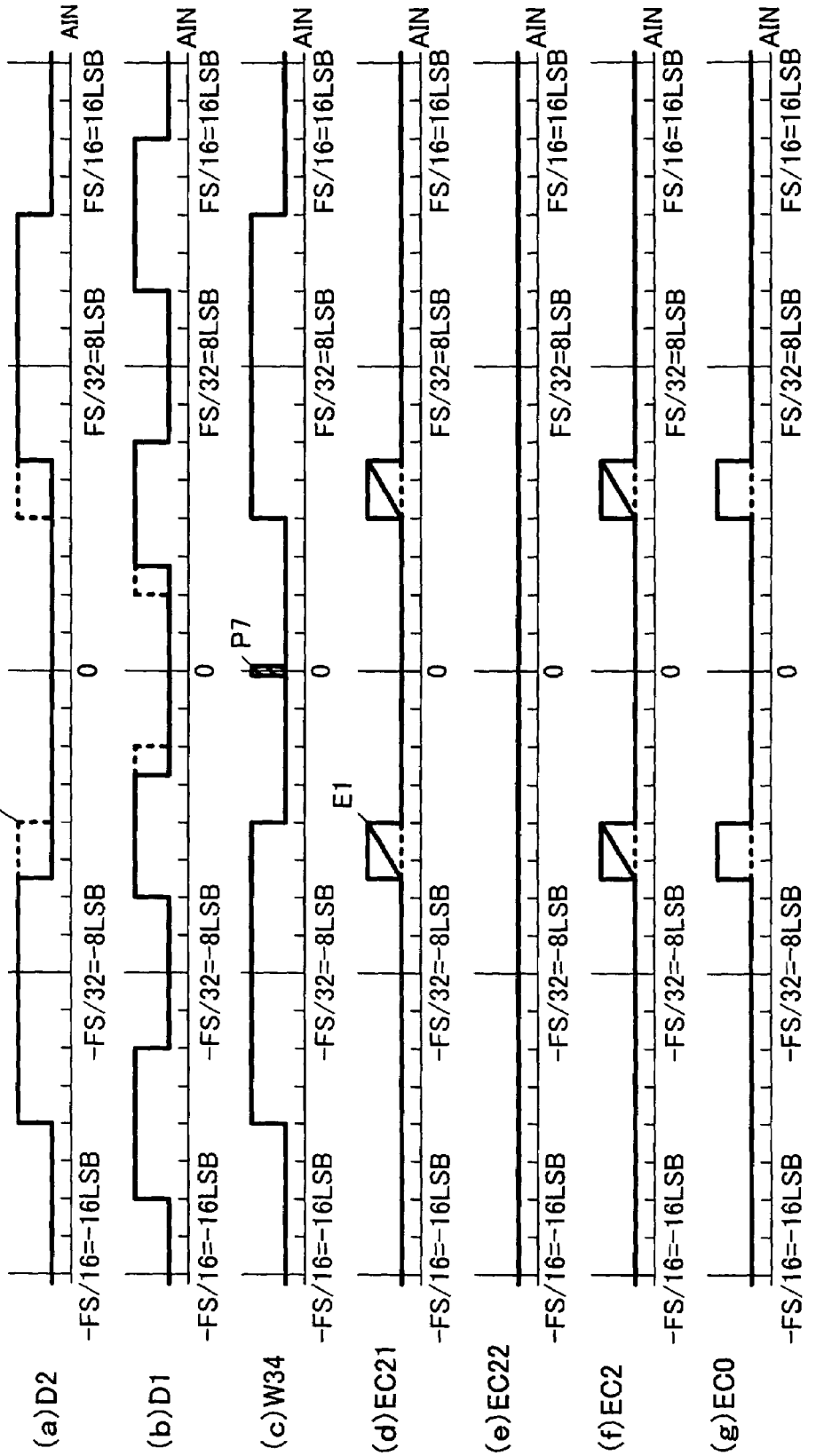

(a)D2
(b)D1
(c)W34
(d)EC21
(e)EC22
(f)EC2
(g)EC0
AIN
-FS/16=-16LSB
-FS/32=-8LSB
0
FS/32=8LSB
FS/16=16LSB
R3
E1
P7

FIG. 15

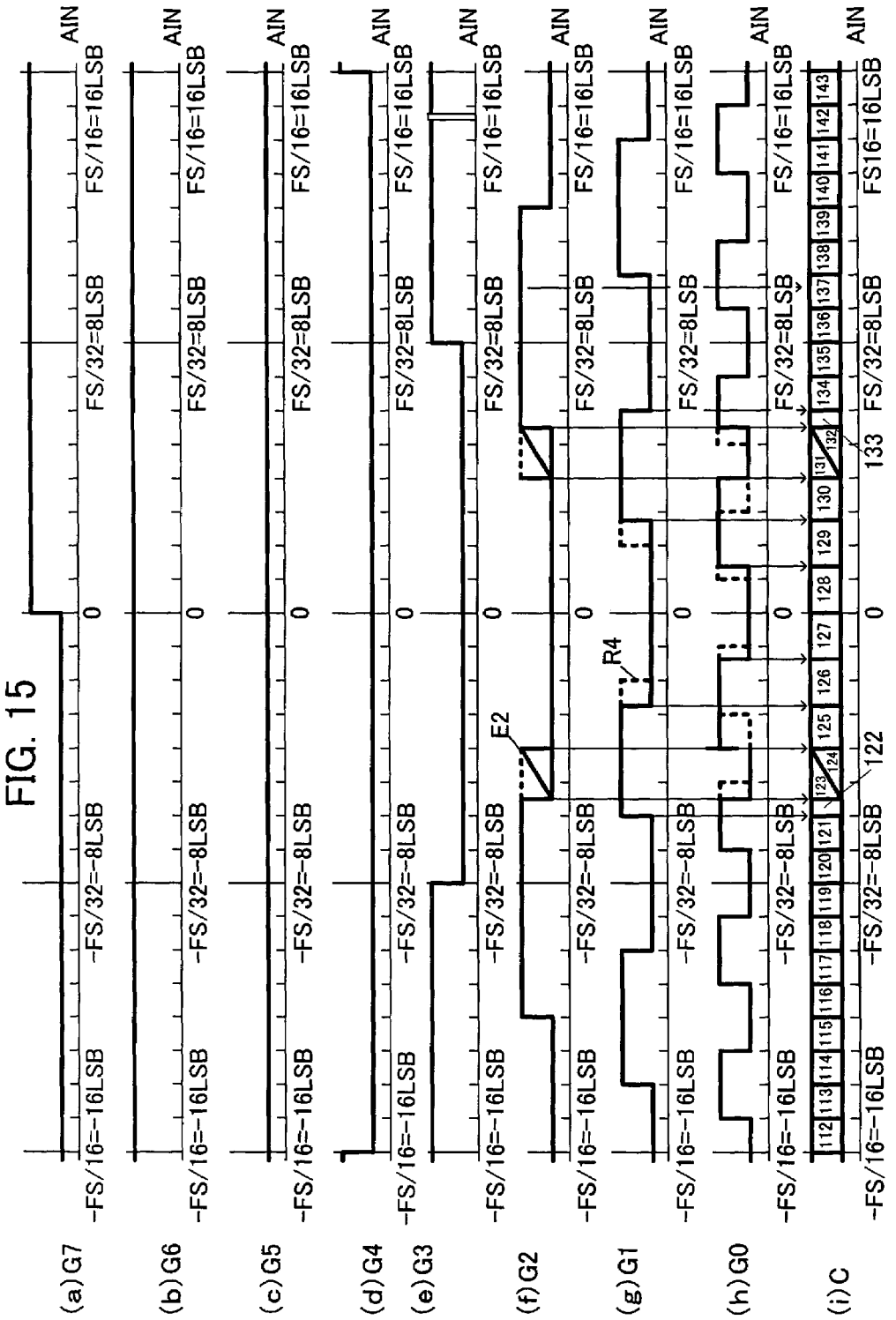

(a) G7
(b) G6
(c) G5
(d) G4
(e) G3
(f) G2
(g) G1
(h) G0
(i) C
AIN
-FS/16=-16LSB
-FS/32=-8LSB
0
FS/32=8LSB
FS/16=16LSB
E2
R4
122
133
112 113 114 115 116 117 118 119 120 121 123 124 125 126 127 128 129 130 131 132 134 135 136 137 138 139 140 141 142 143

FIG. 16

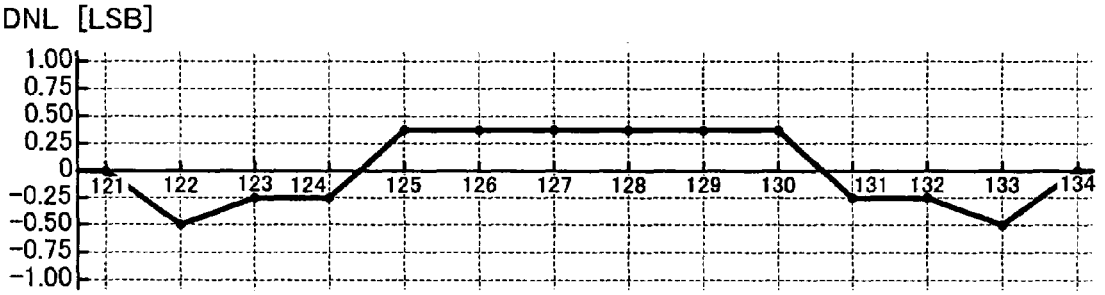

DNL [LSB]
1.00
0.75
0.50
0.25
0
-0.25
-0.50
-0.75
-1.00
121
122
123
124
125
126
127
128
129
130
131
132
133
134

FIG. 21

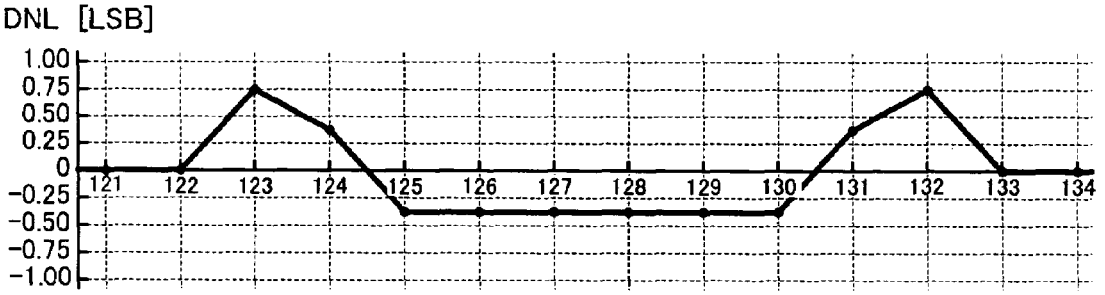

DNL [LSB]
1.00
0.75
0.50
0.25
0
-0.25
-0.50
-0.75
-1.00
121
122
123
124
125
126
127
128
129
130
131
132
133
134

FIG. 17

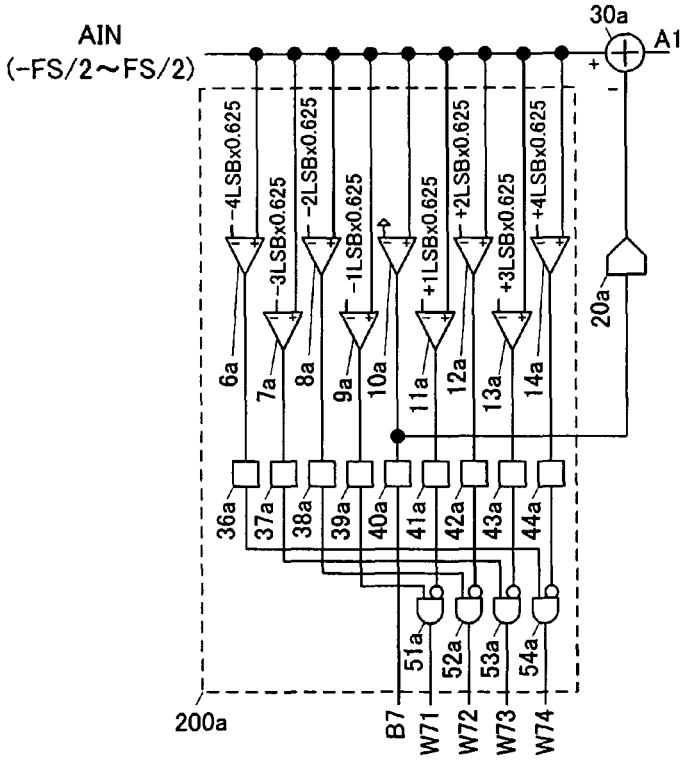

AIN
(-FS/2~FS/2)
30a
A1
+
-
-4LSBx0.625
-3LSBx0.625
-2LSBx0.625
-1LSBx0.625
+1LSBx0.625
+2LSBx0.625
+3LSBx0.625
+4LSBx0.625
20a
6a
7a
8a
9a
10a
11a
12a
13a
14a
36a
37a
38a
39a
40a
41a
42a
43a
44a
51a
52a
53a
54a
200a
B7
W71
W72
W73
W74

FIG. 18

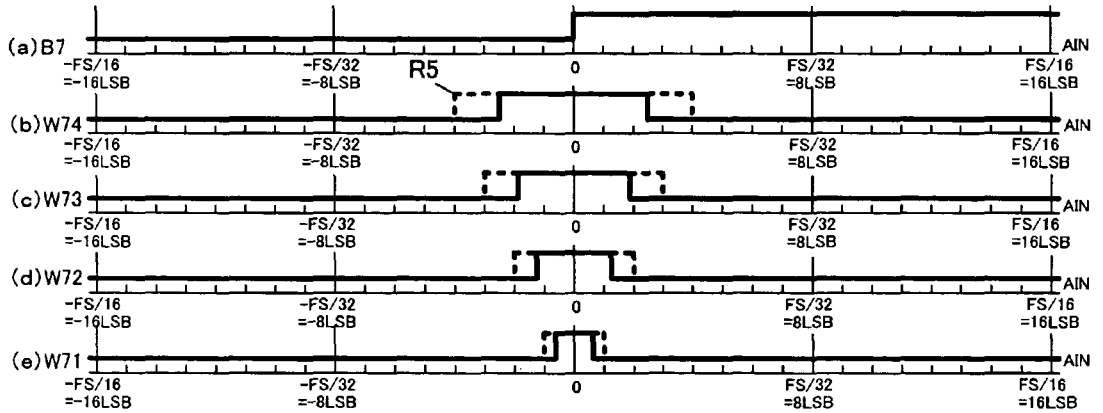

(a)B7
(b)W74
(c)W73
(d)W72
(e)W71
R5
AIN
-FS/16
=-16LSB
-FS/32
=-8LSB
0
FS/32
=8LSB
FS/16
=16LSB

FIG. 19

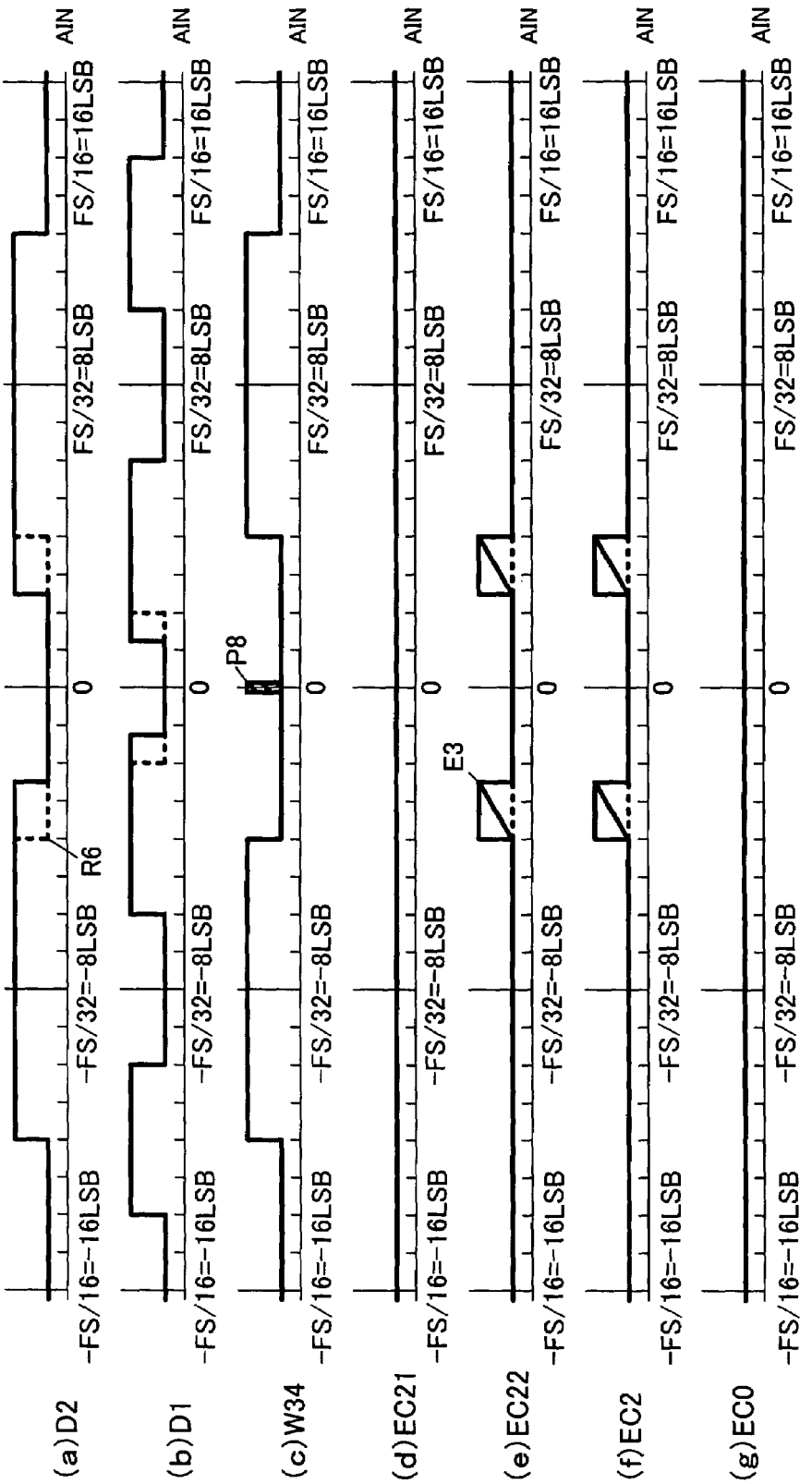
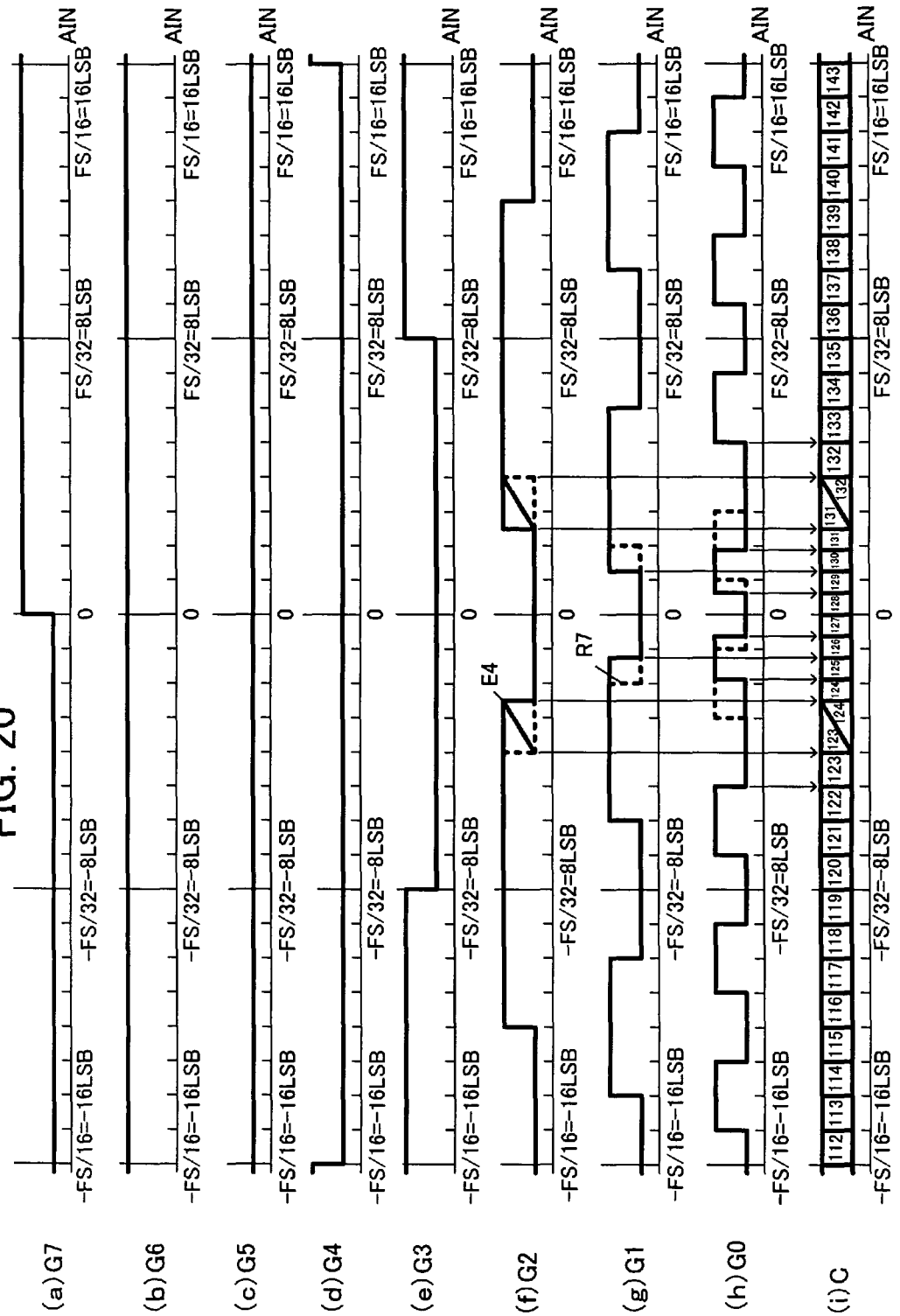

(a)D2
(b)D1
(c)W34
(d)EC21
(e)EC22
(f)EC2
(g)EC0
AIN
-FS/16=-16LSB
-FS/32=-8LSB
0
FS/32=8LSB
FS/16=16LSB
R6
P8
E3

FIG. 20


(a) G7
(b) G6
(c) G5
(d) G4
(e) G3
(f) G2
(g) G1
(h) G0
(i) C
AIN
-FS/16=-16LSB
-FS/32=-8LSB
0
FS/32=8LSB
FS/16=16LSB
E4
R7
112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143

# CASCADE A/D CONVERTER

## BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a cascade A/D converter used for a digital measuring device such as a digital oscilloscope.

2. Description of the Related Art

In a conventional cascade A/D converter, fundamental constituent elements ADA are cascaded in plural stages, the fundamental constituent elements ADA having comparators (**10***a* to **10***f*), which are first comparators for converting an analog input signal AIN to digital signals (D**7** to D**0**), D/A converters (**20***a* to **20***f*) for converting outputs (B**7** to B**2**) of the comparators (**10***a* to **10***f*) to analog signals again, and subtractors (**30***a* to **30***f*) for subtracting outputs of the D/A converters (**20***a* to **20***f*) from the analog input signal AIN (see, for example, Patent Document 1).

FIG. **1** is a structural view showing the conventional cascade A/D converter.

In FIG. **1**, a non-inverting input of the comparator **10***a* is connected to the analog input signal AIN, and an inverting input of the comparator **10***a* is connected to a comparative voltage **0**. The output B**7** of the comparator **10***a* is connected to an error correcting circuit **110**.

An input of the D/A converter **20***a* is connected to the output B**7** of the comparator **10***a*.

Moreover, an addition input of the subtractor **30***a* is connected to the analog input signal AIN, and a subtraction input of the subtractor **30***a* is connected to the output of the D/A converter **20***a*.

At a comparator **9***a*, its non-inverting input is connected to the analog input signal AIN, and its inverting input is connected to a voltage −1LSB having polarity opposite to the polarity of a voltage corresponding to the least significant bit LSB.

Moreover, at a comparator **11***a*, its non-inverting input is connected to a voltage +1LSB corresponding to the least significant bit LSB, and its inverting input is connected to the analog input signal AIN.

At an AND circuit **60***a*, its input is connected to the output of the comparator **9***a* and the output of the comparator **11***a*, and its output W**7** is connected to the error correcting circuit **110**. The comparator **9***a*, the comparator **11***a* and the AND circuit **60***a* form a window comparator **70***a*.

The comparator **10***a*, the D/A converter **20***a*, the subtractor **30***a* and the window comparator **70***a* form the first fundamental constituent element ADA.

Similarly, a non-inverting input of the comparator **10***b* is connected to an output A**1** of the subtractor **30***a*, and an inverting input of the comparator **10***b* is connected to a comparative voltage **0**. The output B**6** of the comparator **10***b* is connected to the error correcting circuit **110**.

An input of the D/A converter **20***b* is connected to the output B**6** of the comparator **10***b*.

Moreover, an addition input of the subtractor **30***b* is connected to the output A**1** of the subtractor **30***a*, and a subtraction input of the subtractor **30***b* is connected to the output of the D/A converter **20***b*.

At a comparator **9***b*, its non-inverting input is connected to the output A**1** of the subtractor **30***a*, and its inverting input is connected to the voltage −1LSB.

Moreover, at comparator **11***b*, its non-inverting input is connected to the voltage +1LSB, and its inverting input is connected to the output A**1** of the subtractor **30***a*.

At an AND circuit **60***b*, its input is connected to the output of the comparator **9***b*, the output of the comparator **11***b* and an inverted version of the output W**7**, and its output W**6** is connected to the error correcting circuit **110**. The comparator **9***b*, the comparator **11***b* and the AND circuit **60***b* form a window comparator **70***b*.



The comparator **10***b*, the D/A converter **20***b*, the subtractor **30***b* and the window comparator **70***b* form the second fundamental constituent elements ADA.

The first fundamental constituent element ADA and the second fundamental constituent element ADA are cascaded with each other.

Similarly, the first fundamental constituent element ADA, the second fundamental constituent element ADA, the third fundamental constituent element ADA formed by the comparator **10***c*, the D/A converter **20***c*, the subtractor **30***c* and a window comparator **70***c*, the fourth fundamental constituent element ADA formed by the comparator **10***d*, the D/A converter **20***d*, the subtractor **30***d* and a window comparator **70***d*, the fifth fundamental constituent element ADA formed by the comparator **10***e*, the D/A converter **20***e*, the subtractor **30***e* and a window comparator **70***e*, and the sixth fundamental constituent element ADA formed by the comparator **10***f*, the D/A converter **20***f*, the subtractor **30***f* and a window comparator **70***f*, are cascaded.

That is, in the conventional example of FIG. **1**, the fundamental constituent elements are cascaded in six stages.

A non-inverting input of the comparator **10***g* is connected to an output A**6** of the subtractor **30***f*, and an inverting input of the comparator **10***g* is connected to the comparative voltage **0**. An output B**1** of the comparator **10***g* is connected to the error correcting circuit **110**.

At a comparator **9***g*, its non-inverting input is connected to the output A**6** of the subtractor **30***f*, and its inverting input is connected of the voltage −1LSB.

Moreover, at a comparator **11***g*, its non-inverting input is connected to the voltage +1LSB, and its inverting input is connected to the output A**6** of the subtractor **30***f*.

At an AND circuit **60***g*, its input is connected to the output of the comparator **9***g*, the output of the comparator **11***g*, an inverted version of the output W**7**, an inverted version of the output W**6**, an inverted version of the output W**5**, an inverted version of the output W**4**, an inverted version of the output W**3** and an inverted version of the output W**2**. Its output W**1** is connected to the error correcting circuit **110**.

The comparator **9***g*, the comparator **11***g* and the AND circuit **60***g* form a window comparator **70***g*.

The error correcting circuit **110** performs calculations based on the following logical expressions (1) to (8) and outputs digital signals D**7** (most significant bit MSB) to D**0** (least significant bit LSB). That is, in the conventional example of FIG. **1**, digital signals (D**7** to D**0**) of an 8-bit gray code are outputted.

$$D7=B7 \tag{1}$$

$$D6=(B7 \text{ xor } B6) \text{ or } W7 \tag{2}$$

$$D5=\{(B6 \text{ xor } B5) \text{ or } W6\} \text{ and not } (W7) \tag{3}$$

$$D4=\{(B5 \text{ xor } B4) \text{ or } W5\} \text{ and not } (W7) \text{ and not } (W6) \tag{4}$$

$$D3=\{(B4 \text{ xor } B3) \text{ or } W4\} \text{ and not } (W7) \text{ and not } (W6) \text{ and not } (W5) \tag{5}$$

$$D2=\{(B3 \text{ xor } B2) \text{ or } W3\} \text{ and not } (W7) \text{ and not } (W6) \text{ and not } (W5) \text{ and not } (W4) \tag{6}$$

$$D1=\{(B2 \text{ xor } B1) \text{ or } W2\} \text{ and not } (W7) \text{ and not } (W6) \text{ and not } (W5) \text{ and not } (W4) \text{ and not } (W3) \tag{7}$$

$$D0=W1 \tag{8}$$

The operation in the conventional example of FIG. **1** having the above-described structure will now be described.

The comparator **10***a* compares the analog input signal AIN with the comparative voltage **0** and converts (A/D conversion) the analog input signal AIN to a digital signal with respect to the digital signal D**7** (most significant bit MSB).

The D/A converter **20***a* converts the 1-bit output of the comparator **10***a* to an analog signal again. The subtractor **30***a* subtracts the output of the D/A converter **20***a* from the analog input signal AIN.

Similarly, the comparator **10***b* compares the output A**1** of the subtractor **30***a* with the comparative voltage **0** and converts (A/D conversion) the analog output A**1** to a digital signal. Since the output A**1** is the result of subtracting the output of D/A converter **20***a* from the analog input signal AIN, the comparator **10***b* performs A/D conversion of the second bit from the most significant bit MSB with respect to the digital signal D**6**.

Similarly, in the conventional example of FIG. **1**, A/D conversion of each bit is performed sequentially.

In this manner, in the conventional example of FIG. **1**, digital signals (D**7** to D**0**) of 8-bit gray codes are outputted.

The window comparators (**70***a* to **70***g*) generate mask signals to restrain occurrence of an error at a transition point from 0 to 1 and a transition point from 1 to 0 in the comparators (**10***a* to **10***g*).

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However, the conventional example of FIG. **1** has a problem that settling takes a long time because of the many stages of fundamental constituent elements ADA. Therefore, the conventional example of FIG. **1** has a difficulty in achievement of high-speed operation.

## SUMMARY OF THE INVENTION

It is an object of this invention to provide a cascade A/D converter that requires a shorter settling time and enables high-speed operation.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a structural view showing a conventional cascade A/D converter.

FIG. **2** is a structural view showing an embodiment of this invention.

FIGS. **3**A to **3**E show operating waveforms in the embodiment of FIG. **2**.

FIGS. **4**A to **4**J show operating waveforms in the embodiment of FIG. **2**.

FIGS. **5**A to **5**H show operating waveforms in the embodiment of FIG. **2**.

FIGS. **6**A to **6**H show operating waveforms in the embodiment of FIG. **2**.

FIG. **7** is a structural view showing another embodiment of this invention.

FIGS. **8**A to **8**D show operating waveforms in the embodiment of FIG. **7**.

FIGS. **9**A to **9**L show operating waveforms in the embodiment of FIG. **7**.

FIGS. **10**A to **10**L show operating waveforms in the embodiment of FIG. **7**.

FIG. **11** is a structural view showing still another embodiment of this invention.

FIG. **12** is an equivalent circuit diagram of a sub-A/D converter **200***a* in the embodiment of FIG. **11** in the case where an input range is 1.375 times.

FIGS. **13**A to **13**E show operating waveforms in the embodiment of FIG. **12**.

FIGS. **14**A to **14**G show operating waveforms in the case where an input range is 1.375 times in the embodiment of FIG. **11**.

FIGS. **15**A to **15**I show operating waveforms in the case where an input range is 1.375 times in the embodiment of FIG. **11**.

FIG. **16** shows differential non-linear error (DNL) based on the operating waveforms of FIGS. **15**A to **15**I in the case where an input range is 1.375 times in the embodiment of FIG. **11**.

FIG. **17** is an equivalent circuit diagram of the sub-A/D converter **200***a* in the embodiment of FIG. **11** in the case where an input range is 0.625 times.

FIGS. **18**A to **18**E show operating waveforms in the embodiment of FIG. **17**.

FIGS. **19**A to **19**G show operating waveforms in the case where an input range is 0.625 times in the embodiment of FIG. **11**.

FIGS. **20**A to **20**I show operating waveforms in the case where an input range is 0.625 times in the embodiment of FIG. **11**.

FIG. **21** shows differential non-linear error (DNL) based on the operating waveforms of FIGS. **20**A to **20**I in the case where an input range is 0.625 times in the embodiment of FIG. **11**.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This invention will now be described in detail with reference to FIG. **2**. FIG. **2** is a structural view showing an embodiment of this invention. The same elements as those in the conventional example of FIG. **1** are denoted by the same numerals and will not be described further in detail. An arithmetic operating unit **100** in the embodiment of FIG. **2** is equivalent to the error correcting circuit **110** in the conventional example of FIG. **1**.

The embodiment of FIG. **2** is characterized by the structure of comparators (**6***a* to **9***a*, **11***a* to **14***a*, **6***b* to **9***b*, **11***b* to **14***b*, **6***c* to **9***c*, **11***c* to **14***c*, **6***d* to **9***d*, and **11***d* to **14***d*), which are second comparators, and the arithmetic operating unit **100**.

In FIG. **2**, a voltage +1LSB is a voltage corresponding to the least significant bit LSB. A voltage +2LSB is a voltage twice as large as the voltage +1LSB. A voltage +3LSB is a voltage three times as large as the voltage +1LSB. A voltage +4LSB is a voltage four times as large as the voltage +1LSB. A voltage −1LSB, a voltage −2LSB, a voltage −3LSB and a voltage −4LSB are voltages having polarity opposite to the polarity of the voltage +1LSB, the voltage +2LSB, the voltage +3LSB and the voltage +4LSB, respectively.

The comparator **6***a* is a comparator for multiplication by −4 of the least significant bit LSB. Its non-inverting input is connected to an analog input signal AIN, and its inverting input is connected to the voltage −4LSB. Its output is connected to an AND circuit **54***a* via a latch circuit **36***a*.

The comparator **7***a* is a comparator for multiplication by −3 of the least significant bit LSB. Its non-inverting input is connected to the analog input signal AIN, and its inverting input is connected to the voltage −3LSB. Its output is connected to an AND circuit **53***a* via a latch circuit **37***a*.

The comparator **8***a* is a comparator for multiplication by −2 of the least significant bit LSB. Its non-inverting input is connected to the analog input signal AIN, and its inverting

input is connected to the voltage −2LSB. Its output is connected to an AND circuit **52***a* via a latch circuit **38***a*.

The comparator **9***a* is a comparator for multiplication by −1 of the least significant bit LSB. Its non-inverting input is connected to the analog input signal AIN, and its inverting input is connected to the voltage −1LSB. Its output is connected to an AND circuit **51***a* via a latch circuit **39***a*.

The comparator **11***a* is a comparator for multiplication by +1 of the least significant bit LSB. Its non-inverting input is connected to the analog input signal AIN, and its inverting input is connected to the voltage +1LSB. Its output is connected to the AND circuit **51***a* via a latch circuit **41***a* and an inverting unit.

The comparator **12***a* is a comparator for multiplication by +2 of the least significant bit LSB. Its non-inverting input is connected to the analog input signal AIN, and its inverting input is connected to the voltage +2LSB. Its output is connected to the AND circuit **52***a* via a latch circuit **42***a* and an inverting unit.

The comparator **13***a* is a comparator for multiplication by +3 of the least significant bit LSB. Its non-inverting input is connected to the analog input signal AIN, and its inverting input is connected to the voltage +3LSB. Its output is connected to the AND circuit **53***a* via a latch circuit **43***a* and an inverting unit.

The comparator **14***a* is a comparator for multiplication by +4 of the least significant bit LSB. Its non-inverting input is connected to the analog input signal AIN, and its inverting input is connected to the voltage +4LSB. Its output is connected to the AND circuit **54***a* via a latch circuit **44***a* and an inverting unit.

An output W**71** of the AND circuit **51***a*, an output W**72** of the AND circuit **52***a*, an output W**73** of the AND circuit **53***a* and an output W**74** of the AND circuit **54***a* are connected to the arithmetic operating unit **100**.

The comparators (**6***a* to **14***a*), a D/A converter **20***a*, a subtractor **30***a*, the latch circuits (**36***a* to **44***a*), the AND circuits (**51***a* to **54***a*) and the inverting units form a first fundamental constituent element ADA.

Similarly, the comparator **6***b* is a comparator for multiplication by −4 of the least significant bit LSB. Its non-inverting input is connected to an output A**1** of the subtractor **30***a*, and its inverting input is connected to the voltage −4LSB. Its output is connected to an AND circuit **54***b* via a latch circuit **36***b*.

The comparator **7***b* is a comparator for multiplication by −3 of the least significant bit LSB. Its non-inverting input is connected to the output A**1** of the subtractor **30***a*, and its inverting input is connected to the voltage −3LSB. Its output is connected to an AND circuit **53***b* via a latch circuit **37***b*.

The comparator **8***b* is a comparator for multiplication by −2 of the least significant bit LSB. Its non-inverting input is connected to the output A**1** of the subtractor **30***a*, and its inverting input is connected to the voltage −2LSB. Its output is connected to an AND circuit **52***b* via a latch circuit **38***b*.

The comparator **9***b* is a comparator for multiplication by −1 of the least significant bit LSB. Its non-inverting input is connected to the output A**1** of the subtractor **30***a*, and its inverting input is connected to the voltage −1LSB. Its output is connected to an AND circuit **51***b* via a latch circuit **39***b*.

The comparator **11***b* is a comparator for multiplication by +1 of the least significant bit LSB. Its non-inverting input is connected to the output A**1** of the subtractor **30***a*, and its inverting input is connected to the voltage +1LSB. Its output is connected to the AND circuit **51***b* via a latch circuit **41***b* and an inverting unit.

The comparator **12***b* is a comparator for multiplication by +2 of the least significant bit LSB. Its non-inverting input is connected to the output A**1** of the subtractor **30***a*, and its inverting input is connected to the voltage +2LSB. Its output is connected to the AND circuit **52***b* via a latch circuit **42***b* and an inverting unit.

The comparator **13***b* is a comparator for multiplication by +3 of the least significant bit LSB. Its non-inverting input is connected to the output A**1** of the subtractor **30***a*, and its inverting input is connected to the voltage +3LSB. Its output is connected to the AND circuit **53***b* via a latch circuit **43***b* and an inverting unit.

The comparator **14***b* is a comparator for multiplication by +4 of the least significant bit LSB. Its non-inverting input is connected to the output A**1** of the subtractor **30***a*, and its inverting input is connected to the voltage +4LSB. Its output is connected to the AND circuit **54***b* via a latch circuit **44***b* and an inverting unit.

An output W**61** of the AND circuit **51***b*, an output W**62** of the AND circuit **52***b*, an output W**63** of the AND circuit **53***b* and an output W**64** of the AND circuit **54***b* are connected to the arithmetic operating unit **100**.

The comparators (**6***b* to **14***b*), a D/A converter **20***b*, a subtractor **30***b*, the latch circuits (**36***b* to **44***b*), the AND circuits (**51***b* to **54***b*) and the inverting units form a second fundamental constituent element ADA.

The first fundamental constituent element ADA and the second fundamental constituent element ADA are cascaded with each other.

Similarly, the first fundamental constituent element ADA, the second fundamental constituent element ADA, a third fundamental constituent element ADA formed by comparators (**6***c* to **14***c*), a D/A converter **20***c*, a subtractor **30***c*, latch circuits (**36***c* to **44***c*), AND circuits (**51***c* to **54***c*) and inverting units, and a fourth fundamental constituent element ADA formed by comparators (**6***d* to **14***d*), a D/A converter **20***d*, a subtractor **30***d*, latch circuits (**36***d* to **44***d*), AND circuits (**51***d* to **54***d*) and inverting units, are cascaded.

That is, in the embodiment of FIG. **2**, the fundamental constituent elements are connected in four stages. On the stage subsequent to the fundamental constituent elements, the following structure is provided.

A comparator **7***e* is a comparator for multiplication by −3 of the least significant bit LSB. Its non-inverting input is connected to an output A**4** of the subtractor **30***d*, and its inverting input is connected to the voltage −3LSB. Its output is connected to an AND circuit **53***e* via a latch circuit **37***e*.

A comparator **8***e* is a comparator for multiplication by −2 of the least significant bit LSB. Its non-inverting input is connected to the output A**4** of the subtractor **30***d*, and its inverting input is connected to the voltage −2LSB. Its output is connected to an AND circuit **52***e* via a latch circuit **38***e*.

A comparator **9***e* is a comparator for multiplication by −1 of the least significant bit LSB. Its non-inverting input is connected to the output A**4** of the subtractor **30***d*, and its inverting input is connected to the voltage −1LSB. Its output is connected to an AND circuit **51***e* via a latch circuit **39***e*.

A comparator **11***e* is a comparator for multiplication by +1 of the least significant bit LSB. Its non-inverting input is connected to the output A**4** of the subtractor **30***d*, and its inverting input is connected to the voltage +1LSB. Its output is connected to the AND circuit **51***e* via a latch circuit **41***e* and an inverting unit.

A comparator **12***e* is a comparator for multiplication by +2 of the least significant bit LSB. Its non-inverting input is connected to the output A**4** of the subtractor **30***d*, and its

inverting input is connected to the voltage +2LSB. Its output is connected to the AND circuit **52***e* via a latch circuit **42***e* and an inverting unit.

A comparator **13***e* is a comparator for multiplication by +3 of the least significant bit LSB. Its non-inverting input is connected to the output A**4** of the subtractor **30***d*, and its inverting input is connected to the voltage +3LSB. Its output is connected to the AND circuit **53***e* via a latch circuit **43***e* and an inverting unit.

An output W**31** of the AND circuit **51***e*, an output W**32** of the AND circuit **52***e* and an output W**33** of the AND circuit **53***e* are connected to the arithmetic operating unit **100**.

Moreover, the arithmetic operating unit **100** executes calculations for error correction and encoding based on the following logical expressions (9) to (16) and outputs digital signals D**7** (most significant bit MSB) to D**0** (least significant bit LSB). That is, in the embodiment of FIG. **2**, digital signals (D**7** to D**0**) of 8-bit gray codes are outputted.

$$D7=B7 \tag{9}$$

$$D6=(B7 \text{ xor } B6) \text{ or } W74 \tag{10}$$

$$D5=\{(B6 \text{ xor } B5) \text{ or } W64\} \text{ and not } (W74) \tag{11}$$

$$D4=\{(B5 \text{ xor } B4) \text{ or } W54\} \text{ and not } (W74) \text{ and not } (W64) \tag{12}$$

$$D3=\{(B4 \text{ xor } B3) \text{ or } W44\} \text{ and not } (W74) \text{ and not } (W64) \text{ and not } (W54) \tag{13}$$

$$D2=\text{not } (W74 \text{ or } W64 \text{ or } W54 \text{ or } W44) \tag{14}$$

$$D1=\text{not } (W72 \text{ or } W62 \text{ or } W52 \text{ or } W42 \text{ or } W32) \tag{15}$$

$$D0=(W73 \text{ or } W63 \text{ or } W53 \text{ or } W43 \text{ or } W33) \text{ and not } (W71 \text{ or } W61 \text{ or } W51 \text{ or } W41 \text{ or } W31) \tag{16}$$

The operation in the embodiment of FIG. **2** having the above-described structure will be described with reference to FIGS. **3**A to **5**H. FIGS. **3**A to **5**H show operating waveforms in the embodiment of FIG. **2**. The horizontal axes represent the analog input signal AIN within a range from −¼ of a full scale FS (i.e., −FS/4) to +¼ of the full scale (i.e., FS/4). That is, each of the operating waveforms shown in FIGS. **3**A to **5**H represents a half of the full scale FS of the analog input signal AIN.

FIG. **3**A shows the waveform of the output B**7** of the latch circuit **40***a*. FIG. **3**B shows the waveform of the output B**6** of the latch circuit **40***b*. FIG. **3**C shows the waveform of the output B**5** of the latch circuit **40***c*. FIG. **3**D shows the waveform of the output B**4** of the latch circuit **40***d*. FIG. **3**E shows the waveform of the output B**3** of the latch circuit **40***e*.

FIG. **4**A shows the waveform of the outputs of the comparators (**6***a* to **9***a* and **11***a* to **14***a*). FIG. **4**B shows the waveform of the outputs (W**71** to W**74**) of the AND circuits (**51***a* to **54***a*). FIG. **4**C shows the waveform of the outputs of the comparators (**6***b* to **9***b* and **11***b* to **14***b*). FIG. **4**D shows the waveform of the outputs (W**61** to W**64**) of the AND circuits (**51***b* to **54***b*).

FIG. **4**E shows the waveform of the outputs of the comparators (**6***c* to **9***c* and **11***c* to **14***c*). FIG. **4**F shows the waveform of the outputs (W**51** to W**54**) of the AND circuits (**51***c* to **54***c*).

FIG. **4**G shows the waveform of the outputs of the comparators (**6***d* to **9***d* and **11***d* to **14***d*). FIG. **4**H shows the waveform of the outputs (W**41** to W**44**) of the AND circuits (**51***d* to **54***d*).

FIG. **4**I shows the waveform of the outputs of the comparators (**7***e* to **9***e* and **11***e* to **13***e*). FIG. **4**J shows the waveform of the outputs (W**31** to W**33**) of the AND circuits (**51***e* to **53***e*).

FIG. **5**A shows the waveform of the digital signal D**7**. FIG. **5**B shows the waveform of the digital signal D**6**. FIG. **5**C shows the waveform of the digital signal D**5**. FIG. **5**D shows the waveform of the digital signal D**4**. FIG. **5**E shows the waveform of the digital signal D**3**. FIG. **5**F shows the waveform of the digital signal D**2**. FIG. **5**G shows the waveform of the digital signal D**1**. FIG. **5**H shows the waveform of the digital signal D**0**.

The waveforms shown in FIGS. **3**A to **3**E show that the arithmetic operating unit **100** acquires the signals of the upper five bits from the outputs (B**6** to B**3**) of the fundamental constituent elements ADA cascaded in four stages.

The outputs (B**6** to B**3**) have regions P**1** where the outputs are undefined, at transition points from 0 to 1 and transition points from 1 to 0.

The waveforms shown in FIGS. **4**A and **4**B show that A/D conversion is performed every least significant bit LSB in the region from −4LSB to +4LSB near the transition point from 0 to 1 and near the transition point from 1 to 0 of the digital signal D**7**.

Similarly, the waveforms shown in FIGS. **4**C and **4**D show that A/D conversion is performed every least significant bit LSB in the region from −4LSB to +4LSB near the transition point from 0 to 1 and near the transition point from 1 to 0 of the digital signal D**6**.

Similarly, the waveforms shown in FIGS. **4**E and **4**F show that A/D conversion is performed every least significant bit LSB in the region from −4LSB to +4LSB near the transition point from 0 to 1 and near the transition point from 1 to 0 of the digital signal D**5**.

Similarly, the waveforms shown in FIGS. **4**G and **4**H show that A/D conversion is performed every least significant bit LSB in the region from −4LSB to +4LSB near the transition point from 0 to 1 and near the transition point from 1 to 0 of the digital signal D**4**.

Similarly, the waveforms shown in FIGS. **4**I and **4**J show that A/D conversion is performed every least significant bit LSB in the region from −3LSB to +3LSB near the transition point from 0 to 1 and near the transition point from 1 to 0 of the digital signal D**3**.

Therefore, the comparators (**6***a* to **9***a*, **11***a* to **14***a*, **6***b* to **9***b*, **11***b* to **14***b*, **6***c* to **9***c*, **11***c* to **14***c*, **6***d* to **9***d*, **11***d* to **14***d*, **7***e* to **9***e*, and **11***e* to **13***e*) in the embodiment of FIG. **2** perform A/D conversion of the lower three bits in such a manner as to interpolate the transition point from 0 to 1 and the transition point from 1 to 0 of the upper five bits.

The arithmetic operating unit **100** interpolates the lower three bits on the basis of the outputs (W**61** to W**64**, W**51** to W**54**, W**41** to W**44**, and W**31** to W**33**) based on the outputs of the comparators (**6***b* to **9***b*, **11***b* to **14***b*, **6***c* to **9***c*, **11***c* to **14***c*, **6***d* to **9***d*, **11***d* to **14***d*, **7***e* to **9***e*, and **11***e* to **13***e*).

The outputs of the comparators (**6***b* to **9***b*, **11***b* to **14***b*, **6***c* to **9***c*, **11***c* to **14***c*, **6***d* to **9***d*, **11***d* to **14***d*, **7***e* to **9***e*, and **11***e* to **13***e*) and the outputs (W**61** to W**64**, W**51** to W**54**, W**41** to W**44**, and W**31** to W**33**) have regions P**2** where the outputs are undefined, respectively.

As described above, in the embodiment of FIG. **2**, an 8-bit cascade A/D converter is formed in which the fundamental constituent elements ADA are cascaded in four stages. In the embodiment of FIG. **2**, the fundamental constituent elements ADA are cascaded in four stages, whereas in the conventional example of FIG. **1**, the fundamental constituent elements ADA are cascaded in six stages.

Therefore, in the embodiment of FIG. **2**, the settling time is reduced because of the fewer stages of the fundamental constituent elements ADA.

FIGS. **6**A to **6**H show operating waveforms in the embodiment of FIG. **2**. The horizontal axes in FIGS. **6**A to **6**H represent the analog input signal AIN within a range from −½ of the full scale FS (i.e., −FS/2) to −⅜ of the full scale FS (i.e., −3FS/8).

FIG. **6**A shows the waveform of the outputs (**W71** to **W74**) of the AND circuits (**51***a* to **54***a*), corresponding to FIG. **4**B.

FIG. **6**B shows the waveform of the outputs (**W61** to **W64**) of the AND circuits (**51***b* to **54***b*), corresponding to FIG. **4**D.

FIG. **6**C shows the waveform of the outputs (**W51** to **W54**) of the AND circuits (**51***c* to **54***c*), corresponding to FIG. **4**F.

FIG. **6**D shows the waveform of the outputs (**W41** to **W44**) of the AND circuits (**51***d* to **54***d*), corresponding to FIG. **4**H.

FIG. **6**E shows the waveform of the outputs (**W31** to **W33**) of the AND circuits (**51***e* to **53***e*), corresponding to FIG. **4**J.

FIG. **6**F shows the waveform of the digital signal **D2**, corresponding to FIG. **5**F.

FIG. **6**G shows the waveform of the digital signal **D1**, corresponding to FIG. **5**G.

FIG. **6**H shows the waveform of the digital signal **D0**, corresponding to FIG. **5**H.

In FIGS. **6**F to **6**H, broken lines R represent characteristics proper to the gray codes. That is, FIGS. **6**F to **6**H show that codes **0** to **3** cannot be acquired in the embodiment of FIG. **2**.

Specifically, in the embodiment of FIG. **2**, there are codes that cannot be acquired at the lower end of the full scale FS and the upper end of the full scale FS. More specifically, in the embodiment of FIG. **2**, codes **0** to **3** and codes **252** to **255** cannot be acquired.

Such an embodiment as shown in FIG. **2** has a defect that a part of the codes are missing. However, since the missing codes are limited to the very small regions at both ends, it can operate without any trouble in most applications.

Therefore, in the embodiment of FIG. **2**, the minimum number of comparators (**6***a* to **9***a*, **11***a* to **14***a*, **6***b* to **9***b*, **11***b* to **14***b*, **6***c* to **9***c*, **11***c* to **14***c*, **6***d* to **9***d*, **11***d* to **14***d*, **7***e* to **9***e*, and **11***e* to **13***e*) necessary for practical applications are arranged, thus realizing lower cost and smaller size.

FIG. **7** is a structural view showing another embodiment of this invention. The same elements as those in the embodiment of FIG. **2** are denoted by the same numerals and will not be described further in detail. An arithmetic operating unit **101** in the embodiment of FIG. **7** is equivalent to the arithmetic operating unit **100** in the embodiment of FIG. **2**.

The embodiment of FIG. **7** is characterized by having an auxiliary A/D converter **105**.

In FIG. **7**, the input of a non-inverting amplifier **103** and the input of an inverting amplifier **104** are connected to an analog input signal AIN.

At an analog multiplexer **102**, its input A is connected to an output of the non-inverting amplifier **103**, and its input B is connected to an output of the inverting amplifier **104**. Its input SEL_A is connected to the output of a comparator **10***a*.

At a subtractor **30***e*, its addition input is connected to an output OUT of the analog multiplexer **102**, and its subtraction input is connected to a voltage FS/2 corresponding to ½ of the full scale FS.

A comparator **6***f* is a comparator for multiplication by four of the least significant bit LSB. Its non-inverting input is connected to an output of the subtractor **30***e*, and its inverting input is connected to a voltage −4LSB. Its output is connected to an AND circuit **51***f* via a latch circuit **36***f*.

A comparator **7***f* is a comparator for multiplication by three of the least significant bit LSB. Its non-inverting input is connected to the output of the subtractor **30***e*, and its inverting input is connected to a voltage −3LSB. Its output is connected to an AND circuit **53***f* via a latch circuit **37***f*.

A comparator **8***f* is a comparator for multiplication by two of the least significant bit LSB. Its non-inverting input is connected to the output of the subtractor **30***e*, and its inverting input is connected to a voltage −2LSB. Its output is connected to an AND circuit **52***f* via a latch circuit **38***f*.

A comparator **9***f* is a comparator for multiplication by one of the least significant bit LSB. Its non-inverting input is connected to the output of the subtractor **30***e*, and its inverting input is connected to a voltage −1LSB. Its output is connected to the AND circuit **53***f* via a latch circuit **39***f* and an inverting unit.

An output **W74** is connected to the AND circuit **51***f* via an inverting unit. The output **W74** is also connected to the AND circuit **52***f* via an inverting unit. The output **W74** is also connected to the AND circuit **53***f* via an inverting unit.

An output **B2** of the AND circuit **51***f*, an output **B1** of the AND circuit **52***f* and an output **W11** of the AND circuit **53***f* are connected to the arithmetic operating unit **101**.

The non-inverting amplifier **103**, the inverting amplifier **104**, the analog multiplexer **102**, the subtractor **30***e*, the comparators (**6***f* to **9***f*), the latch circuits (**36***f* to **39***f*) and the AND circuits (**51***f* to **53***f*) form the auxiliary A/D converter **105**.

The auxiliary A/D converter **105** operates in parallel with a structure having fundamental constituent elements ADA cascaded in plural stages. It operates at a higher speed than the structure having fundamental constituent elements ADA cascaded in plural stages (i.e., structure equivalent to the embodiment of FIG. **2**).

Specifically, the delay at the auxiliary A/D converter **105** is of a small value based on the non-inverting amplifier **103**, the inverting amplifier **104**, the analog multiplexer **102**, the subtractor **30***e*, the comparators (**6***f* to **9***f*), the latch circuits (**36***f* to **39***f*) and the AND circuits (**51***f* to **53***f*), whereas the delay in the structure having fundamental constituent elements ADA cascaded in plural stages is of a large value based on the comparators (**10***a* to **10***e*), the D/A converters (**20***a* to **20***d*), the subtractors (**30***a* to **30***d*), the latch circuits (**37***e* to **43***e*) and the AND circuits (**51***e* to **53***e*).

The arithmetic operating unit **101** executes calculation for error correction and encoding based on the following logical expressions (17) to (24) and outputs digital signals **D7** (most significant bit MSB) to **D0** (least significant bit LSB) That is, in the embodiment of FIG. **7**, digital signals (**D7** to **D0**) of 8-bit gray codes are outputted.

$$D7=B7 \tag{17}$$

$$D6=(B7 \text{ xor } B6) \text{ or } W74 \tag{18}$$

$$D5=\{(B6 \text{ xor } B5) \text{ or } W64\} \text{ and not } (W74) \tag{19}$$

$$D4=\{(B5 \text{ xor } B4) \text{ or } W54\} \text{ and not } (W74) \text{ and not } (W64) \tag{20}$$

$$D3=\{(B4 \text{ xor } B3) \text{ or } W44\} \text{ and not } (W74) \text{ and not } (W64) \text{ and not } (W54) \tag{21}$$

$$D2=\text{not } (W74 \text{ or } W64 \text{ or } W54 \text{ or } W44) \text{ and not } (B2) \tag{22}$$

D1=not (W72 or W62 or W52 or W42 or W32) and not (B2) (23)

D0= (W73 or W63 or W53 or W43 or W33) and not (W71 or W61 or W51 or W41 or W31) or W11 (24)

Here, the operations of the analog multiplexer **102** and the subtractor **30***e* with reference to FIGS. **8**A to **8**D. FIGS. **8**A to **8**D show operating waveforms in the embodiment of FIG. **7**. In FIGS. **8**A to **8**D, the horizontal axes represent the analog input signal AIN within a range from −½of the full scale FS (i.e., −FS/2) to +½ of the full scale FS (i.e., FS/2).

FIG. **8**A shows the waveforms of the input A of the analog multiplexer **102** and the input B of the analog multiplexer **102**. FIG. **8**B shows the waveform of the input SEL_A of the analog multiplexer **102**. FIG. **8**C shows the waveform of the output OUT of the analog multiplexer **102**. FIG. **8**D shows the waveform of the output of the subtractor **30***e*.

As shown in FIGS. **8**A to **8**C, when the input SEL_A is at high level, the analog multiplexer **102** outputs the value of the input A as the output OUT, and when the input SEL_A is at low level, the analog multiplexer **102** outputs the value of the input B as the output OUT.

The subtractor **30***e* subtracts the voltage FS/2 from the output OUT and shifts the level of the output OUT. The output of the subtractor **30***e* is 0 when the analog input signal AIN is −FS/2, and the output of the subtractor **30***e* is 0 when the input analog signal AIN is FS/2, as shown in FIG. **8**D.

Therefore, the analog multiplexer **102** switches the vicinity of the lower end of the range and the vicinity of the upper end of the range. In the embodiment of FIG. **7**, with this structure, the number of constituent elements is reduced, and simplification, lower cost and smaller size are realized.

The operation in the embodiment of FIG. **7**, constructed as described above, will now be described with reference to FIGS. **9**A to **9**L and FIGS. **10**A to **10**L. FIGS. **9**A to **9**L and FIGS. **10**A to **10**L show operating waveforms in the embodiment of FIG. **7**. In FIGS. **9**A to **9**L, the horizontal axes represent the vicinity of the lower end of the analog input signal AIN within a range from −½ of the full scale FS (i.e., −FS/2) to −⅜ of the full scale FS (i.e., −3FS/8). In FIGS. **10**A to **10**L, the horizontal axes represent the vicinity of the upper end of the analog input signal AIN within a range from +⅜ of the full scale FS (i.e., 3FS/8) to +½ of the full scale FS (i.e., FS/2).

FIGS. **9**A and **10**A show the waveform of the output of the subtractor **30***e*, corresponding to FIG. **8**D. FIGS. **9**B and **10**B show the waveform of the output B**2** of the AND circuit **51***f*. FIGS. **9**C and **10**C show the waveform of the output B**1** of the AND circuit **52***f*. FIGS. **9**D and **10**D show the waveform of the output W**11** of the AND circuit **53***f*.

FIGS. **9**E and **10**E show the waveform of the outputs (W**71** to W**74**), corresponding to FIG. **6**A. FIGS. **9**F and **10**F show the waveform of the outputs (W**61** to W**64**), corresponding to FIG. **6**B. FIGS. **9**G and **10**G show the waveform of the outputs (W**51** to W**54**), corresponding to FIG. **6**C. FIGS. **9**H and **10**H show the waveform of the outputs (W**41** to W**44**), corresponding to FIG. **6**D. FIGS. **9**I and **10**I show the waveform of the outputs (W**31** to W**33**), corresponding to FIG. **6**E.

FIGS. **9**J and **10**J show the waveform of the digital signal D**2**, corresponding to FIG. **6**F. FIGS. **9**K and **10**K show the waveform of the digital signal D**1**, corresponding to FIG. **6**G. FIGS. **9**L and **10**L show the waveform of the digital signal D**0**, corresponding to FIG. **6**H.

First, the operation in the vicinity of the lower end of the range in the embodiment of FIG. **7** will be described with reference to FIGS. **9**A to **9**L. As shown in FIG. **9**A, the output of the subtractor **30***e* is 0 when the analog input signal AIN is at a voltage −FS/2, and it decreases with the increase of the analog input signal AIN.

When the analog input signal AIN increases from the voltage −FS/2 by a voltage +1LSB, the output of the subtractor **30***e* increases from 0 by a voltage −1LSB. The output of the comparator **9***f* changes from high level to low level, and the output W**11** changes from low level to high level.

When the analog input signal AIN increases from the voltage −FS/2 by a voltage +2LSB, the output of the subtractor **30***e* increases from 0 by a voltage −2LSB. The output of the comparator **8***f* changes from high level to low level, and the output B**1** changes from high level to low level.

When the analog input signal AIN increases from the voltage −FS/2 by a voltage +3LSB, the output of the subtractor **30***e* increases from 0 by a voltage −3LSB. The output of the comparator **7***f* changes from high level to low level, and the output W**11** changes from high level to low level.

When the analog input signal AIN increase from the voltage −FS/2 by a voltage +4LSB, the output of the subtractor **30***e* increases from 0 by a voltage −4LSB. The output of the comparator **6***f* changes from high level to low level, and the output B**2** changes from high level to low level.

That is, in the vicinity of the lower end of the range in the embodiment of FIG. **7**, the comparators (**6***f* to **9***f*) perform A/D conversion every least significant bit LSB. The arithmetic operating unit **101** in the embodiment of FIG. **7** interpolates the lower three bits.

Therefore, in the embodiment of FIG. **7**, correct codes **252** to **255** can be acquired, as shown in FIGS. **9**J to **9**L.

Next, the operation in the vicinity of the upper end of the range in the embodiment of FIG. **7** will be described with reference to FIGS. **10**A to **10**L. As shown in FIG. **10**A, the output of the subtractor **30***e* is 0 when the analog input signal AIN is at a voltage FS/2, and it increases with the decrease of the analog input signal AIN.

When the analog input signal AIN increases from the voltage FS/2 by a voltage −1LSB, the output of the subtractor **30***e* increases from 0 by a voltage −1LSB. The output of the comparator **9***f* changes from high level to low level, and the output W**11** changes from low level to high level.

When the analog input signal AIN increases from the voltage FS/2 by a voltage −2LSB, the output of the subtractor **30***e* increases from 0 by a voltage −2LSB. The output of the comparator **8***f* changes from high level to low level, and the output B**1** changes from high level to low level.

When the analog input signal AIN increases from the voltage FS/2 by a voltage −3LSB, the output of the subtractor **30***e* increases from 0 by a voltage −3LSB. The output of the comparator **7***f* changes from high level to low level, and the output W**11** changes from high level to low level.

When the analog input signal AIN increase from the voltage FS/2 by a voltage −4LSB, the output of the subtractor **30***e* increases from 0 by a voltage −4LSB. The output of the comparator **6***f* changes from high level to low level, and the output B**2** changes from high level to low level.

That is, in the vicinity of the upper end of the range in the embodiment of FIG. **7**, the comparators (**6***f* to **9***f*) perform A/D conversion every least significant bit LSB. The arithmetic operating unit **101** in the embodiment of FIG. **7** interpolates the lower three bits.

Therefore, in the embodiment of FIG. **7**, correct codes **0** to **3** can be acquired, as shown in FIGS. **10**J to **10**L.

By the above-described operation, in the embodiment of FIG. **7**, all the codes can be correctly acquired on the full scale FS.

Meanwhile, the waveform of the output OUT and the waveform of the output of the subtractor **30***e* have a region P**4** where the outputs are undefined, respectively, near the transition point of the input SEL_A, as shown in FIGS. **8**C and **8**D. The region P**4** is in the vicinity of the point where the analog input signal AIN becomes 0 and therefore in the vicinity of the switching point of the analog multiplexer **102**.

In such vicinity of the region P**4**, the output W**74** of the AND circuit **54***a* is at high level, and the output B**2** of the AND circuit **51***f*, the output B**1** of the AND circuit **52***f* and the output W**11** of the AND circuit **53***f* are at low level and therefore masked.

That is, the auxiliary A/D converter **105** masks the outputs (B**2**, B**1** and W**11**) in the vicinity of the switching point of the analog multiplexer **102**.

The embodiment of FIG. **7** operates normally and no malfunction occurs in the embodiment of FIG. **7**. The AND circuit **51***f*, the AND circuit **52***f* and the AND circuit **53***f* restrains malfunction based on the region P**4** where the output is undefined.

While the input SEL_A of the analog multiplexer **102** is connected to the output of the comparator **10***a* in the above-described embodiment, similar effects and advantages can be achieved, for example, by connecting the input SEL_A to other signals than the output of the comparator **10***a*.

Specifically, in association with the embodiments of FIG. **2** and FIG. **7**, similar effects and advantages can be achieved by connecting the input SEL_A of the analog multiplexer **102** to the signal that switches between the vicinity of the lower end of the range and the vicinity of the upper end of the range.

Moreover, while the output W**74** is connected to the AND circuits (**51***f* to **53***f*) in the above-described embodiment, similar effects and advantages can be achieved, for example, by connecting the output W**73** to the AND circuits (**51***f* to **53***f*).

Specifically, in association with the embodiment of FIG. **7**, similar effects and advantages can be achieved as long as the auxiliary A/D converter **105** masks the output in the vicinity of the switching point (region P**4**) of the analog multiplexer **102**.

FIG. **11** is a structural view showing still another embodiment of this invention. The same elements as those in the embodiment of FIG. **2** are denoted by the same numerals and will not be described further in detail.

The embodiment of FIG. **11** is characterized by having a structure related to a differential non-linear error correcting circuit **300** (differential non-linear error correcting unit).

In the embodiment of FIG. **11**, comparators (**6***a* to **14***a*) latch circuits (**36***a* to **44***a*) and AND circuits (**51***a* to **54***a*) are formed with structures similar to those in the embodiment of FIG. **2**, and they form a first sub-A/D converter **200***a*.

Similarly, comparators (**6***b* to **14***b*), latch circuits (**36***b* to **44***b*) and AND circuits (**51***b* to **54***b*) form a second sub-A/D converter **200***b*. Comparators (**6***c* to **14***c*), latch circuits (**36***c* to **44***c*) and AND circuits (**51***c* to **54***c*) form a third sub-A/D converter **200***c*. Comparators (**6***d* to **14***d*), latch circuits (**36***d* to **44***d*) and AND circuits (**51***d* to **54***d*) form a fourth sub-A/D converter **200***d*.

A comparator **6***e* is a comparator for multiplication by −4 of the least significant bit LSB. Its non-inverting input is connected to an output A**4** of a subtractor **30***d*, and its inverting input is connected to a voltage −4LSB. Its output is connected to an AND circuit **54***e* via a latch circuit **36***e*.

A comparator **14***e* is a comparator for multiplication by +4 of the least significant bit LSB. Its non-inverting input is connected to the output A**4** of the subtractor **30***d*, and its inverting input is connected to a voltage +4LSB. Its output is connected to the AND circuit **54***e* via a latch circuit **44***e* and an inverting unit.

Comparators (**6***a* to **14***a*), latch circuits (**36***e* to **44***e*) and AND circuits (**51***e* to **54***e*) form a fifth sub-A/D converter **201***e*.

Digital signals (D**7** to D**3**) of upper five bits outputted from an arithmetic operating unit **100** become digital signals (G**7** to G**3**) via flip-flops (**70** to **74**). The digital signal G**7** is the most significant bit MSB.

A digital signal D**2** of a lower bit becomes a digital signal G**2** via a flip-flop **75** and an exclusive OR circuit **64**. A digital signal D**1** of a lower bit becomes a digital signal G**1** via a flip-flop **76**. Moreover, a digital signal D**0** of a lower bit becomes a digital signal G**0** via a flip-flop **77** and an AND circuit **65**. The digital signal G**0** is the least significant bit LSB.

The differential non-linear error correcting circuit **300** inputs the digital signal D**2**, the digital signal D**1**, and an output W**34** of the AND circuit **54***e*, and outputs an output EC**2** and an output EC**0**. The output EC**2** is connected to an input of the exclusive OR circuit **64**, and the output EC**0** is connected to an input of the AND circuit **65** via an inverting unit.

The internal structure of the differential non-linear error correcting circuit **300** will now be described in detail.

To an input of an AND circuit **60**, an inverted version of the digital signal D**2**, the digital signal D**1**, the output W**34**, and an inverted version of the output EC**2** are connected.

To an input of an AND circuit **61**, the digital signal D**2**, an inverted version of the output W**34**, and an inverted version of the output EC**2** are connected.

To an input of an AND circuit **63**, an output EC**21** of the AND circuit **60** and an output EC**22** of the AND circuit **61** are connected. An output EC**23** of the AND circuit **63** becomes the output EC**2** via a flip-flop **78**.

Moreover, to an input of an AND circuit **62**, an inverted version of the digital signal D**2**, the digital signal D**1**, and the output W**34** are connected. An output EC**20** of the AND circuit **62** becomes the output EC**0** via a flip-flop **79**.

That is, the AND circuits **60** to **62** calculate the logical products of the outputs of the comparators **6***e* and **14***e*, which are second comparators, and the digital signals D**2** and D**1** of lower bits.

Therefore, the outputs (EC**21**, EC**22**, EC**23**, EC**20**) in the differential non-linear error correcting circuit **300** satisfy the following logical expressions (25) to (28).

$$EC21=\text{not}(D2)\ \text{and}\ D1\ \text{and}\ W34\ \text{and not}(EC2) \tag{25}$$

$$EC22=D2\ \text{and not}(W34)\ \text{and not}(EC2) \tag{26}$$

$$EC23=EC21\ \text{or}\ EC22 \tag{27}$$

$$EC20=\text{not}(D2)\ \text{and}\ D1\ \text{and}\ W34 \tag{28}$$

The digital signals (G**7** to G**0**) satisfy the following logical expressions (29) to (36) and form 8-bit gray codes.

$$G7=D7 \tag{29}$$

$$G6=D6 \tag{30}$$

$$G5=D5 \tag{31}$$

G4=D4 (32)

G3=D3 (33)

G2=D2 or EC2=D2 xor EC23 (34)

G1=D1 (35)

G0=D0 and not (EC0)=D0 and not (EC20) (36)

First, the operation in the case where the embodiment of FIG. **11** is in the normal state (ideal state), that is, in the case where the A/D conversion range of the sub-A/D converter **200***a* is stable, will be described.

In this case, the output EC**21** is zero (EC**21**=0), the output EC**22** is zero (EC**22**=0), the output EC**23** is zero (EC**23**=0), and the output EC**2** is zero (EC**2**=0). The output EC**20** is zero (EC**20**=0) and the output EC**0** is zero (EC**0**=0).

Thus, in the case, the digital signal G**2** is the digital signal D**2** (G**2**=D**2**) and the digital signal G**0** is the digital signal D**0** (G**0**=D**0**).

Therefore, the operation in the case where the embodiment of FIG. **11** is in the normal state is equivalent to the operation in the case where the embodiment of FIG. **2** is in the normal state. It is equivalent to the above-described operation in the embodiment of FIG. **2**.

Next, the operation in the case where the embodiment of FIG. **11** is in an abnormal state (state deviated from the ideal state), that is, in the case where the A/D conversion range of the sub-A/D converter **200***a* varies, will be described.

First, the operation in the embodiment of FIG. **11**, for example, in the case where the input range of the sub-A/D converter **200***a* is 1.375 times, will be described. FIG. **12** is an equivalent circuit diagram of the sub-A/D converter **200***a* in the embodiment of FIG. **11** in the case where the input range is 1.375 times. The description of the other parts than the sub-A/D converter **200***a* is not given here.

In this case, the sub-A/D converter **200***a* in the embodiment of FIG. **11** is equivalently constructed as shown in the equivalent circuit diagram of FIG. **12**. Specifically, the inverting input of the comparator **6***a* is a voltage (−4LSB×1.375) the inverting input of the comparator **7***a* is a voltage (−3LSB×1.375), the inverting input of the comparator **8***a* is a voltage (−2LSB×1.375), the inverting input of the comparator **9***a* is a voltage (−1LSB×1.375), the inverting input of the comparator **11***a* is a voltage (+1LSB×1.375), the inverting input of the comparator **12***a* is a voltage (+2LSB×1.375), the inverting input of the comparator **13***a* is a voltage (+3LSB×1.375), and the inverting input of the comparator **14***a* is a voltage (+4LSB×1.375).

FIGS. **13**A to **15**I show operating waveforms in the embodiment of FIG. **12** and operating waveforms in the case where the input range is 1.375 times in the embodiment of FIG. **11**. In FIGS. **13**A to **15**I, the horizontal axes represent the analog input signal AIN within a range from −1/16 of the full scale FS (i.e., −FS/16) to +1/16 of the full scale FS (i.e., FS/16).

FIG. **13**A shows the waveform of the output B**7**. FIG. **13**B shows the waveform of the output W**74**. FIG. **13**C shows the waveform of the output W**73**. FIG. **13**D shows the waveform of the output W**72**. FIG. **13**E shows the waveform of the output W**71**.

In FIGS. **13**B to **13**E, broken lines R**2** represent characteristics in the case where the embodiment of FIG. **11** is in the ideal state (ideal characteristics). The characteristics of the outputs W**74** to W**71** change because the input range in the embodiment of FIG. **11** is enlarged.

FIG. **14**A shows the waveform of the digital signal D**2**. FIG. **14**B shows the waveform of the digital signal D**1**. FIG. **14**C shows the waveform of the output W**34**. FIG. **14**D shows the waveform of the output EC**21**. FIG. **14**E shows the waveform of the output EC**22**. FIG. **14**F shows the waveform of the output EC**2**. FIG. **14**G shows the waveform of the output EC**0**.

In FIGS. **14**A and **14**B, broken lines R**3** represent characteristics in the case where the embodiment of FIG. **11** is in the ideal state (ideal characteristics). In FIGS. **14**D and **14**F, slant line parts E**1** represent characteristics that zero (0) and 1 occur alternately and evenly.

The regions where the broken lines R**3** appear and the regions where the slant line parts E**1** appear correspond to each other. That is, the AND circuit **60** and the AND circuit **62** detect a shift when the sub-A/D converter **200***a* enlarges the input range.

In the circuit formed by the AND circuit **60**, the AND circuit **61**, the AND circuit **63** and the flip-flop **78**, zero (0) and 1 occur alternately and evenly. When the output EC**2** becomes 1, the input of the AND circuit **60** becomes zero. Therefore, the output EC**21** and the output EC**2** have characteristics that zero (0) and 1 occur alternately and evenly.

FIG. **15**A shows the waveform of the digital signal G**7**. FIG. **15**B shows the waveform of the digital signal G**6**. FIG. **15**C shows the waveform of the digital signal G**5**. FIG. **15**D shows the waveform of the digital signal G**4**. FIG. **15**E shows the waveform of the digital signal G**3**. FIG. **15**F shows the waveform of the digital signal G**2**. FIG. **15**G shows the waveform of the digital signal G**1**. FIG. **15**H shows the waveform of the digital signal G**0**. FIG. **15**I shows digital output codes C corresponding to the digital signals (G**7** to G**0**).

In FIGS. **15**G and **15**H, broken lines R**4** represent characteristics in the case where the embodiment of FIG. **11** is in the ideal state (ideal characteristics). Moreover, in FIG. **15**F, slant line parts E**2** represent characteristics that zero (0) and 1 occur alternately and evenly.

In FIG. **15**I, all the digital output codes Care outputted. That is, no code is missing. The codes are arranged in order.

With the above-described structure, in the embodiment of FIG. **11**, a shift in the case where the sub-A/D converter **200***a* enlarges the input range is detected and properly corrected.

FIG. **16** shows differential non-linear error (DNL) based on the operating waveforms of FIGS. **15**A to **15**I in the case where the input range of the sub-A/D converter **200***a* is 1.375 times in the embodiment of FIG. **11**. As shown in FIG. **16**, the differential non-linear error is between −0.5LSB and +0.375LSB.

Therefore, in the embodiment of FIG. **11**, the differential non-linear error can be reduced. Meanwhile, in the embodiment of FIG. **2**, the differential non-linear error (DNL) in the case where the input range of the sub-A/D converter **200***a* is 1.375 times is between −1LSB and +0.875LSB (not shown).

Second, the operation in the embodiment of FIG. **11** in the case where the input range of the sub-A/D converter **200***a* is 0.625 times will be described. FIG. **17** is an equivalent circuit diagram of the sub-A/D converter **200***a* in the embodiment of FIG. **11** in the case where the input range is 0.625 times. The equivalent circuit diagram of FIG. **17** corresponds to the equivalent circuit diagram of FIG. **12**.

In this case, the sub-A/D converter **200***a* in the embodiment of FIG. **11** is equivalently structured as shown in the equivalent circuit diagram of FIG. **17**. Specifically, the inverting input of the comparator **6***a* is a voltage (−4LSB×0.625) the inverting input of the comparator **7***a* is

a voltage (−3LSB×0.625), the inverting input of the comparator **8***a* is a voltage (−2LSB×0.625), the inverting input of the comparator **9***a* is a voltage (−1LSB×1.375), the inverting input of the comparator **11***a* is a voltage (+1LSB×0.625), the inverting input of the comparator **12***a* is a voltage (+2LSB×0.625), the inverting input of the comparator **13***a* is a voltage (+3LSB×0.625), and the inverting input of the comparator **14***a* is a voltage (+4LSB×0.625).

FIGS. **18**A to **20**I show operating waveforms in the embodiment of FIG. **17** and operating waveforms in the case where the input range is 0.625 times in the embodiment of FIG. **11**. FIGS. **18**A to **20**I correspond to FIGS. **13**A to **15**I. Therefore, similar parts will not be described further in detail.

In FIGS. **18**B to **18**E, broken lines R**5** represent characteristics in the case where the embodiment of FIG. **11** is in the ideal state (ideal characteristics). The characteristics of the outputs W**74** to W**71** change because the input range in the embodiment of FIG. **11** is narrowed.

In FIGS. **19**A and **19**B, broken lines R**6** represent characteristics in the case where the embodiment of FIG. **11** is in the ideal state (ideal characteristics). In FIGS. **19**E and **19**F, slant line parts E**3** represent characteristics that zero (0) and 1 occur alternately and evenly.

The regions where the broken lines R**6** appear and the regions where the slant line parts E**3** appear correspond to each other. That is, the AND circuit **61** detects a shift when the sub-A/D converter **200***a* narrows the input range.

In the circuit formed by the AND circuit **60**, the AND circuit **61**, the AND circuit **63** and the flip-flop **78**, zero (0) and 1 occur alternately and evenly. When the output EC**2** becomes 1, the input of the AND circuit **61** becomes zero. Therefore, the output EC**22** and the output EC**2** have characteristics that zero (0) and 1 occur alternately and evenly.

In FIGS. **20**G and **20**H, broken lines R**7** represent characteristics in the case where the embodiment of FIG. **11** is in the ideal state (ideal characteristics). Moreover, in FIG. **20**F, slant line parts E**4** represent characteristics that zero (0) and 1 occur alternately and evenly.

In FIG. **20**I, all the digital output codes Care outputted. That is, no code is missing. The codes are arranged in order.

With the above-described structure, in the embodiment of FIG. **11**, a shift in the case where the sub-A/D converter **200***a* narrows the input range is detected and properly corrected.

FIG. **21** shows differential non-linear error (DNL) based on the operating waveforms of FIGS. **20**A to **20**I in the case where the input range of the sub-A/D converter **200***a* is 0.625 times in the embodiment of FIG. **11**. As shown in FIG. **21**, the differential non-linear error is between −0.375LSB and +0.75LSB.

Therefore, in the embodiment of FIG. **11**, the differential non-linear error can be reduced. Meanwhile, in the embodiment of FIG. **2**, the differential non-linear error (DNL) in the case where the input range of the sub-A/D converter **200***a* is 0.625 times is between −0.375LSB and +1.5LSB (not shown).

In the above-described embodiment, the case where the input range of the sub-A/D converter **200***a* is deviated from the ideal state is described. However, similar effects and advantages can be achieved, for example, when the sub-A/D converter **200***b* to the sub-A/D converter **200***d* and the sub-A/D converter **200***e* are deviated from the ideal state.

While the 8-bit cascade A/D converter is used in the above-described embodiment, similarly preferable effects can be achieved by a cascade A/D converter other than the 8-bit cascade A/D converter.

As can be understood from the above description, this invention is not limited to the above-described embodiment and includes various changes and modifications without departing from the scope of the invention.

This invention has the following effects.

According to this invention, since fewer stages of fundamental constituent elements ADA may be used, the settling time is reduced and a high-speed cascade A/D converter can be provided.

Particularly, according to this invention, an 8-bit cascade A/D converter having fundamental constituent elements ADA cascaded in four stages can be formed.

Moreover, according to this invention, a high-speed cascade A/D converter that can correctly acquire all the codes on the full scale FS can be provided.

Also, according to this invention, a cascade A/D converter of lower cost and smaller size can be provided.

Moreover, according to this invention, it is possible to provide a cascade A/D converter that detects and properly corrects a shift when the input range of a sub-A/D converter varies.

What is claimed is:

**1**. A cascade A/D converter comprising fundamental constituent elements cascaded in plural stages, each fundamental constituent element comprising a first comparator for inputting an analog input signal, a D/A converter for converting an output of the first comparator to an analog signal again, and a subtractor for subtracting an output of the D/A converter from the analog input signal,

the fundamental constituent elements comprising:

a second comparator for inputting the analog input signal every least significant bit near a transition point of the first comparator; and

an arithmetic operating unit for generating upper bits based on an output of the first comparator and interpolating lower bits based on an output of the second comparator.

**2**. The cascade A/D converter as claimed in claim **1**, wherein a comparative voltage of the first comparator is 0.

**3**. The cascade A/D converter as claimed in claim **2**, wherein a comparative voltage of the second comparator increases and decreases from 0 as a central value every least significant bit.

**4**. The cascade A/D converter as claimed in claim **1**, comprising an auxiliary A/D converter formed in parallel with the fundamental constituent elements and for converting the analog input signal to a digital signal every least significant bit in the vicinity of a lower end of a range and in the vicinity of an upper end of the range.

**5**. The cascade A/D converter as claimed in claim **4**, wherein the auxiliary A/D converter has an analog multiplexer for switching the vicinity of the lower end of the range and the vicinity of the upper end of the range.

**6**. The cascade A/D converter as claimed in claim **5**, wherein the auxiliary A/D converter masks an output near a switching point of the analog multiplexer.

**7**. The cascade A/D converter as claimed in claim **1**, wherein the fundamental constituent elements are cascaded in four stages, and

the second comparator has a comparator for multiplication by −4 of the least significant bit, a comparator for multiplication by −3 of the least significant bit, a comparator for multiplication by −2 of the least significant bit, a comparator for multiplication by −1 of the least significant bit, a comparator for multiplication by

+1 of the least significant bit, a comparator for multiplication by +2 of the least significant bit, a comparator for multiplication by +3 of the least significant bit, and a comparator for multiplication by +4 of the least significant bit.

**8**. The cascade A/D converter as claimed in claim **7**, comprising an auxiliary A/D converter formed in parallel with the fundamental constituent elements,

the auxiliary A/D converter having a comparator for multiplication by one of the least significant bit, a comparator for multiplication by two of the least significant bit, a comparator for multiplication by three of the least significant bit, and a comparator for multiplication by four of the least significant bit,

the auxiliary A/D converter converting the analog input signal to a digital signal in the vicinity of a lower end of a range and in the vicinity of an upper end of the range.

**9**. The cascade A/D converter as claimed in claim **7**, wherein outputs **(W74, W64, W54, W44)** based on an output of the comparator for multiplication by −4 of the least significant bit and an output of the comparator for multiplication by +4 of the least significant bit,

outputs **(W73, W63, W53, W43, W33)** based on an output of the comparator for multiplication by −3 of the least significant bit and an output of the comparator for multiplication by +3 of the least significant bit,

outputs **(W72, W62, W52, W42, W32)** based on an output of the comparator for multiplication by −2 of the least significant bit and an output of the comparator for multiplication by +2 of the least significant bit,

outputs **(W71, W61, W51, W41, W31)** based on an output of the comparator for multiplication by −1 of the least significant bit and an output of the comparator for multiplication by +1 of the least significant bit, and

the lower bits **(D2, D1, D0)** are correlated with the following logical expressions:

D2=not (**W74** or **W64** or **W54** or **W44**)

D1=not (**W72** or **W62** or **W52** or **W42** or **W32**)

D0=(**W73** or **W63** or **W53** or **W43** or **W33**) and not (**W71** or **W61** or **W51** or **W41** or **W31**).

**10**. The cascade A/D converter as claimed in claim **1**, comprising a differential non-linear error correcting unit for detecting a shift of a A/D conversion range of a sub-A/D converter having the second comparator and correcting the shift.

**11**. The cascade A/D converter as claimed in claim **10**, wherein the differential non-linear error correcting unit has an AND circuit for detecting the shift on the basis of a logical product an output of a comparator formed on a stage subsequent to the fundamental constituent elements and the lower bits.

**12**. The cascade A/D converter as claimed in claim **11**, wherein the differential non-linear error correcting unit has a unit for generating zero and 1 alternately and evenly with respect to the shift and thus correcting the shift.

**13**. The cascade A/D converter as claimed in claim **9**, comprising:

AND circuits **(60, 61, 62)** for inputting an output **(W34)** based on an output of the comparator **(6*e*)** for multiplication by −4 of the least significant bit and an output of the comparator **(14*e*)** for multiplication by +4 of the least significant bit, and the lower bits **(D2, D1)**, the AND circuit being formed on a stage subsequent to the fundamental constituent elements;

an exclusive OR circuit **(64)** of outputs of the AND circuits and the lower bit **(D2)**; and

an AND circuit **(65)** of the outputs of the AND circuits and the lower bit **(D0)**.

* * * * *

# FURTHER READING

**Click any one of the following links to be taken to a website which contains the following documents.**

**The following are some recent examples of Asynchronous ADC activity off the web.**

6 bit Asynchronous December 2006
Asynchronous ADC In CAD Mentor Graphics
Asynchronous Data Processing System
ASYNCHRONOUS PARALLEL RESISTORLESS ADC
Flash Asynchronous Analog-to-Digital Converter
Novel Asynchronous ADC Architecture
LEVEL BASED SAMPLING FOR ENERGY CONSERVATION IN LARGE NETWORKS
A Level-Crossing Flash Asynchronous Analog-to-Digital Converter
Weight functions for signal reconstruction based on level crossings
Adaptive Rate Filtering Technique Based on the Level Crossing Sampling
Adaptive Level—Crossing Sampling Based DSP Systems
A 0.8 V Asynchronous ADC for Energy Constrained Sensing Applications
Spline-based signal reconstruction algorithm from multiple level crossing samples
A New Class of Asynchronous Analog-to-Digital Converters
Effects of time quantization and noise in level crossing sampling stabilization

**Here is some more background information on Analog to Digital converters.**

A 1-GS/s 6-bit 6.7-mW ADC
A Study of Folding and Interpolating ADC
Folding_ADCs_Tutorials
high speed ADC design
Investigation of a Parallel Resistorless ADC

**Here are some patents on the subject.**

4,291,299_Analog_to_digital_converter_using_timed
4,352,999_Zero_crossing_comparators_with_threshold
4,544,914_Asynchronously_controllable_successive_approximation
4,558,348_Digital_video_signal_processing_system_using
5,001,364_Threshold_crossing_detector
5,315,284_Asynchronous_digital_threshold_detector_
5,945,934_Tracking_analog_to_digital_converter
6,020,840_Method_and_apparatus_for_representing_waveform
6,492,929_Analogue_to_digital_converter_and_method
6,501,412_Analog_to_digital_converter_including_a_quantizers
6,667,707_Analog_to_digital_converter_with_asynchronous_ability
6,720,901_Interpolation_circuit_having_a_conversio2
6,850,180_SelfTimed_ADC
6,965,338_Cascade_A_D_converter
7,133,791_Two_mean_level_crossing_time_interval

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