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A New Class of Asynchronous Analog-to-Digital Converters

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This work is a contribution to a drastic change in standard signal processing chains: Analog-to-Digital Converters (ADCs), digital processing circuits, Digital-to-Analog Converters (DACs)… Integrated Smart Devices and Communicating Objects are the important applications targeted by this study. The main objective is to reduce their power consumption by one or two orders of magnitude, by completely rethinking their architectures and the associated signal processing theory.

In this context, we present a new class of ADCs, based on an irregular sampling of the input analog signal to process (level-crossing sampling), and on an asynchronous implementation (without any global clock). Fixed quantization levels are disposed along the input dynamic of the converter, a sample is taken and processed only when the signal crosses one of them. Its amplitude is then perfectly known (it is the one of the corresponding crossed level), and its time instant is quantized according to the resolution of a timer, the purpose of which is only to date the samples. Of course, the occurrences of samples depend on the signal amplitude variations: this sampling scheme removes the conversion of redundant samples or samples without any relevant information when the analog signal is quiet. Therefore, it leads to a compression of the digital samples and a reduction of the activity of the circuit.

The principle of this asynchronous A/D conversion is the dual case of Nyquist ADCs where the time instants are perfectly known and where the amplitude of samples is quantized. It leads to a completely different theory concerning the Signal-to-Noise Ratio (SNR) and the analog signal reconstruction. Hence a new design method has been elaborated: given an Effective Number Of Bits (ENOB) and the characteristics of the input analog signal to process (statistical properties and power spectral density), it determines the design parameters of the asynchronous ADC. It is shown that this method leads to a significant reduction in terms of hardware complexity and power consumption.

The asynchronous ADC has been designed, in a 0.18µm CMOS technology from STMicroelectronics, for a speech application, according to our design method. A 3-stage, micropipelined architecture, and a 4-phase protocol have been chosen for its implementation. The difference with classical pipelined circuits is that the data path part is here composed of digital and analog blocks (comparators, DAC…). Electrical simulations of the whole converter have been processed to determine its Factor of Merit (FoM). Comparisons with recent publications concerning any architecture (Flash, Successive Approximations…) and any application (high speed, low-power…) of Nyquist ADCs prove that the FoM of the asynchronous converter is improved by more than one order of magnitude. Moreover a significant reduction of the electromagnetic emissions is achieved, and each digital sample respects the targeted SNR, even if metastability occurs during the time quantization process.

We proved that such a converter can successfully be used in a classical Nyquist signal processing chain. In this case, the irregular stream of data must be re-sampled in a regular way. Nevertheless, the targeted objective is to directly use the irregular sampled data to process digital operations such as detection, filtering… This solution is now under investigation in our research team in order to have a fully asynchronous system, only piloted by the input signal. We believe it is one of the most promising approaches to make a significant step in the power consumption reduction of integrated mixed signal circuits.

FURTHER READING

Click any one of the following links to be taken to a website which contains the following documents.

The following are some recent examples of Asynchronous ADC activity off the web.

6 bit Asynchronous December 2006
Asynchronous ADC In CAD Mentor Graphics
Asynchronous Data Processing System
ASYNCHRONOUS PARALLEL RESISTORLESS ADC
Flash Asynchronous Analog-to-Digital Converter
Novel Asynchronous ADC Architecture
LEVEL BASED SAMPLING FOR ENERGY CONSERVATION IN LARGE NETWORKS
A Level-Crossing Flash Asynchronous Analog-to-Digital Converter
Weight functions for signal reconstruction based on level crossings
Adaptive Rate Filtering Technique Based on the Level Crossing Sampling
Adaptive Level—Crossing Sampling Based DSP Systems
A 0.8 V Asynchronous ADC for Energy Constrained Sensing Applications
Spline-based signal reconstruction algorithm from multiple level crossing samples
A New Class of Asynchronous Analog-to-Digital Converters
Effects of time quantization and noise in level crossing sampling stabilization

Here is some more background information on Analog to Digital converters.

A 1-GS/s 6-bit 6.7-mW ADC
A Study of Folding and Interpolating ADC
Folding_ADCs_Tutorials
high speed ADC design
Investigation of a Parallel Resistorless ADC

Here are some patents on the subject.

4,291,299_Analog_to_digital_converter_using_timed
4,352,999_Zero_crossing_comparators_with_threshold
4,544,914_Asynchronously_controllable_successive_approximation
4,558,348_Digital_video_signal_processing_system_using
5,001,364_Threshold_crossing_detector
5,315,284_Asynchronous_digital_threshold_detector_
5,945,934_Tracking_analog_to_digital_converter
6,020,840_Method_and_apparatus_for_representing_waveform
6,492,929_Analogue_to_digital_converter_and_method
6,501,412_Analog_to_digital_converter_including_a_quantizers
6,667,707_Analog_to_digital_converter_with_asynchronous_ability
6,720,901_Interpolation_circuit_having_a_conversio2
6,850,180_SelfTimed_ADC
6,965,338_Cascade_A_D_converter
7,133,791_Two_mean_level_crossing_time_interval

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