Jurnal Teknologi, 40(D) Jun. 2004: 59–76

A BIDIRECTIONAL UPS INVERTER UTILISING HIGH FREQUENCY CENTER-TAPPED TRANSFORMER

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Abstract. A new variation of transformer-isolated inverter for UPS application is proposed. It is basically similar to the circuit proposed by Koutroulis with the following modifications: 1) a modified modulation technique for the HF PWM inverter stage and 2) replacing the full bridge active rectifier with a center-tapped active rectifier. With these modifications, the switches count is reduced, and expectedly, the efficiency is increased. Furthermore, the modified PWM technique will ensure that the transformer can be utilised near to its full potential. This is due to the absence of the low frequency component that can result in transformer saturation. The paper will detail the design considerations for the proposed topology. It will primarily focus on the power circuit, modulation method, and the high frequency transformer design. To prove the concept, a 1-kW prototype inverter was built and tested.

Keywords: Inverter, bidirectional, high frequency transformer, pulse width modulation

1.0 INTRODUCTION

Transformer-isolated inverter is a mandatory requirement for uninterruptible power supplies (UPS). This is due to the fact that UPS is generally supplied by low voltage batteries and connected to the utility mains. The main function of the transformer is to step-up the output voltage to the required mains voltage. The second function is to provide the required electrical isolation for the inverter.

There has been immense interest on reducing the size of these transformers using various inverter topologies. This is because the transformer represents a substantial portion of the inverter's weight and cost. Several approaches to reduce the size of the transformer have been reported in literature over several decades [1–3]. They can be broadly grouped into two-categories: (1) utilising the 'line-frequency (50 Hz)' transformer and (2) using the 'high-frequency-link' transformer. Each method presents their own challenges and problems, alongside with their tangible benefits.

In this paper, we propose a high efficiency and compact bidirectional HF link inverter using center-tapped high frequency transformer. With this topology, fewer switches are used, thus conduction and switching losses are expected to be lower. In addition we implement a modified modulation technique for the PWM bridge that allows for more efficient utilisation of the transformer. The proposed method results in simpler hardware implementation.

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2.0 TRANSFORMER ISOLATED INVERTER TOPOLOGIES

The line-frequency transformer inverter is shown in Figure 1. It utilises the 50 Hz transformer for isolation and voltage stepped-up/down. This circuit is very attractive due to its simplicity and ruggedness. It requires minimum number of power switches and therefore, exhibits low conduction and switching losses. Furthermore, it is inherently bidirectional, i.e. the power can flow from source to load and vice versa. The reverse power flow is accomplished by the diode which is placed anti-parallel to the main power switch.

Despite its simplicity and inherent bidirectional capability, there is one obvious drawback of this topology which is the 50 Hz transformer. This component is very bulky, and expensive. It constitutes over 60% of the inverter's weight and space, and a substantial fraction of the overall cost. Regardless of the PWM modulation method employed on the inverter, the size of the transformer remains. It is of great interest to reduce the transformer size, but given the same topology, the task is impossible.

Recently, substantial work is carried out to use high frequency (HF) transformer link dc/ac inverter as an alternative to the conventional type. Compared to the latter, the HF link inverter offers significant advantages in terms of compactness, weight, and cost. By utilising high frequency transformer, the converter size and weight can be drastically reduced.

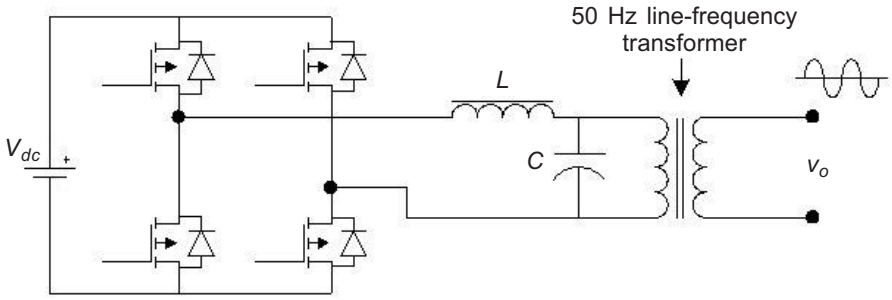


Figure 1 'Line-frequency' inverter

Numerous types of bidirectional high frequency link inverters have been suggested by researchers and are widely publicised elsewhere. However, the two well-known survivors are the 'cycloconverter' and the 'dc-dc converter' types. The cycloconverter HF link inverter, originally suggested by Matsui [2], is shown in Figure 2. The main advantage of this topology is that it requires only two conversion stages, namely the HF square-wave bridge and the cycloconverter circuit. The major disadvantage is that all the (twelve) power switches operate at high frequency, resulting in appreciable switching losses. Furthermore, the required switching scheme for the switches in the cycloconverter section is quite complex.

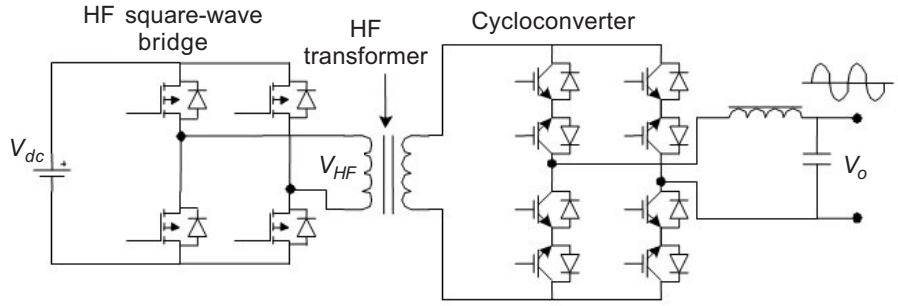


Figure 2 HF link inverter: the 'cycloconverter' type

The dc-dc converter type [3] consists of three power stages, i.e. the HF PWM bridge, active rectifier, and polarity-reversing bridge. The circuit configuration is shown in Figure 3. This topology is quite robust and is also capable of bidirectional power flow. However, it appears that the substantial power losses occur due to the forward conduction losses of the active filter's diodes. Another drawback of this topology is that the HF PWM bridge requires PWM modulated signal, which makes the transformer design less efficient.

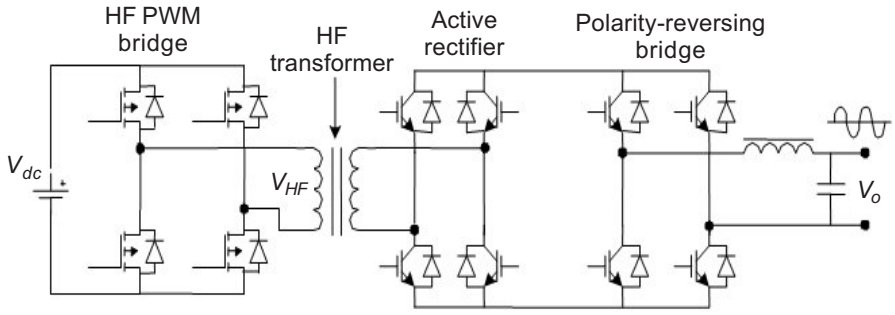


Figure 3 HF link inverter: the 'dc-dc converter' type

With regard to transformer capacity utilisation, the dc-dc type is marginally inferior to the cycloconverter. This is because the former requires PWM modulated signal at the HF bridge, while the cycloconverter type utilises square wave at 50% duty cycle. Since the PWM output voltage at the transformer primary has different pulse widths for each successive pulse, there is a possibility that the transformer may saturate, especially at low modulation index. This is attributed to the fact that a low frequency envelope is developed along with the high frequency components. Furthermore, the variable pulse widths of PWM modulation make the transformer design less efficient. It is difficult to determine the pulse width that is to be used in the design equation as pulses varies continuously over one complete mains cycle.

Nevertheless, the dc-dc type is very attractive due to the other features, namely low overall losses and simpler switching strategy at the secondary. Hence, we propose a modified dc-dc type with the following modifications:

1. HF PWM for the inverter bridge.
2. Using a center-tapped active rectifier (instead of a full bridge) at the secondary.

With these modifications, the switches count is reduced, and expectedly, the efficiency is increased. Furthermore, the modified PWM technique will ensure that the transformer can be utilised near to its full potential. This paper will detail the design considerations for the proposed topology. It will primarily focus on the power circuit, modulation method, and high frequency transformer design. To prove the concept, a 1-kW prototype inverter will be built and tested.

3.0 THE PROPOSED TOPOLOGY

The proposed topology for a single-phase inverter is shown in Figure 4. Basically, there are three conversion stages. At the first stage, the HF bridge converts the dc voltage into high frequency ac voltage using PWM scheme. Then, the power is transferred to the second stage via a center-tapped HF transformer. At this stage, the HF PWM waveform will be rectified using a center-tapped active rectifier. The active rectifier enables bidirectional power flow in the case of inductive load. For transfer of power from the source, the diodes are utilised. For reverse power flow, the power switches S3 and $\overline{S3}$ are turned-on. The opening and closure of the switches are accomplished by a control signal, v_s. It must also be noted that every switch of the active rectifier requires a snubber network to reduce the high voltage spike that results from the leakage inductor of the transformer secondary. The snubber circuit is not shown in the block diagram for simplicity.

The PWM waveform is then low-pass filtered to obtain the rectified fundamental component and remove the high order harmonics. The LC filter also helps to reduce the remaining spikes that are not completely clamped by the active rectifier snubbers. Finally,

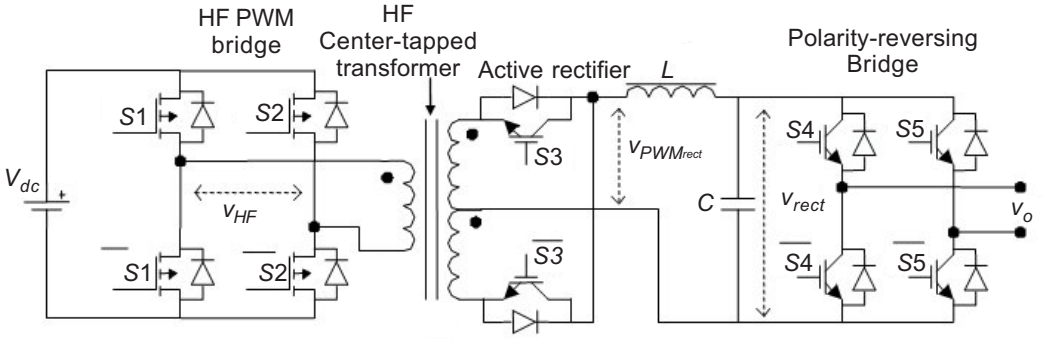


Figure 4 Block diagram of the proposed inverter

using a polarity-reversing bridge, the second half of the rectified sinusoidal voltage waveform is inverted at zero-crossing, and the sinusoidal output waveform is obtained. Note that the polarity-reversing bridge utilises only supply switching frequency switches.

Using this configuration, the total number of power switches is reduced into ten. From this, only six switches are switched at high frequency.

The timing diagrams for the key waveforms are illustrated in Figures 5 and 6. The rectified sinusoidal modulating signal is compared with the triangular carrier signal to produce the switching instants of the PWM waveform, v_{pwm}. This process is done digitally using a microcontroller. Using the HF bridge, the HF PWM waveform, v_{HF}, is produced at the primary side of the HF transformer. The stepped-up HF PWM voltage at the secondary side is then rectified by the active rectifier. The gate control signal of the active rectifier, v_s, shown in Figure 6, is used to control the power flow at the active rectifier stage. The produced output voltage waveform, $v_{PWMrect}$, is filtered using a low pass *LC* filter, and the rectified sinusoidal voltage waveform is obtained. Through polarity-reversing bridge, the ac sinusoidal output waveform is obtained. The gate control signal for polarity-reversing bridge is denoted as v_u.

The timing diagrams for the key waveforms are illustrated in Figure 5. The rectified sinusoidal modulating signal is compared with the triangular carrier signal to produce the switching instants of the PWM waveform. This process is done digitally using a microcontroller. Using the HF bridge, the HF PWM waveform, v_{HF}, is produced at the primary side of the HF transformer. The stepped-up HF PWM voltage at the

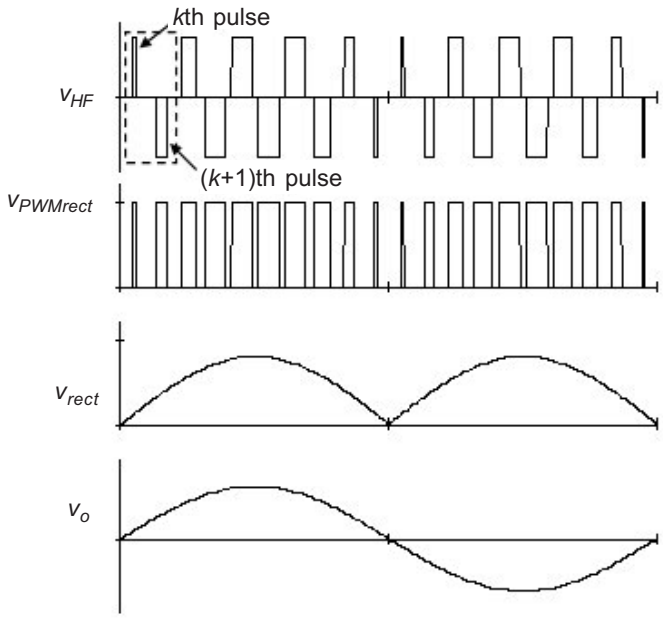


Figure 5 Principal waveforms at different stages of the dc/ac conversion

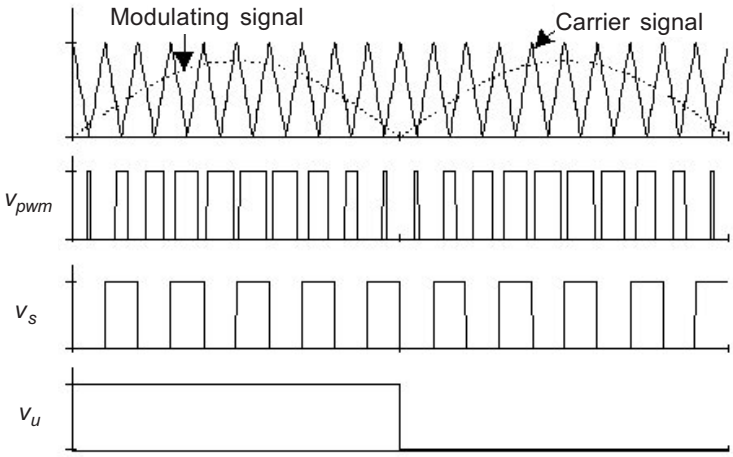


Figure 6 Modulating technique and signal generated by microcontroller

secondary side is then rectified by the active rectifier. The gate control signal of the active rectifier, v_s, shown in Figure 6, is used to control the power flow at the active filter stage. The produced output voltage waveform, $v_{PWMrect}$, is filtered using a low pass *LC* filter, and the rectified sinusoidal voltage waveform is obtained. Through polarity-reversing bridge, the second half of the rectified sinusoidal voltage waveform is inverted at zero-crossing, thus producing the ac sinusoidal output waveform. The gate control signal for polarity-reversing bridge is denoted as v_u.

4.0 MODULATION METHOD

In this work, the modulation technique of the HF bridge is based on the symmetric regular sampling sinusoidal PWM. The derivation of the switching angles is accomplished using the volt-second equalization method, as illustrated in Figure 7. The PWM pulse width characterization is also shown in the same figure. Note that the modulating waveform is a rectified sinusoidal signal. The equation used to calculate the pulse width of the *k*th PWM for a given modulation index, M_I, and modulation ratio, m_f, is given as follows:

$$\delta_k = 4\delta_o M_I \sin \alpha_k \tag{1}$$

where $k = 1 \cdots \left(\frac{m_f}{2} \right)$

Using Equation (1), the rising and falling edges (i.e. the switching instants) of the *k*th pulse can be known. For the rising edge, the angle can be calculated as:

$$\alpha_{1k} = \alpha_k - \delta_k \tag{2}$$

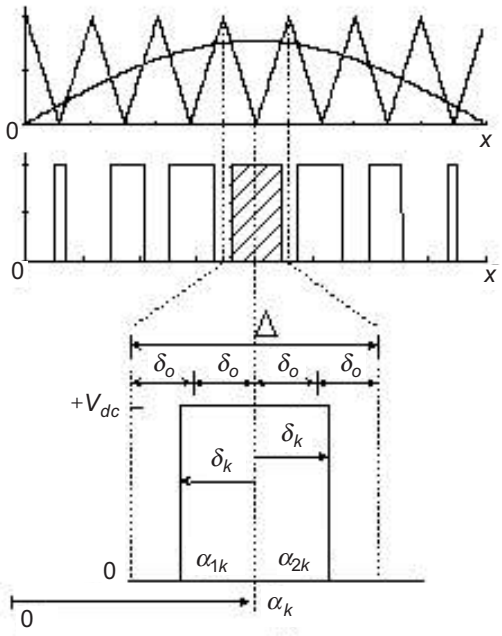


Figure 7 Volt-second modulation technique

For the falling edge,

$$\alpha_{2k} = \alpha_k + \delta_k \tag{3}$$

Looking back into Figure 5, it can be noticed that the widths for kth and (k+1)th pulses are not equal in v_{HF}. If the differences in the pulse widths are plotted from k=1 through m_f, it can be observed that a low frequency voltage envelope existed along with the high frequency component. This may results in transformer saturation, as the transformer is normally designed for high frequency operation. Alternatively, the transformer can be utilized below its rated capacity to avoid the possible saturation.

To overcome this problem, we propose the kth pulse width to be equalized to the (k+1)th. Using this approach, the use of dc blocking capacitance at primary side of transformer, as suggested in [3] can be avoided. Furthermore, the processing speed to calculate the pulse widths can be increased, with only $m_f/8$ pulses to be calculated in each cycle. The following equation is used for this purpose:

$$\delta_k = \delta_{(k+1)} = 4\delta_o M_I \sin(\alpha_{k'}) \tag{4}$$

where:

$$\alpha'_k = \frac{\alpha_k + \alpha_{k+1}}{2},\ k = 1,3,5\cdots\left(\frac{m_f}{2} - 1\right)$$

5.0 HARDWARE DESIGN

5.1 PWM Waveform Generation

The Siemen's C167 microcontroller has been chosen as the waveform generator for the PWM and other control signals in the circuit. It is a low cost, 16-bit fixed-point microcontroller, equipped with extensive on-chip peripherals to assist interfacing with other external components. Some of these peripherals are independent modules that require minimum intervention from the main CPU, thus freeing the latter to perform other tasks.

The PWM waveform generation is accomplished by the C1676 peripheral known as the PWM Module. Four PWM channels are available , which can be programmed separately for different types of PWM modes. In this work, the center aligned PWM mode, shown in Figure 8 has been selected as the gate signal for the HF bridge. The PWM signals generated by the microcontroller will then go through a series of external logic gates and become the input signals of gate drivers as shown in Figure 9.

5.2 Power and Driver Circuit

The HF bridge is constructed using the IRFP460 power MOSFET. It is a low $R_{ds(ON)}$ device with good switching capability. The active rectifier's switch is built using the IRG4PH40K IGBTs with discrete 20EFT10 fast recovery anti-parallel diodes. The rated

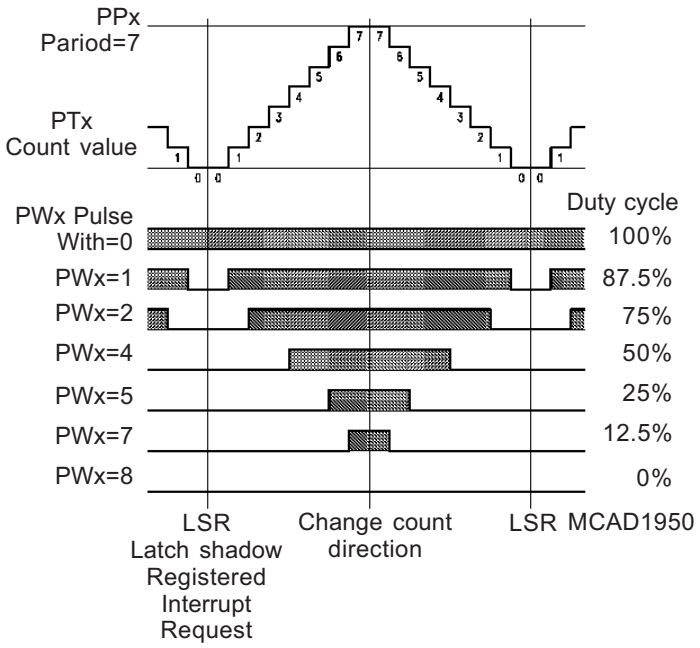


Figure 8 Center-aligned PWM mode using the C167 PWM module

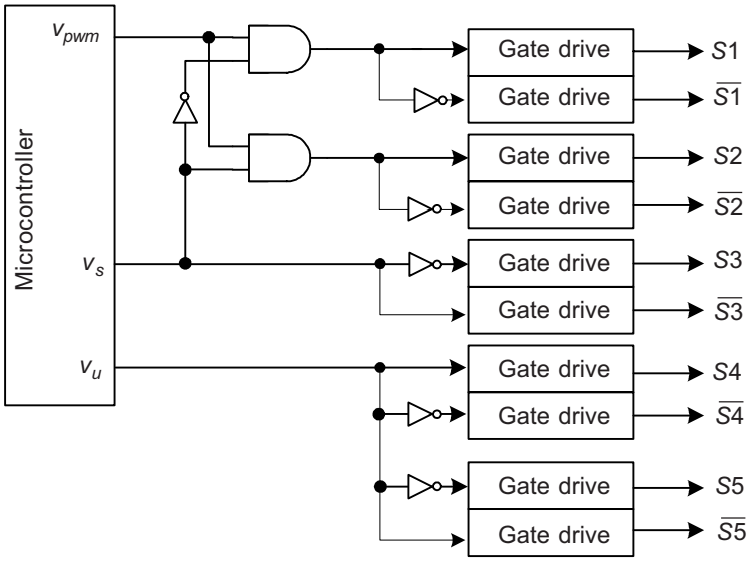


Figure 9 Interface between the microcontroller with the power switches

voltage for the diode is 1200V, in precaution to the possible voltage surge that may result from the transformer leakage inductance. An RC snubber network has been placed across the active rectifier's switch to reduce the surge voltage. The polarity-reversing bridge is constructed using SK25GB065 IGBT module. Since almost all the surge voltages have been filtered before entering polarity-reversing bridge, the chosen power switches are only rated at 600 V. Using low voltage IGBT, the forward conduction losses can be minimized.

Each power transistor is driven by a Hewlett Packard gate driver chip, HCPL 3120. This chip has a built-in opto-coupler, mid-stage amplifier, and output-stage (power) amplifier. The 'all-in-one chip' solution has simplified the gate-driver to power transistor interface greatly. To obtain the isolated power supplies for the top and bottom gate-driver of an inverter leg, a transformer-isolated DC-DC converter is designed. The heart of the DC-DC converter is the SG3524 pulse generator, while the isolation is performed by the ET12 Ferroxcube high frequency miniature transformer. Using a single 9 V battery, all the gate-drivers are isolated and are individually powered to +15 Volts (to turn on the switch) and –15 V (to turn off).

A dead-time compensation scheme for the HF bridge is incorporated into the software. The waveform for the compensation is shown in Figure 10. Note that t_d is the amount of dead-time taken away from the pulse width.

5.3 Power Transformer Design

As has been emphasised throughout the discussion, the main feature of the high frequency link inverter is transformer size reduction. To achieve this goal, typically

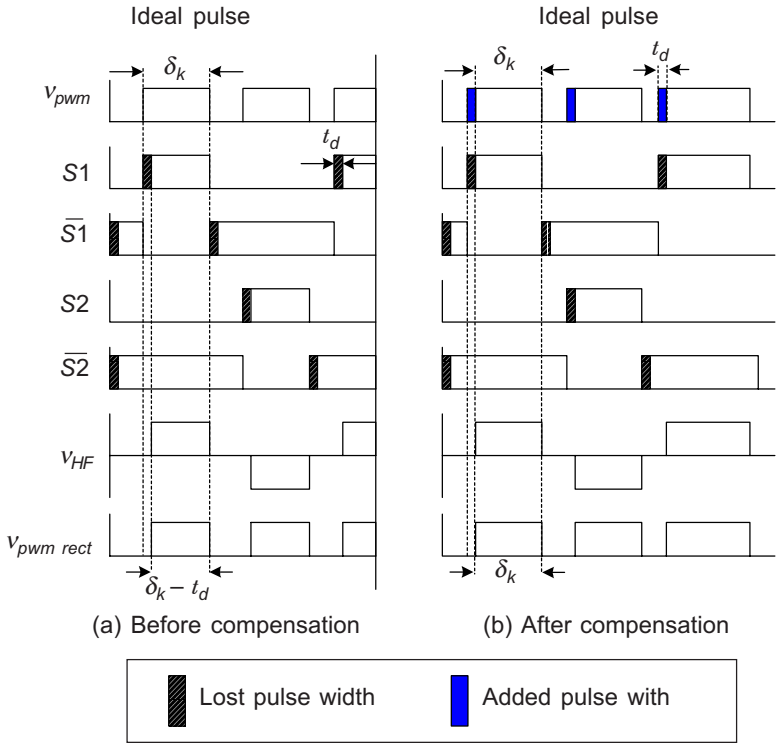


Figure 10 Dead-time compensation scheme for the HF bridge

ferrite cores are selected due to its low core loss when operated at high frequency. Ferrite core has a simple structure, good winding coupling, and easy to construct. It is also significantly lower in cost.

The procedure of designing a transformer inevitably started by choosing the size of the core. This mainly depends on the power capacity required for the transformer. The relationship between the power capacity (P_o) and the effective core area, A_e, and core windows area, A_c, at a given switching frequency (f) is given as [4].

$$A_e A_c = \left(\frac{3.39(10^2) D_{cma}}{B_{max} f} \right) P_o \tag{5}$$

$$\text{and } B_{max} \cong \frac{B_{sat}}{2} \tag{6}$$

Where B_{sat} and D_{cma} is the saturation flux density and diameter in circular mils, respectively. Subsequently, the number of primary winding, N_p can be determined by:

$$N_p = \frac{10^5 V_p D}{4 B_{max} A_e f} \tag{7}$$

In equation (7), D is the duty ratio, which varies from 0 to 0.5. The secondary turns ratio can be calculated as:

$$V_s = \eta V_p \frac{N_s}{N_p} \tag{8}$$

V_s and V_p are the primary and secondary voltage, respectively, while η is the assumed efficiency of the transformer. Design example of the transformer used in this work is attached in Appendix A.

The designed high frequency transformer with power rating of 1000 VA has an approximate size of 2.5 in × 2.5 in and weighted 500 g. For comparison, a 50 Hz line-frequency transformer of the same rating is 6 in × 6 in and has a weight of approximately 7 kg. Figure 11 shows the finished prototype inverter. The total weight of the inverter is about 1.4 kg. Apart from the power transformer and inductor, substantial portion of the weight is contributed by the heat sink and cooling fan.

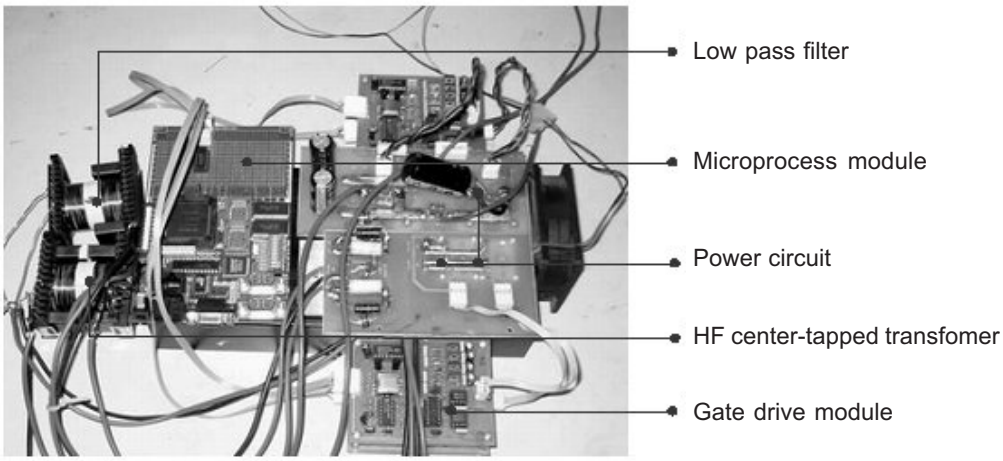


Figure 11 Photograph of the prototype inverter

6.0 EXPERIMENTAL RESULTS AND DISCUSSIONS

Laboratory experiments have been carried out to verify the viability of the proposed inverter. The specifications of the inverter are as follows:

- Input voltage ranged from 60 to 110 V.
- Sinusoidal output voltage 220-250 V_{rms}, 50 Hz.
- Maximum output power of 1 kW.

The output waveforms for resistive load and inductive load are shown in Figure 12 and Figure 13 respectively. From the latter, it can be observed that the inverter is

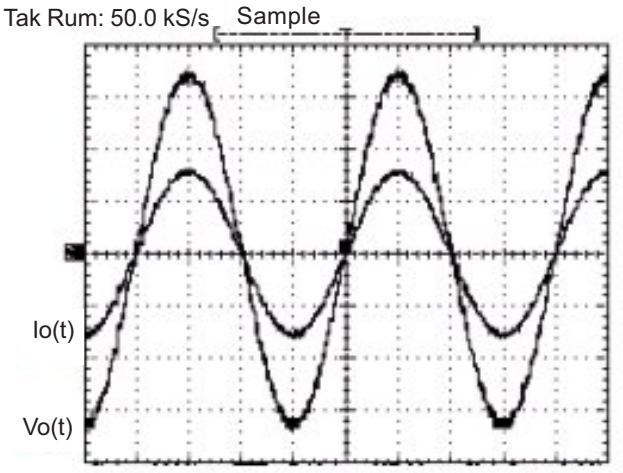


Figure 12 Output voltage and current with resistive load output power = 1050W
Scales: output voltage 100 V/div, output current 4 A/div, time 5 ms/div

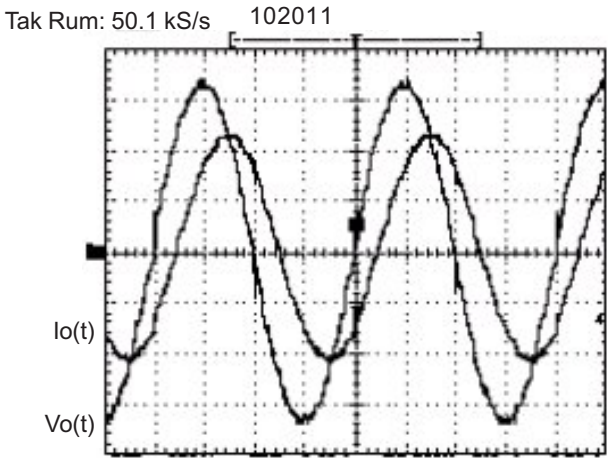


Figure 13 Output voltage and current with inductive load. Real power = 511.7 W; power factor = 0.7
Scales: output voltage 100 V/div, output current 2 A/div, time 5 ms/div

capable of carrying bidirectional power flow. To measure the harmonics of the inverter output, the LC filter is disconnected. The frequency spectrum is shown in Figure 14. The main harmonic components exist at and around the multiples of switching frequency, which are m_f, $2m_f$, $3m_f$, and $4m_f$. This is to be expected because the modulation technique is basically based on sinusoidal PWM.

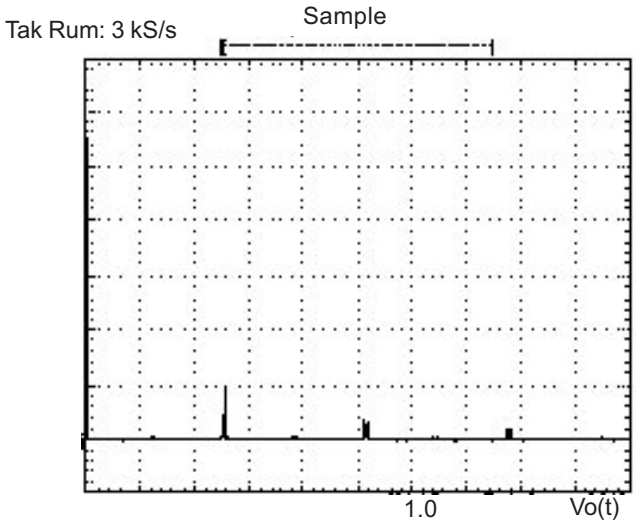
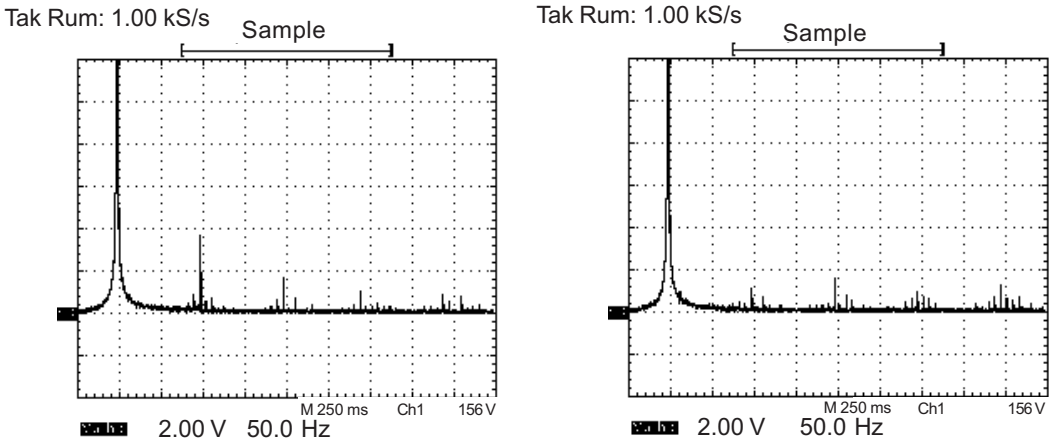


Figure 14 Frequency spectrum of the output voltage without *LC* filter. Parameters: $M_I = 1.0$, $m_f = 650$
Scales: spectra 40 V/div, frequency 12.5 kHz/div

Figures 15(a) and (b) show the spectra of the filtered output voltage before and after dead-time compensation, respectively. The chosen dead-time to the pulse period ratio (t_d/T_s) is 0.1. As can be seen, most of the low order harmonics (3^{rd}, 5^{th}, etc) that resulted from the dead time effect is reduced. Figure 16 indicates the effectiveness of the dead-time compensation technique employed on the inverter. Even as td/Ts is increased to a large value, i.e. 0.25, the compensation scheme works quite well.



(a) Output spectra before dead-time compensation

(b) Output spectra after dead-time compensation

Figure 15 Frequency spectrum of the filtered output voltage before and after dead-time compensation
Scales: spectra 2 V/div, frequency 50 Hz/div

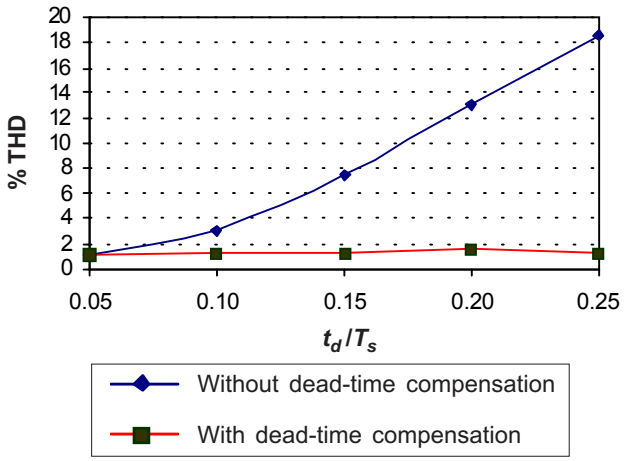


Figure 16 Effectiveness of the dead-time compensation for various values of t_d/T_s

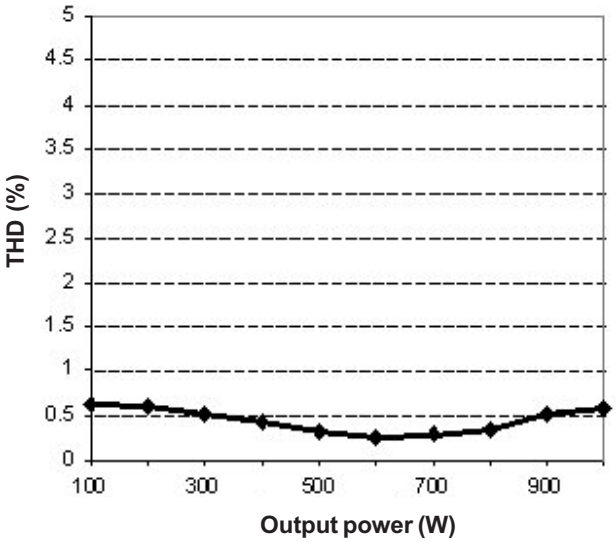


Figure 17 Output voltage THD versus output power

The measured output voltage THD for resistive load is shown in Figure 17. It can be seen that the output voltage THD is less than 1% over the entire output power, with the average value approximately 0.5%. This can be attributed to the effectiveness of the dead-time compensation scheme. The measured values are much less than the 5% level, the industrial standard for UPS systems. The minimum value of THD (0.35%) is obtained when the inverter operates at output power 600 – 700 W.

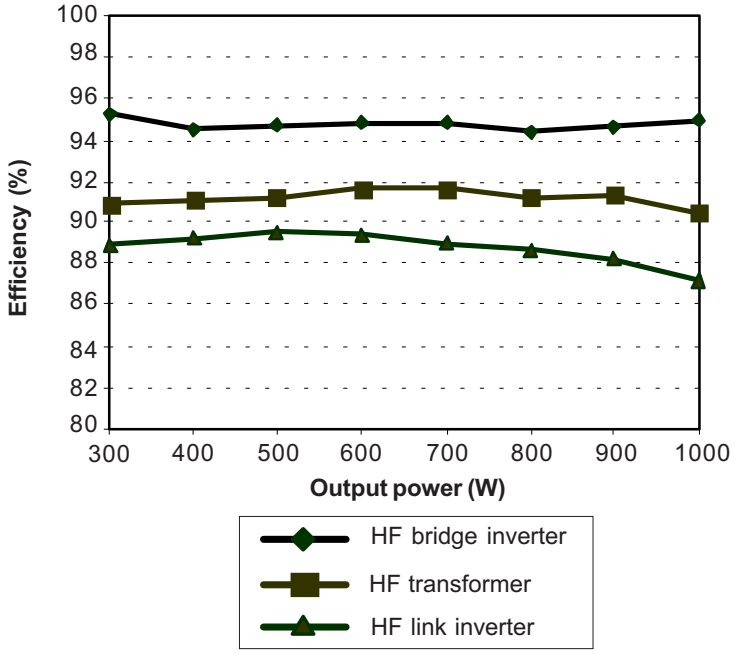


Figure 18 Efficiency vs output power of the inverter

Figure 18 shows the measured efficiency of the inverter at each conversion stages, against the output power. The average efficiency of HF bridge is 95%, while the mean efficiency of the HF transformer is 91%. The average total efficiency of the inverter is around 88%. Note that when the output power increases to 1 kW, the average efficiency decreases to the minimum level of 87%. This can be attributed to the increased losses of power switches and transformer at high current operation.

7.0 CONCLUSION

A compact HF link inverter that enables bidirectional power flow using center-tapped transformer has been described. The use of center-tapped active rectifier requires less power switches, thus increases the overall system efficiency. The modified digital PWM technique allows better utilisation of the transformer capacity. It also increases the switching angle calculation processing speed. A 1kW prototype is constructed to study the viability of the inverter. It was found that the output voltage has a very low THD with an average efficiency of 88%.

ACKNOWLEDGEMENTS

The authors wish to acknowledge the Ministry of Science, Technology and the Environmental (MOSTE), Malaysia, for the financial funding of this project.

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APPENDIX A

Transformer Design Example

In this work, the designed high frequency transformer has to meet the following specifications:

- input voltage range, V_{max} = 67.5 V – 100 V.
- switching frequency, f = 17 kHz.
- maximum input power, = 1000 W.

The design procedure of the transformer are summarised as follows:

1. Selection of core geometry and core material.
   For the power and frequency ratings, an EE geometry with ferrite grade material 3C90 from Ferroxcube is selected.

2. Selection of flux density, B_{max}.
   Information from data sheets show that ferrite with grade 3C90 has the saturated flux density, B_{sat} of 3500 Gauss at 100C. Thus,

$$B_{max} \cong \frac{B_{sat}}{2} = \frac{3500}{2} = 1700\,G$$

3. Determination of conductor size.
   Calculated current density is 500 ampere per circular mils. Thus the required size of conductor would be 7120 circular mil. The most appropriate diameter for a conductor to operate at frequency of 17 kHz is approximately 1.06 mm, taking into account the conductor skin effect. Alternatively, five conductors sized awg-18 (in parallel) can be used to obtain the equivalent area of a conductor sized awg-12.

4. Determination of core and bobbin size.
To calculate the core dimension, Equation (5) is used. The selected core should have a greater size than the calculated value to ensure that all winding fitted well into the core. Hence:

$$A_e A_c = \left(\frac{3.39(10^2) D_{cma}}{B_{max} f} \right) P_o = \frac{3.39(10^2)500}{170 \times 10G(17 \times 10^3 \text{ Hz})}(1000\ W) = 5.87\,\text{cm}^4$$

Core and bobbin 3C90 ETD54 have been chosen with $A_e A_c$ value of 8.848 cm^4.

5. Calculation of the primary turns:
Using Equation (8), the secondary turns can be estimated as:

$$N_p = \frac{10^5 V_{dc} D}{2 B_{max} A_e f} = \frac{10^5 (66.7 \text{ V})(0.5)}{2(1700G)(2.8 \text{ cm}^2)(17 \text{ kHz})} = 20.6 \text{ turn}$$

6. Calculation for Secondary turns:
Calculation is done using Equation (11). However, the voltage drop of the power switch and certain circuit parameters should be taken into consideration. These include:

- The IGBT saturated voltage: $V_{ce} = 1.8$ V;
- MOSFET voltage drop: $I_{ds} \times R_{ds} = 14.24 \text{ A} \times 0.085$;
- Diode forward biased voltage: $V_F = 1.2$ V;
- Estimated transformer's efficiency: $\eta = 80\%$;
- The minimum modulation index, $p = 0.7$;

Using these values, the minimum input voltage of primary winding can be estimated as:

$$V_p = V_{min} - 2(I_{ds} R_{ds}) = 67.5 - 2(14.24 \times 0.085\ \Omega) = 65.1 \text{ V}$$

The output sine wave voltage,

$$V_{out} = 240 + V_d + V_{ce} = 240 + 2 \times 1.8 \text{ V} + 1.8 \text{ V} = 245.4 \text{ V}$$

Hence the secondary voltage is:

$$V_s = \frac{V_{out}\sqrt{2}}{p} = \frac{245.4 \times \sqrt{2}}{0.7} = 495.8 \cong 496 \text{ V}$$

The secondary turns can be calculated as:

$$N_s = \frac{\eta V_s N_p}{V_p} = \frac{0.8 \times 496 \text{ V} \times 21}{65.1} = 128 \text{ winding}$$

FURTHER READING

Click any one of the following links to be taken to a website which contains the following documents.

There appears to be a lot of recent patent activity in the area of building "bridgeless PFC convertors". The following are some of the patents.

11_584_983_Method_and_apparatus_for_high_efficieny_rectifier
11_204_307_AC_to_DC_power_supply_with_PF
11_302_544_Simple_partial_switching_power_factor_correction
11_474_712_BRIDGELESS_BI_DIRECTIONAL_FORWARD_TYPE_CONVERTER
11_480_004_High_efficiency_power_converter_system
11_706_645_AC_to_DC_voltage_converter_as_power_supply
12_401_983_BRIDGELESS_PFC_CIRCUIT_FOR_CRM
12_798_682_Bridgeless_PFC_converter

3295043_MASSEY_D_C__TO_D_C__REGULATED_CONVERTER
4183079_DC_AC_inverter
4523266_AC_to_DC_conversion_system
4943902_AC_to_DC_power_converter_and_method
5570276_Switching_converter_with_open_loop_input_regulation
5815380_Switching_converter_with_open_loop_Primary_regulation
5815384_Transformer_uses_bi_directional_synch_Rectifiers
6115267_AC_DC_converter_with_no_input_rectifiers
6157182_DC_DC_converter_with_multiple_operating_modes
6608522_DC_to_DC_converter_providing_stable_operation
7250742_Digital_control_of_bridgeless_power_factor_correction
7265591_CMOS_driver_with_minimum_shoot_through

And here is some more information for those who may be interested.

A BIDIRECTIONAL PWM THREE-PHASE STEP-DOWN RECTIFIER
A bidirectional, sinusoidal, high-frequency inverter
A DUAL INPUT BIDIRECTIONAL POWER CONVERTER
A new structure for bidirectional Power flow
BI-DIRECTIONAL INVERTER-CHARGER
Bi-directional single-phase half-bridge rectifier for power quality
BiDirectional Converter
Bidirectional_UP_Inverter
Synthesis of Input-Rectifierless AC/DC

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