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(54) SIMPLE PARTIAL SWITCHING POWER FACTOR CORRECTION CIRCUIT

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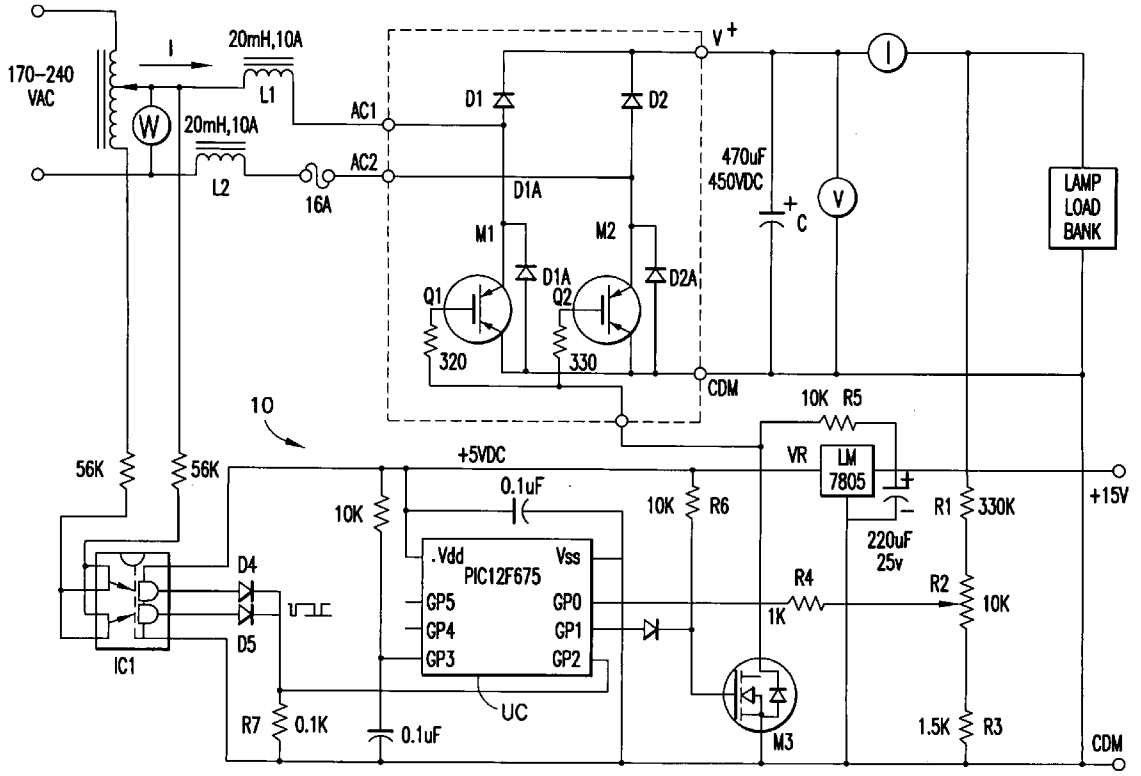
(57) **ABSTRACT**

A boost type power supply circuit for providing a DC output voltage comprising first and second semiconductor switches coupled between respective input lines and a common connection, an AC input voltage from an AC source being supplied across the input lines; first and second diodes coupled in series with respective ones of the switches; third and fourth diodes coupled across respective ones of the switches in a free-wheeling relationship with the switches, an inductance coupled in at least one of the input lines; a controller for controlling the conduction times of the switches by providing a pulse width and phase modulated control signal to each of the switches; whereby the controller turns on at least one of the switches during a positive half cycle of the AC voltage to allow energy storage in the inductance and turns off the at least one switch to allow the energy stored in the inductance to be supplied to an attached load through one of the first and second diodes and one of the third or fourth diodes; and the controller turns on at least one of the switches during a negative half cycle of the AC voltage to allow energy storage in the inductance and turns off the at least one switch to allow the energy stored in the inductance to be supplied to the attached load through one of the first and second diodes and one of the third and fourth diodes; and wherein the controller determines an on-time and an off-time of a pulse of the pulse width modulated control signal during each half cycle of the AC voltage based on at least one input without requiring sensing of the input current from the AC source; the on-time and off-time of the pulse being controlled to regulate said output voltage and to provide power factor correction of said AC input voltage.



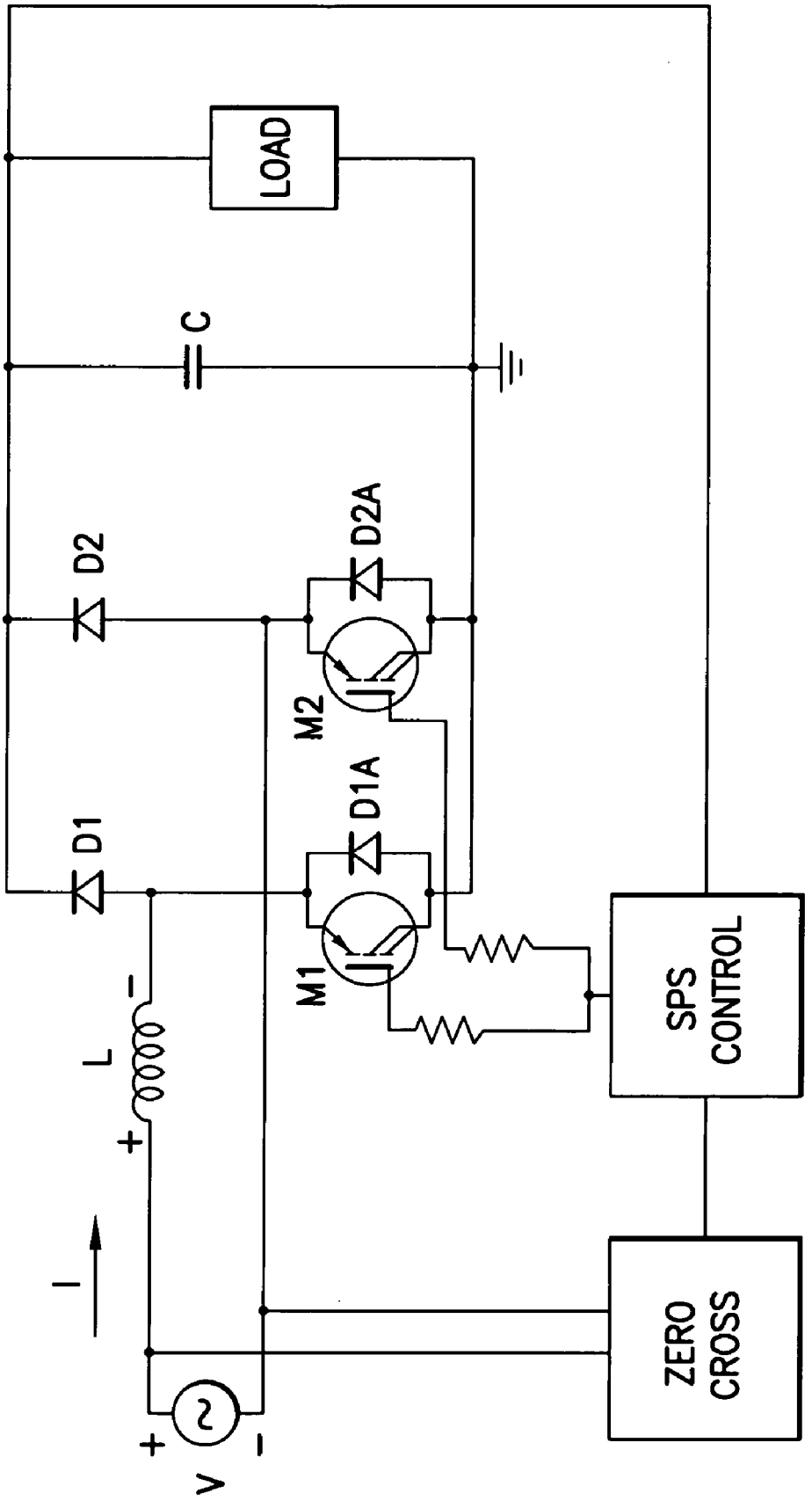


FIG. 1

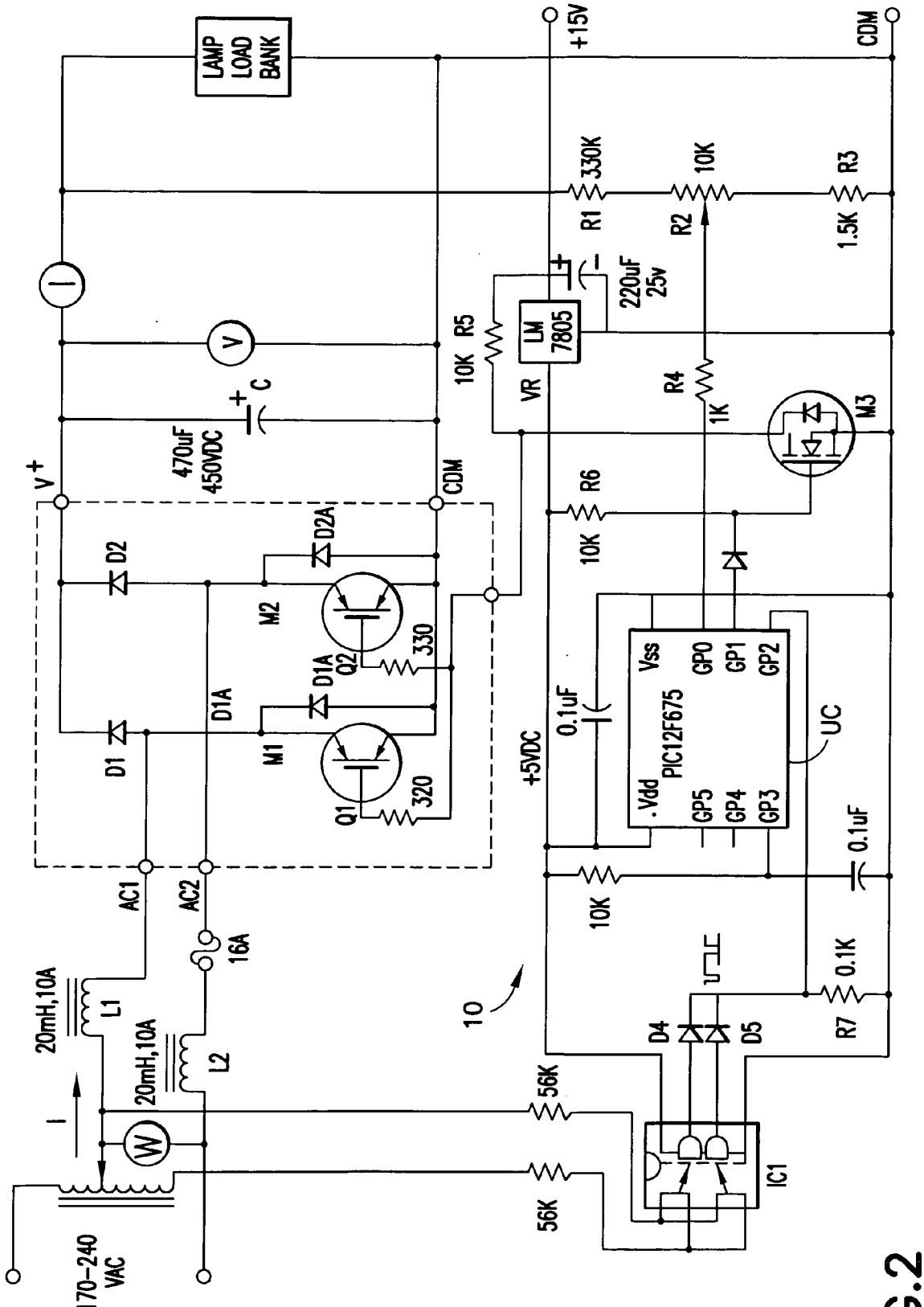

LAMP LOAD BANK
+15V
COM
330K
10K
R3
R1
R2
1.5K
220uF 25v
LM 7805
10K R5
VR
R4
1K
M3
470uF 450VDC
C
V+
COM
R6
10K
D2A
D2
M2
D1A
Q2
330
D1A
D1
M1
Q1
320
Vss
GP0
GP1
GP2
0.1uF
+5VDC
PIC12F675
UC
.Vdd
GP5
GP4
GP3
0.1uF
AC1
AC2
16A
10K
20mH,10A
L1
20mH,10A
L2
10
0.1K
R7
D4
D5
56K
I
W
IC1
56K
170-240 VAC

FIG.2

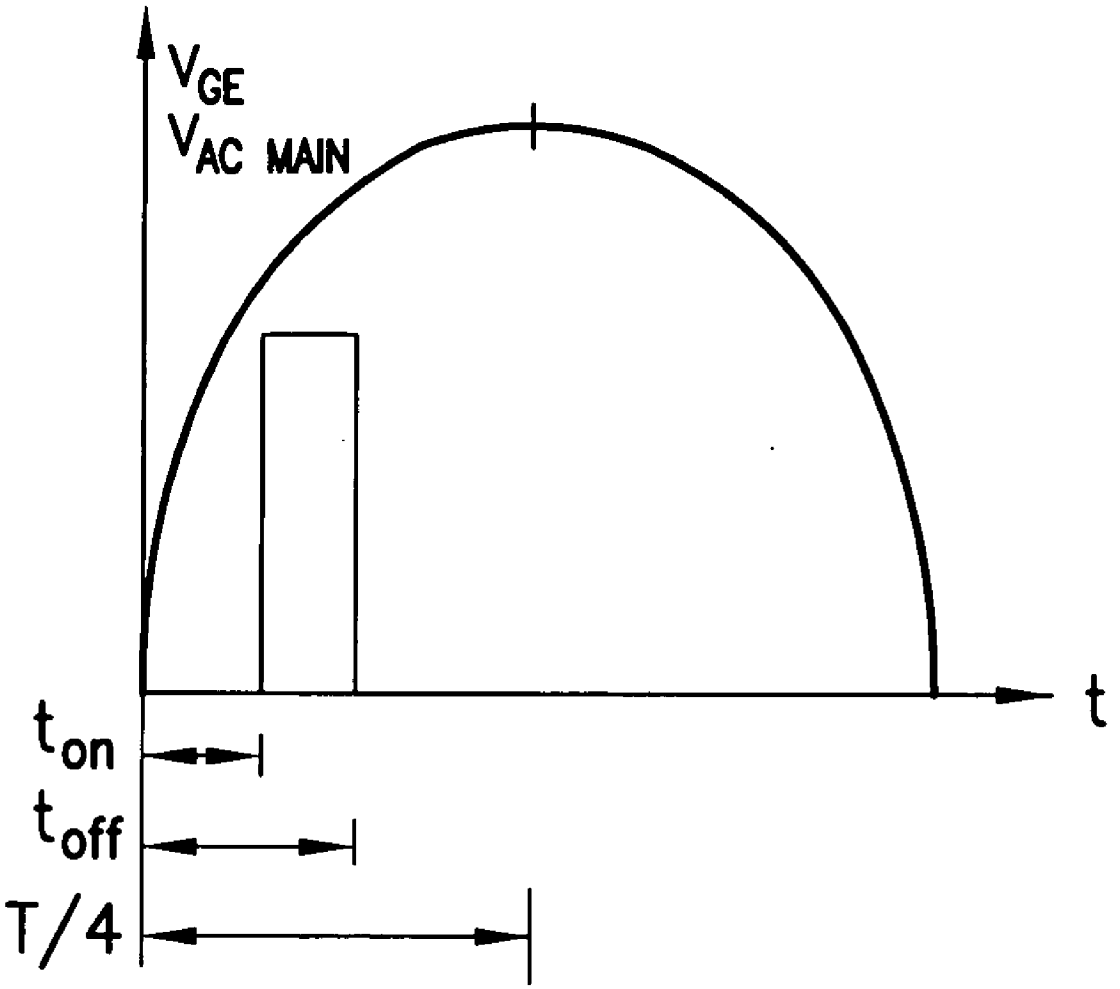


FIG.3

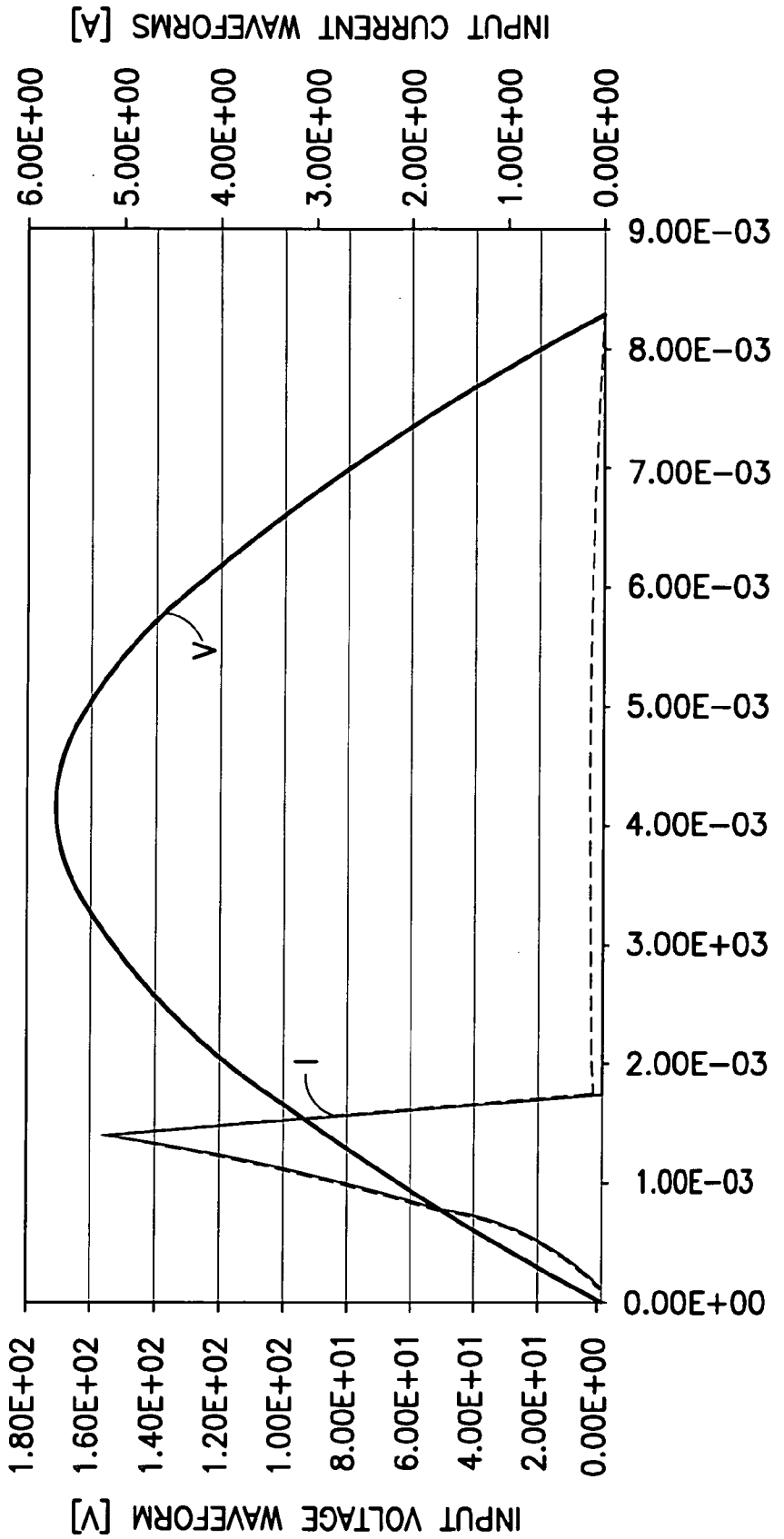

INPUT CURRENT WAVEFORMS [A]
6.00E+00
5.00E+00
4.00E+00
3.00E+00
2.00E+00
1.00E+00
0.00E+00
9.00E-03
8.00E-03
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E+03
2.00E-03
1.00E-03
0.00E+00
TIME [s]
V
I
1.80E+02
1.60E+02
1.40E+02
1.20E+02
1.00E+02
8.00E+01
6.00E+01
4.00E+01
2.00E+01
0.00E+00
INPUT VOLTAGE WAVEFORM [V]

FIG.3A

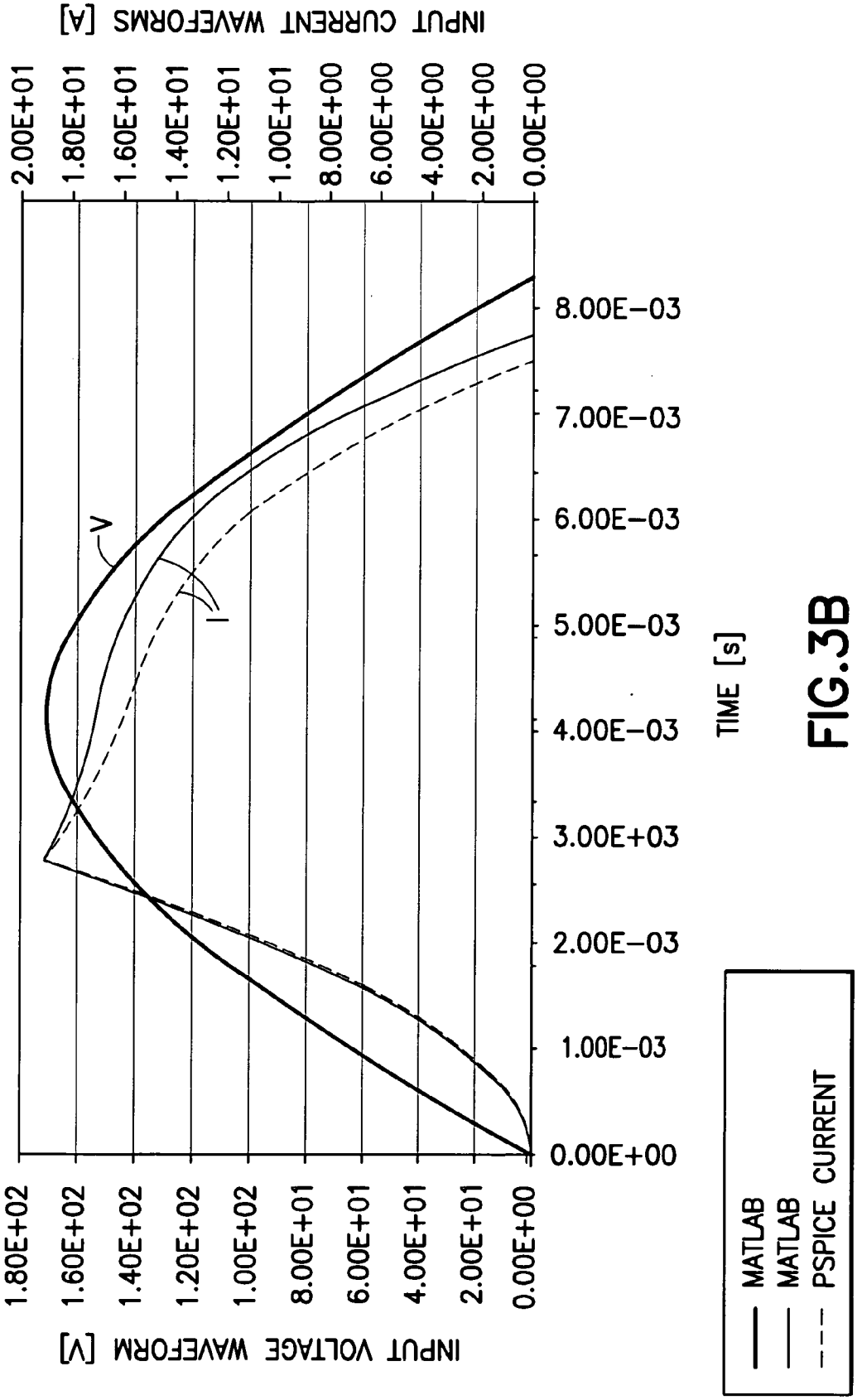

INPUT CURRENT WAVEFORMS [A]
2.00E+01
1.80E+01
1.60E+01
1.40E+01
1.20E+01
1.00E+01
8.00E+00
6.00E+00
4.00E+00
2.00E+00
0.00E+00
V
I
8.00E-03
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E+03
2.00E-03
1.00E-03
0.00E+00
TIME [s]
1.80E+02
1.60E+02
1.40E+02
1.20E+02
1.00E+02
8.00E+01
6.00E+01
4.00E+01
2.00E+01
0.00E+00
INPUT VOLTAGE WAVEFORM [V]
MATLAB
MATLAB
PSPICE CURRENT

FIG.3B

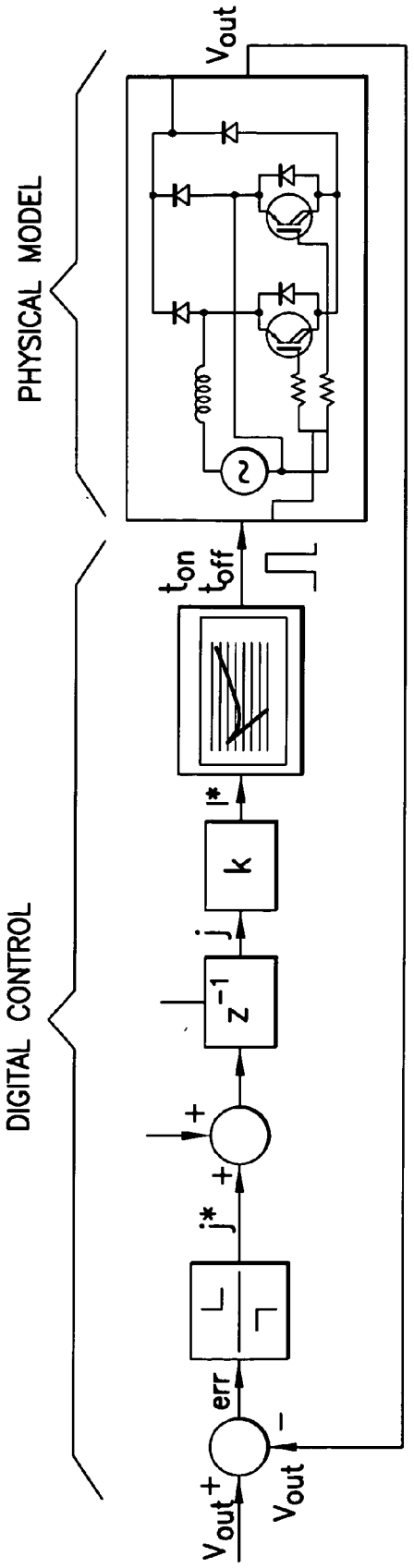

PHYSICAL MODEL
DIGITAL CONTROL
Vout
ton
toff
k
i*
j
z-1
j*
err
Vout+
Vout-

FIG.4

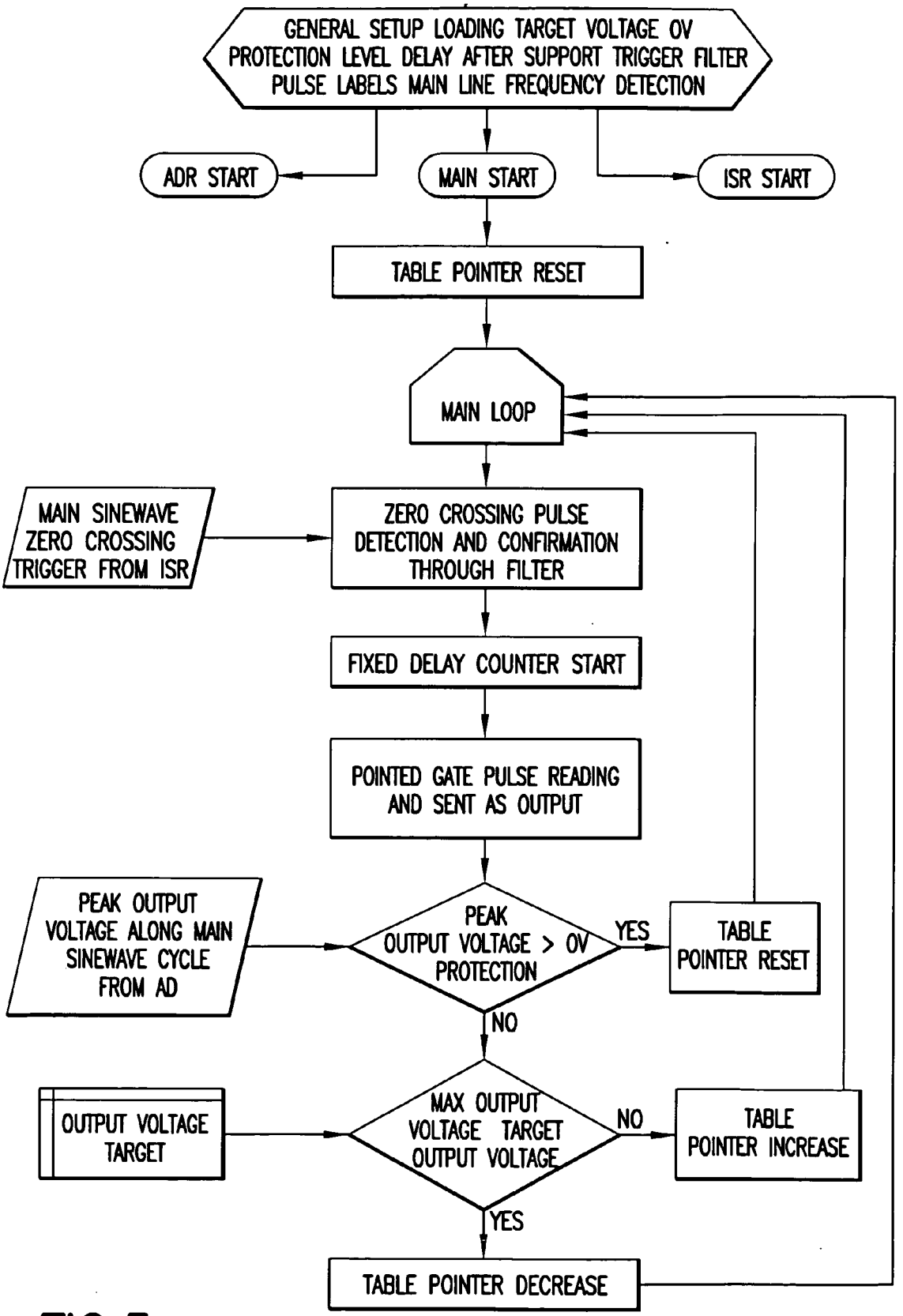

GENERAL SETUP LOADING TARGET VOLTAGE OV PROTECTION LEVEL DELAY AFTER SUPPORT TRIGGER FILTER PULSE LABELS MAIN LINE FREQUENCY DETECTION
ADR START
MAIN START
ISR START
TABLE POINTER RESET
MAIN LOOP
MAIN SINEWAVE ZERO CROSSING TRIGGER FROM ISR
ZERO CROSSING PULSE DETECTION AND CONFIRMATION THROUGH FILTER
FIXED DELAY COUNTER START
POINTED GATE PULSE READING AND SENT AS OUTPUT
PEAK OUTPUT VOLTAGE ALONG MAIN SINEWAVE CYCLE FROM AD
PEAK OUTPUT VOLTAGE > OV PROTECTION
YES
TABLE POINTER RESET
NO
OUTPUT VOLTAGE TARGET
MAX OUTPUT VOLTAGE TARGET OUTPUT VOLTAGE
NO
TABLE POINTER INCREASE
YES
TABLE POINTER DECREASE

FIG.5

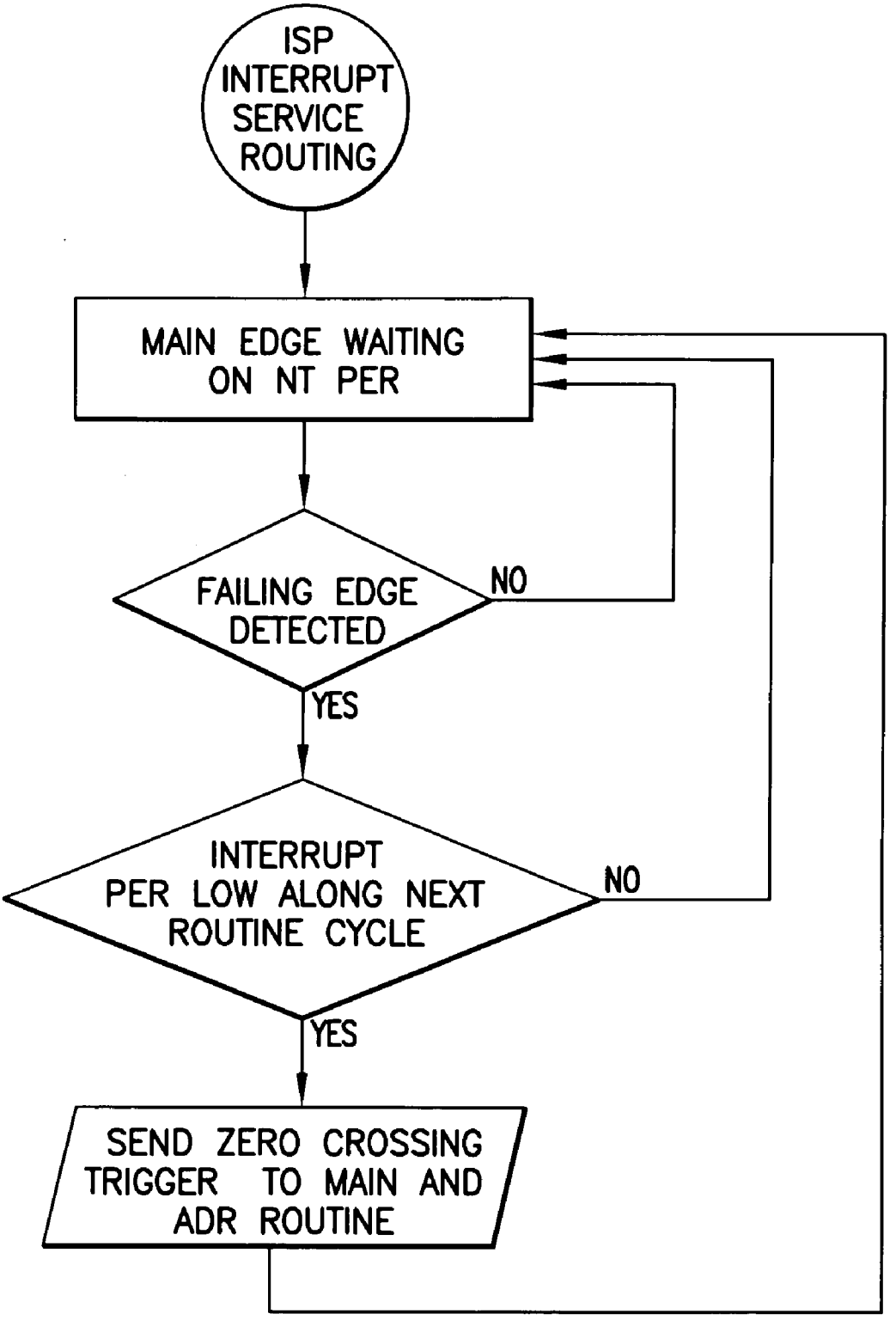

ISP
INTERRUPT
SERVICE
ROUTING
MAIN EDGE WAITING
ON NT PER
FAILING EDGE
DETECTED
NO
YES
INTERRUPT
PER LOW ALONG NEXT
ROUTINE CYCLE
NO
YES
SEND ZERO CROSSING
TRIGGER TO MAIN AND
ADR ROUTINE

FIG.6A

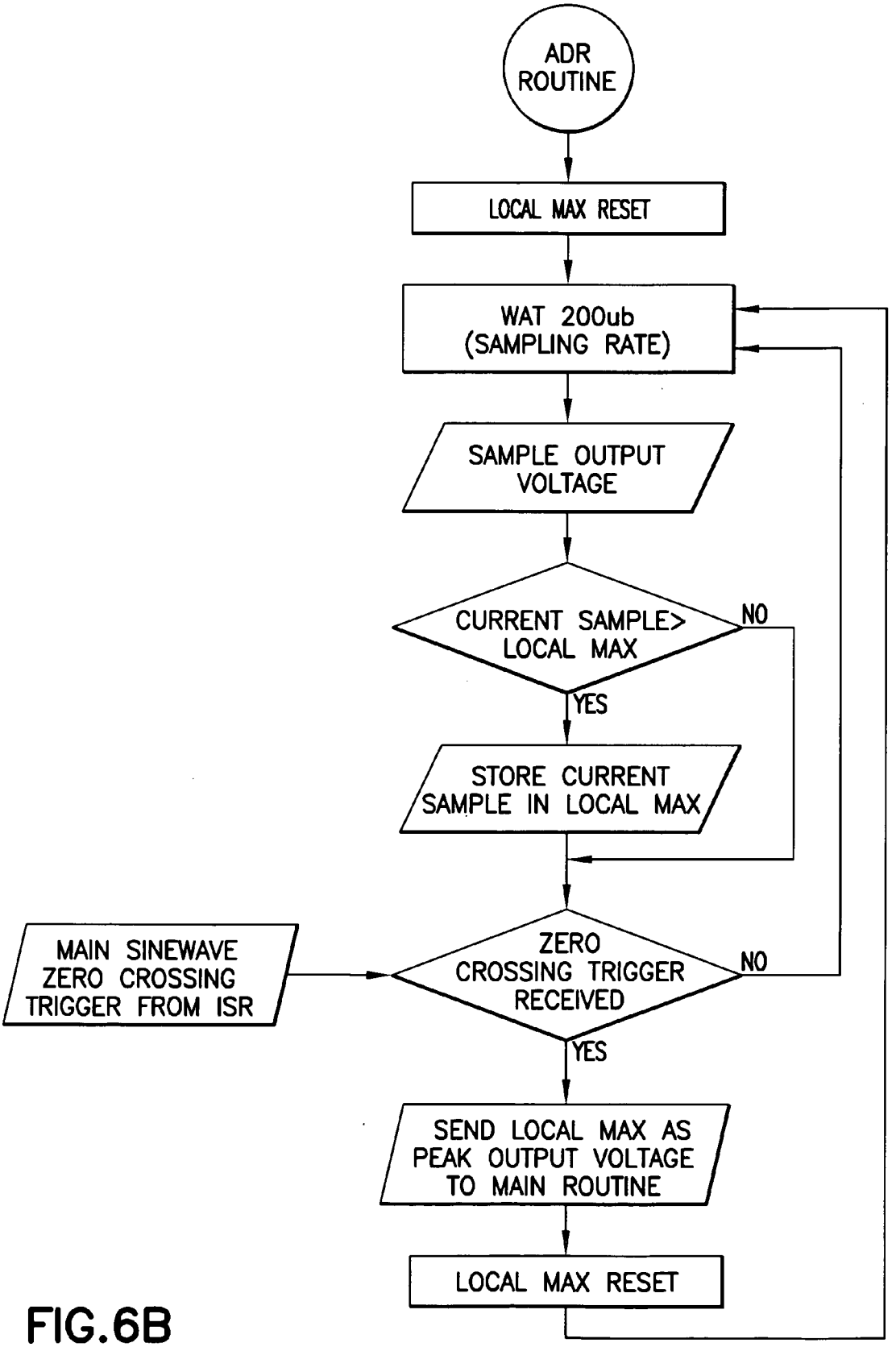

ADR ROUTINE
LOCAL MAX RESET
WAT 200ub (SAMPLING RATE)
SAMPLE OUTPUT VOLTAGE
CURRENT SAMPLE> LOCAL MAX
NO
YES
STORE CURRENT SAMPLE IN LOCAL MAX
MAIN SINEWAVE ZERO CROSSING TRIGGER FROM ISR
ZERO CROSSING TRIGGER RECEIVED
NO
YES
SEND LOCAL MAX AS PEAK OUTPUT VOLTAGE TO MAIN ROUTINE
LOCAL MAX RESET

FIG.6B

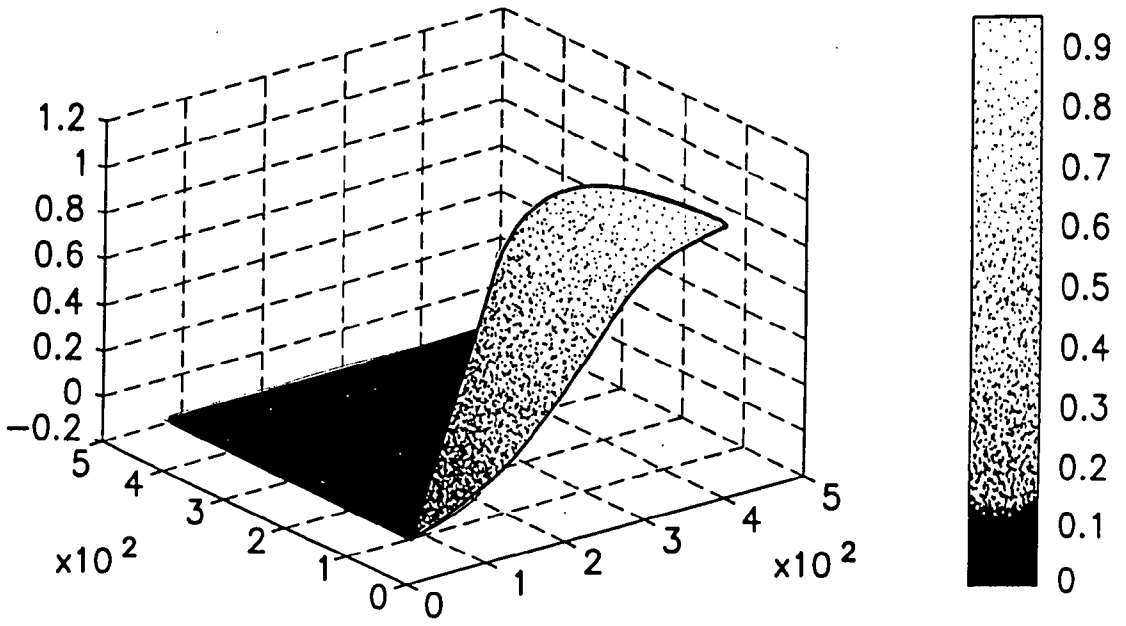

1.2
1
0.8
0.6
0.4
0.2
0
−0.2
5
4
3
2
1
0
x10 2
0
1
2
3
4
5
x10 2
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0

FIG.7

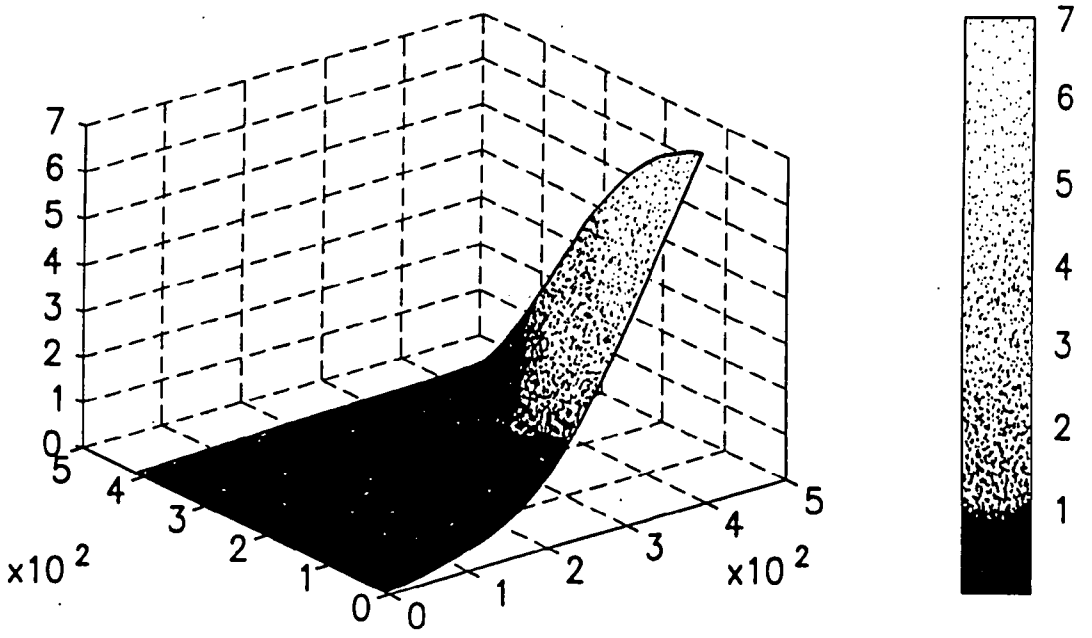

7
6
5
4
3
2
1
0
5
4
3
2
1
0
x10 2
0
1
2
3
4
5
x10 2
7
6
5
4
3
2
1

FIG.8

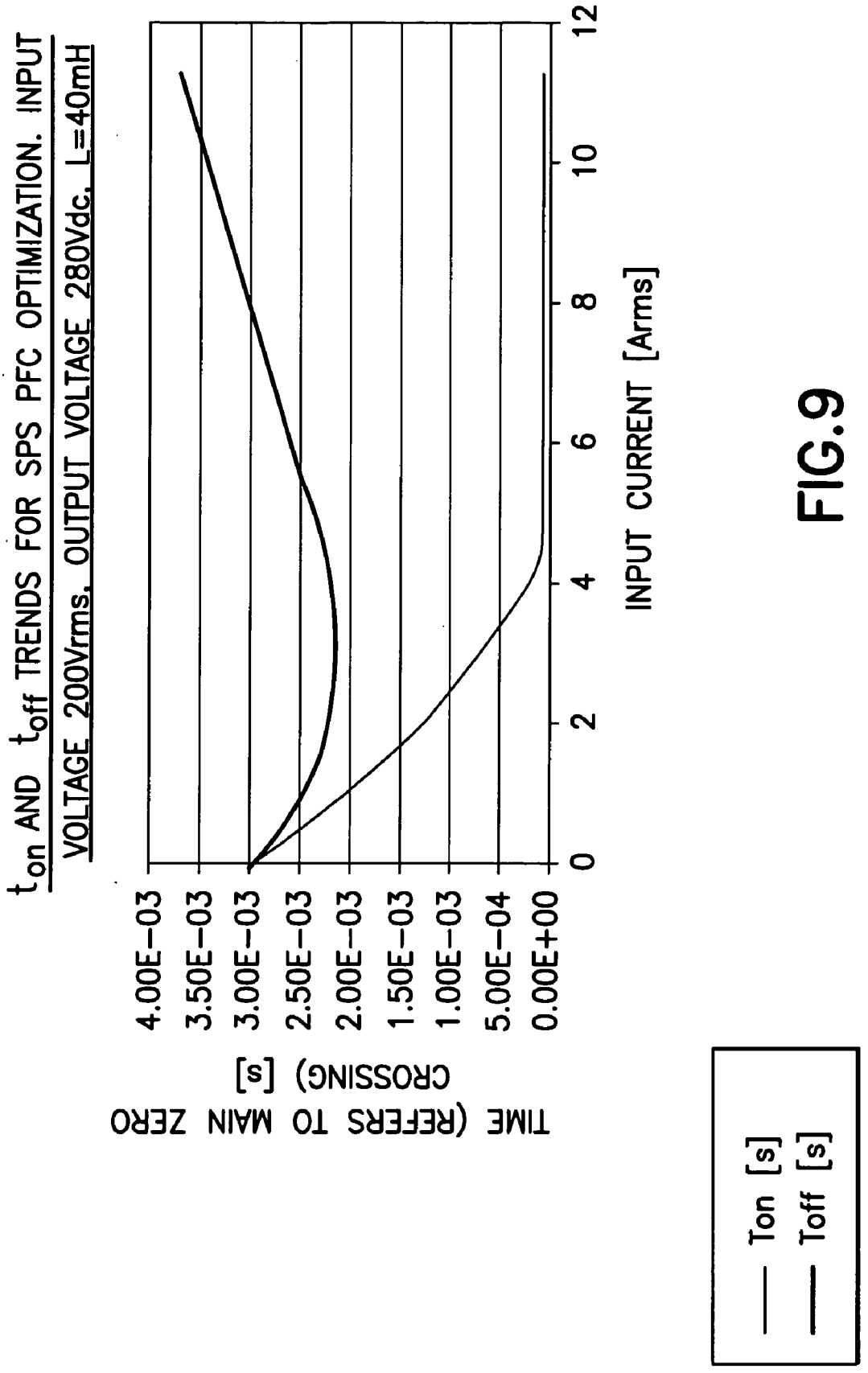

t_{on} AND t_{off} TRENDS FOR SPS PFC OPTIMIZATION. INPUT VOLTAGE 200Vrms, OUTPUT VOLTAGE 280Vdc, L=40mH
TIME (REFERS TO MAIN ZERO CROSSING) [s]
4.00E-03
3.50E-03
3.00E-03
2.50E-03
2.00E-03
1.50E-03
1.00E-03
5.00E-04
0.00E+00
0
2
4
6
8
10
12
INPUT CURRENT [Arms]
Ton [s]
Toff [s]

FIG.9

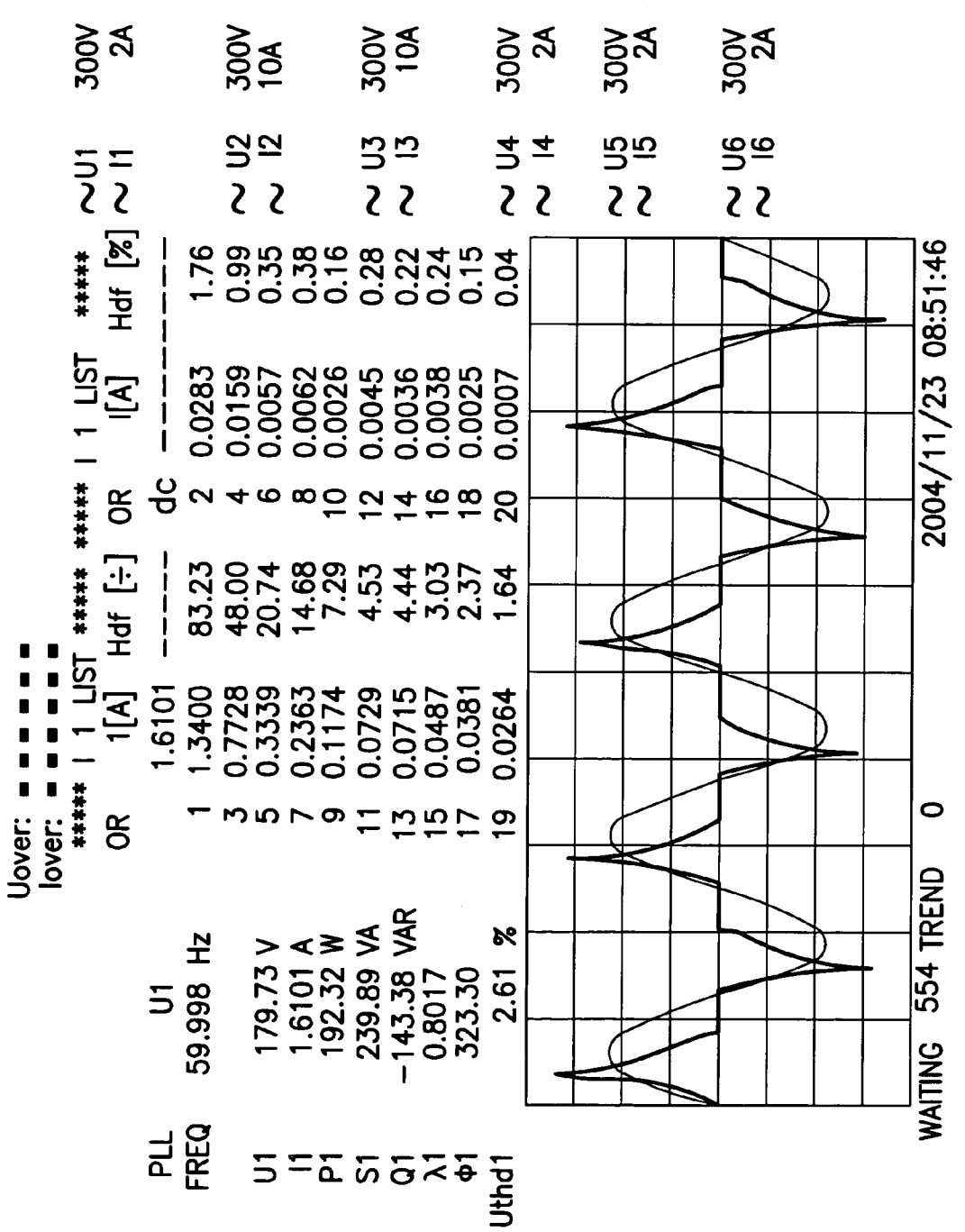


FIG. 10 Vin =180Vrms Pin=190W

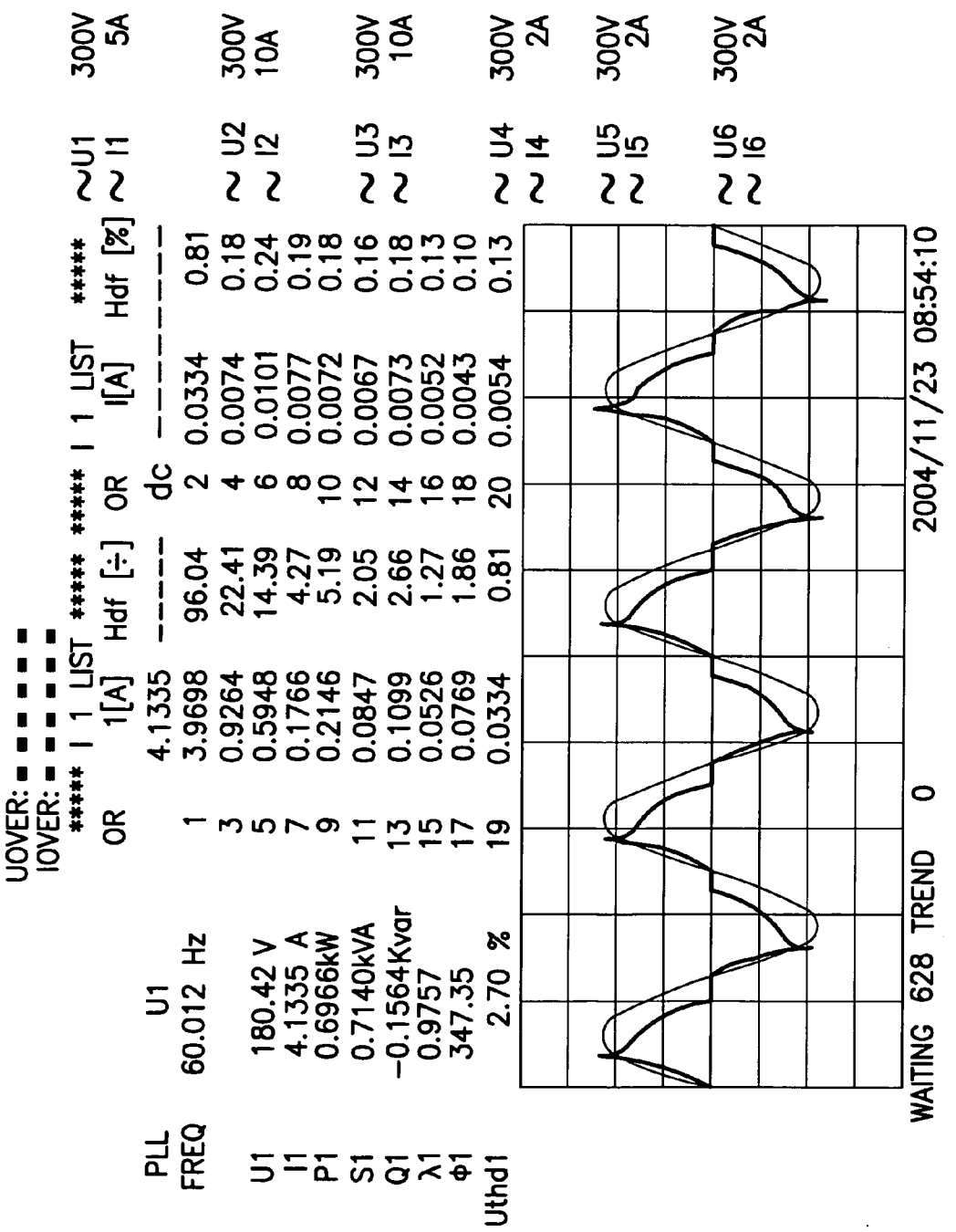


FIG. 11 Vin =180Vrms Pin=700W

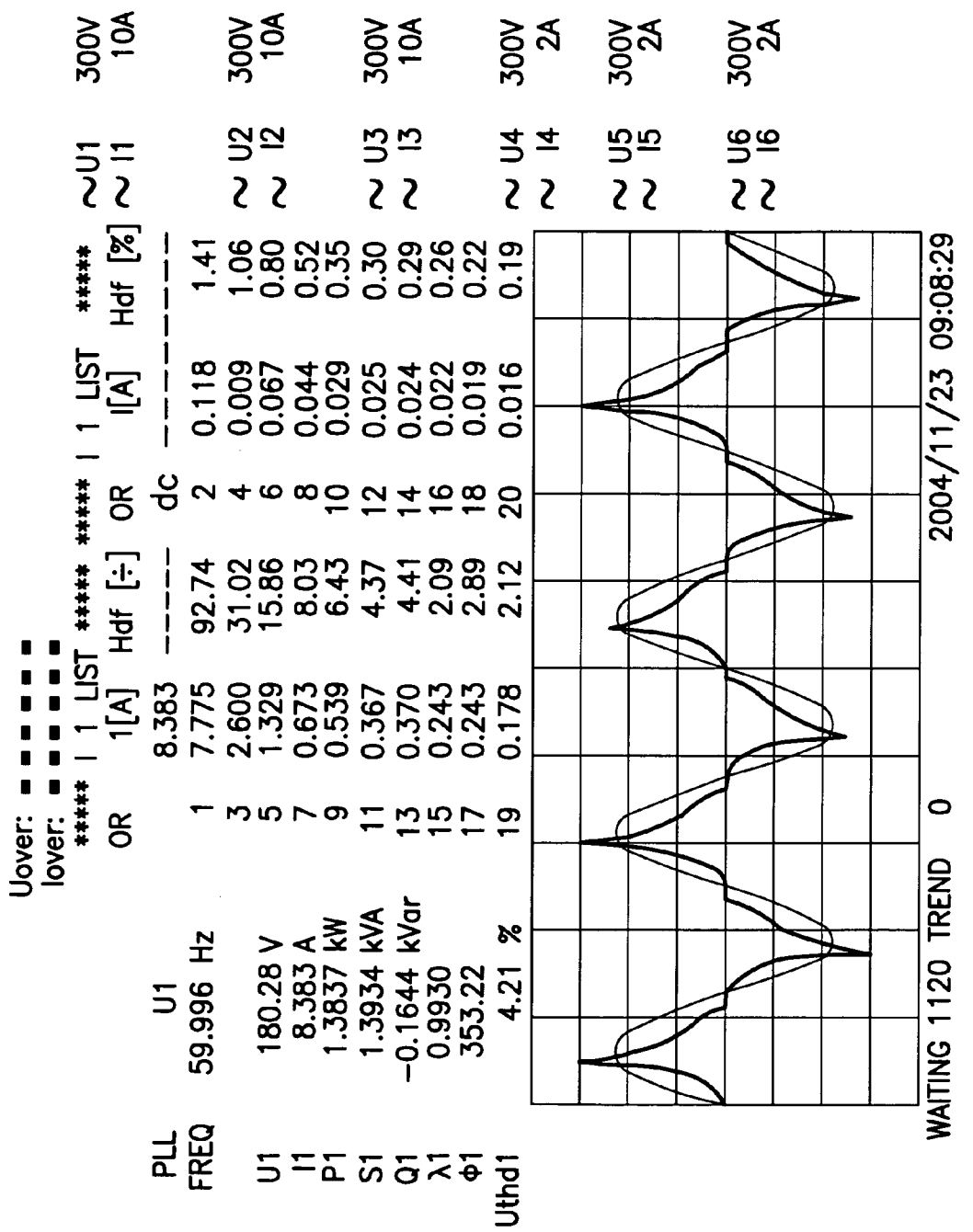


FIG. 12 Vin =180Vrms, Pin=1380W

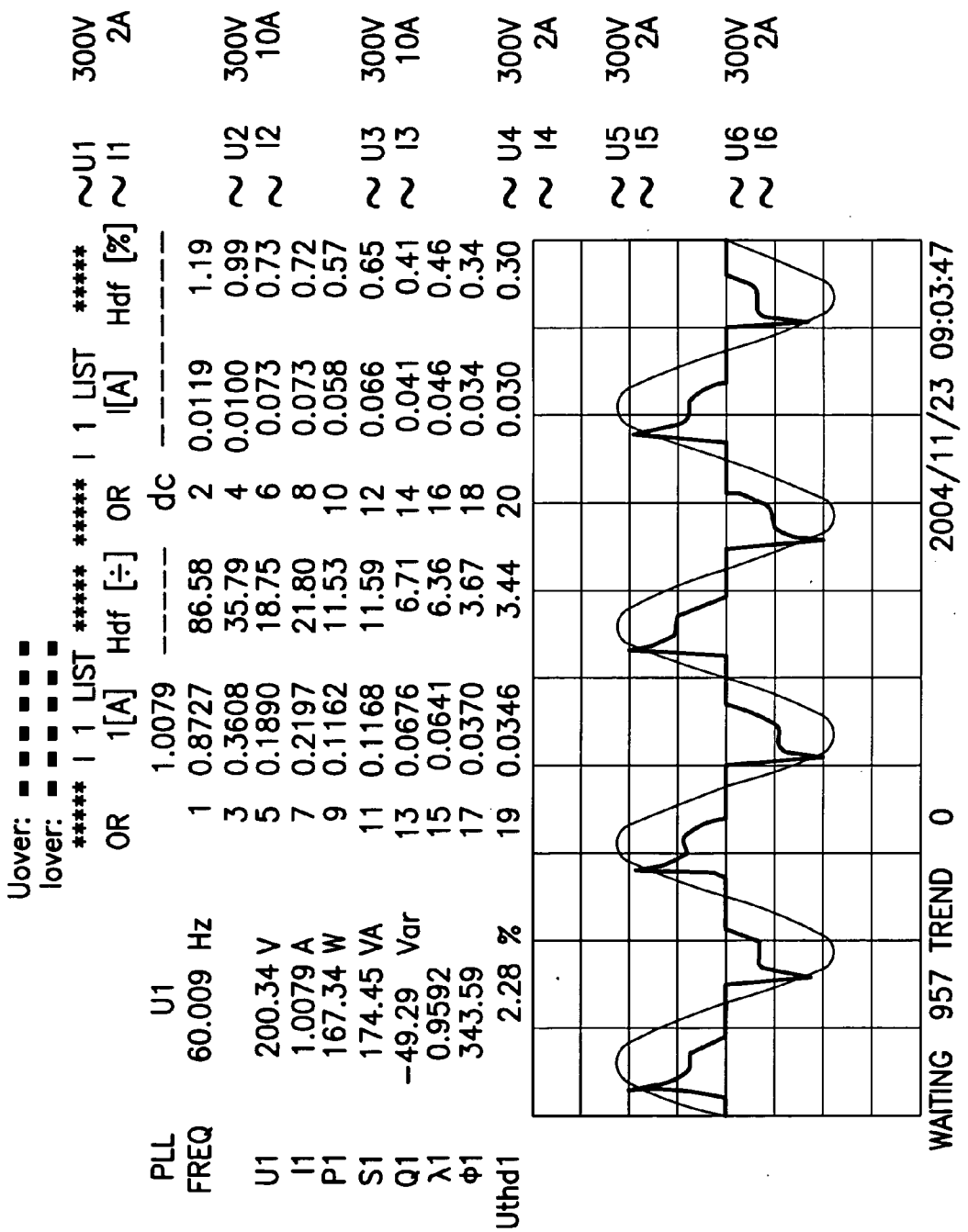


FIG.13 Vin =200Vrms, Pin=170W

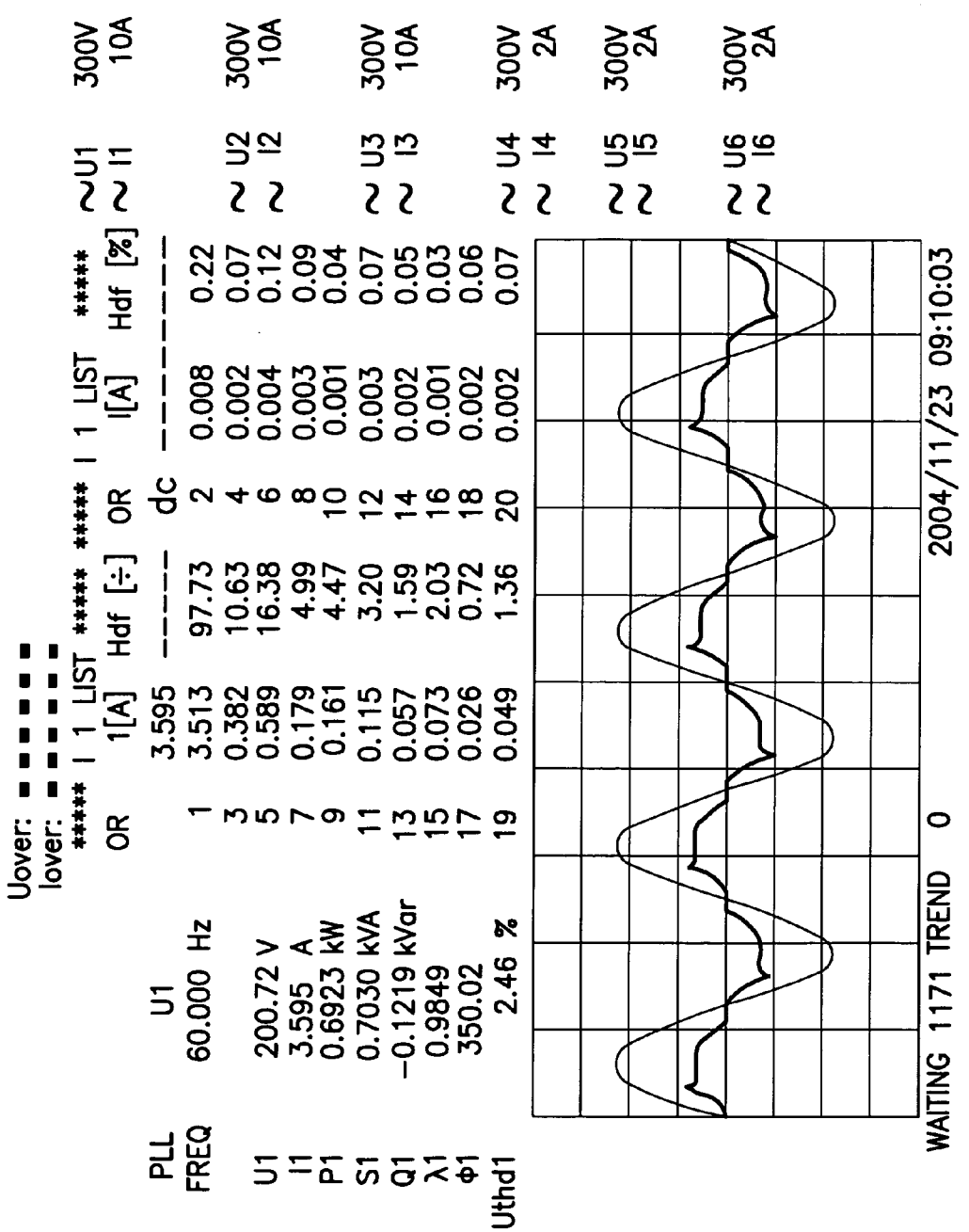


FIG.14 Vin =200Vrms, Pin=690W

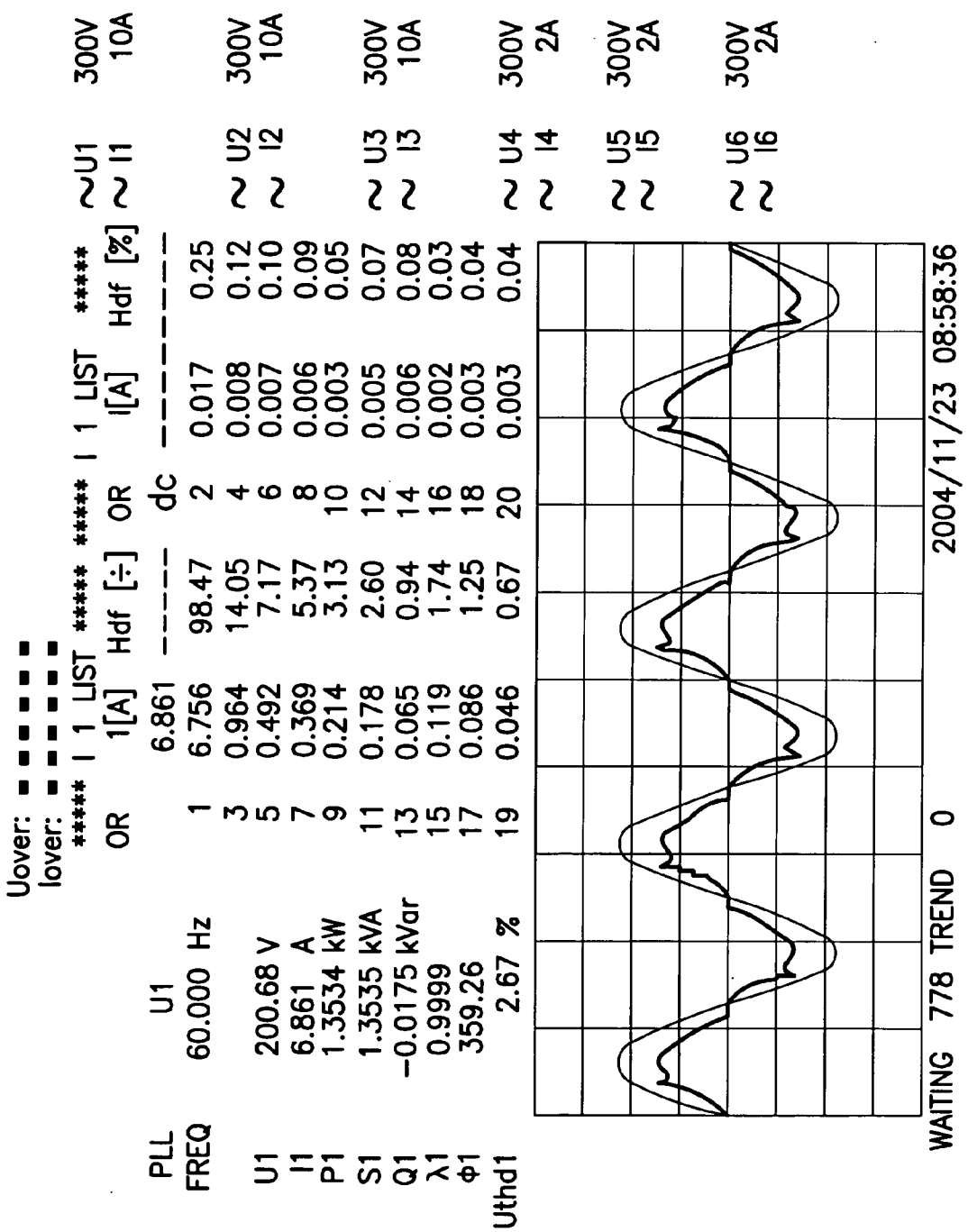


FIG.15 Vin =200Vrms, Pin=1350W

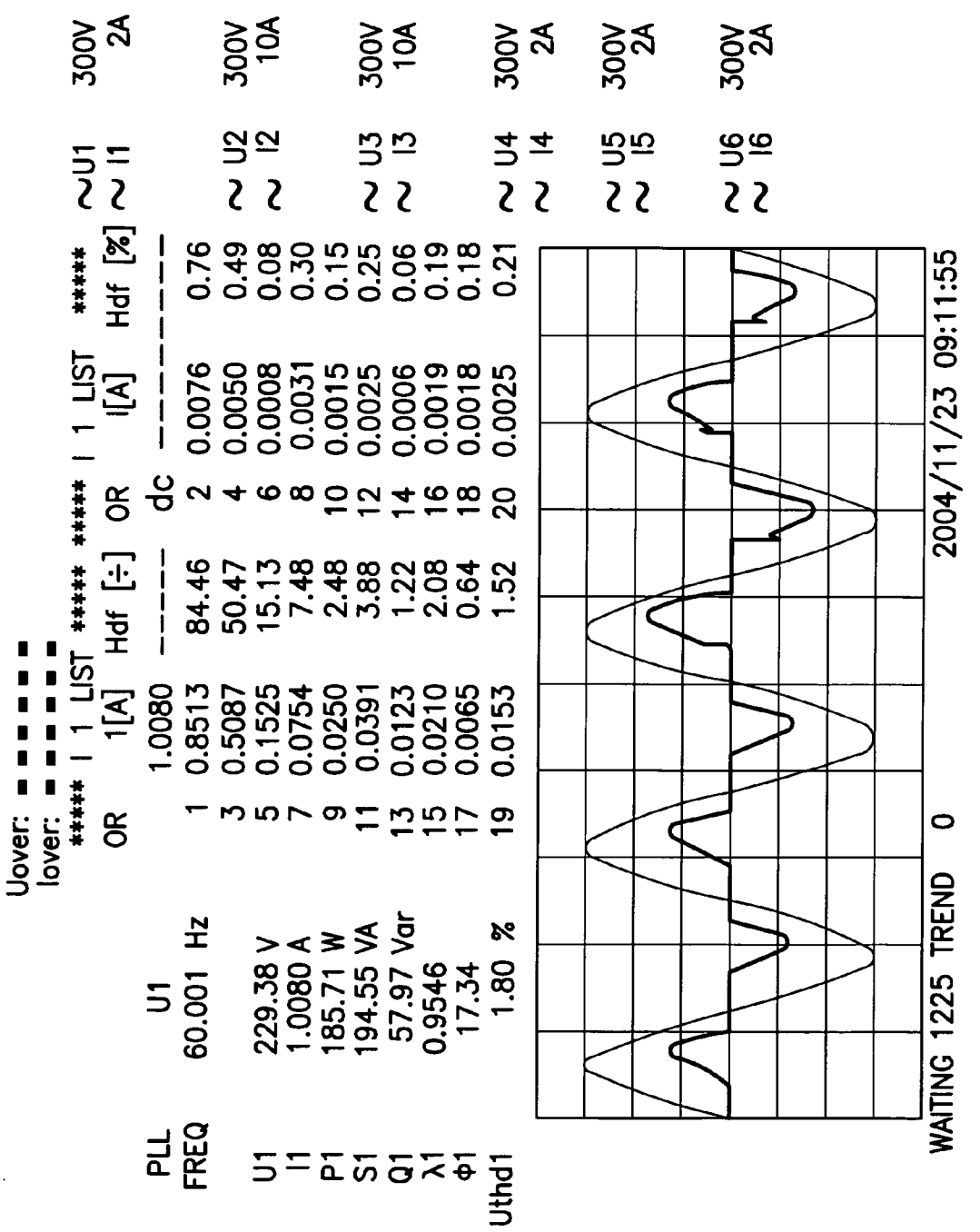


FIG.16 Vin =230Vrms, Pin=185W

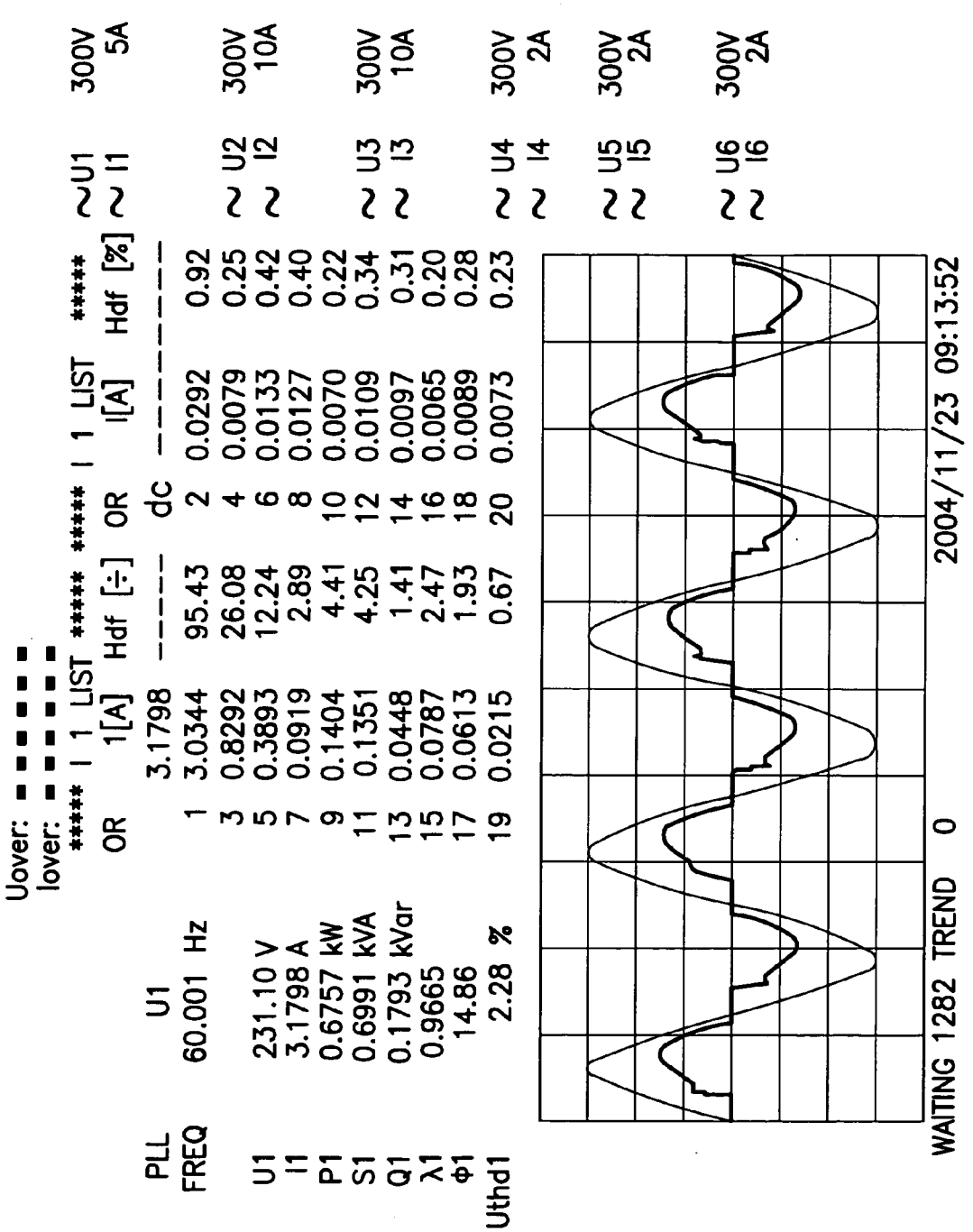

Uover: ■■■■■■■
Iover: ■■■■■■■
***** I 1 LIST ***** ***** I 1 LIST *****
OR 1[A] Hdf [÷] OR I[A] Hdf [%]
3.1798 ----- dc ----------
PLL U1
FREQ 60.001 Hz
1 3.0344 95.43 2 0.0292 0.92
3 0.8292 26.08 4 0.0079 0.25
5 0.3893 12.24 6 0.0133 0.42
7 0.0919 2.89 8 0.0127 0.40
U1 231.10 V
I1 3.1798 A
P1 0.6757 kW
S1 0.6991 kVA
Q1 0.1793 kVar
λ1 0.9665
φ1 14.86
Uthd1 2.28 %
9 0.1404 4.41 10 0.0070 0.22
11 0.1351 4.25 12 0.0109 0.34
13 0.0448 1.41 14 0.0097 0.31
15 0.0787 2.47 16 0.0065 0.20
17 0.0613 1.93 18 0.0089 0.28
19 0.0215 0.67 20 0.0073 0.23
~U1 300V 5A
~ I1
~ U2 300V 10A
~ I2
~ U3 300V 10A
~ I3
~ U4 300V 2A
~ I4
~ U5 300V 2A
~ I5
~ U6 300V 2A
~ I6
WAITING 1282 TREND 0
2004/11/23 09:13:52
Vin =230Vrms, Pin=675W

FIG.17

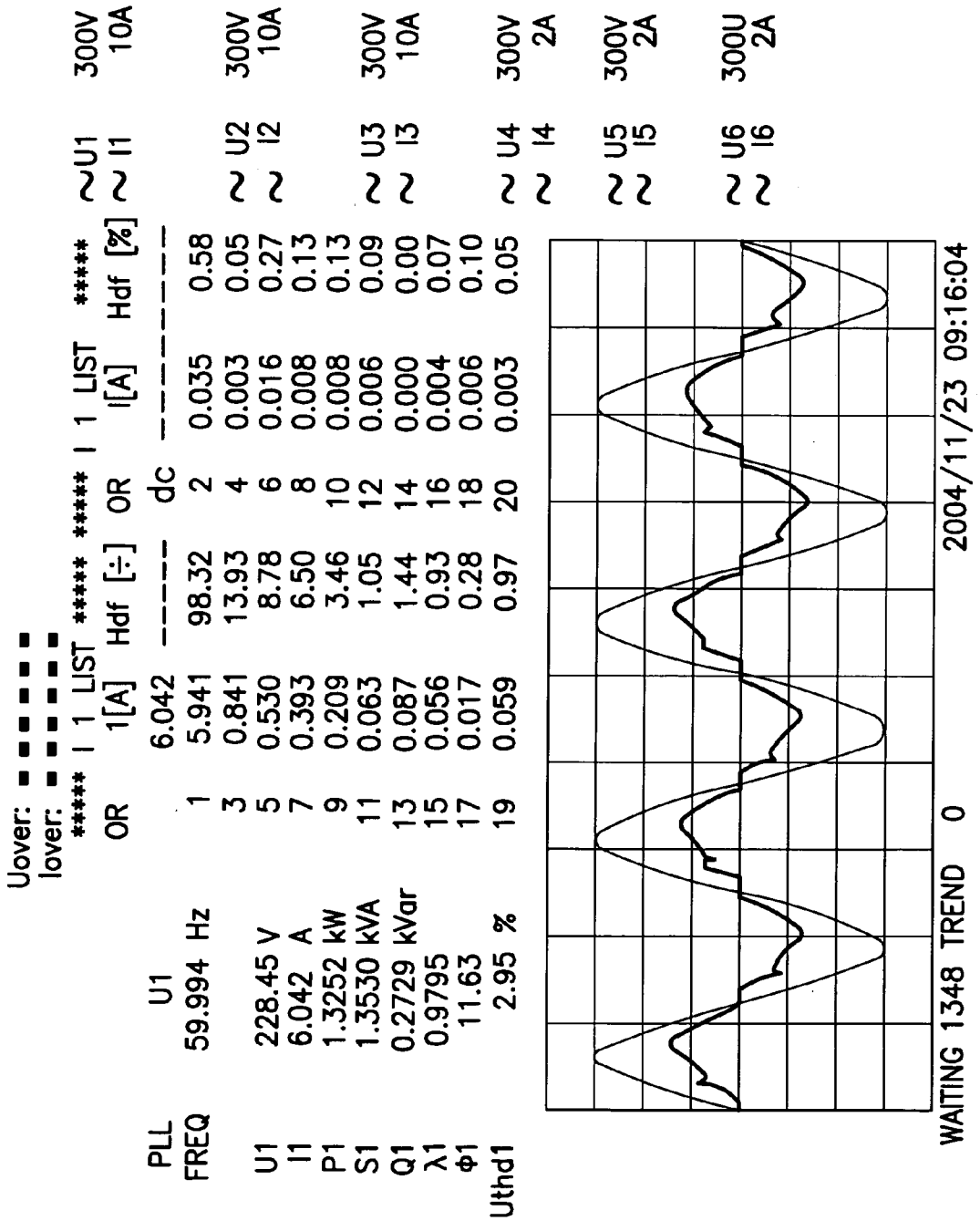


FIG.18 Vin =230Vrms, Pin=1350W

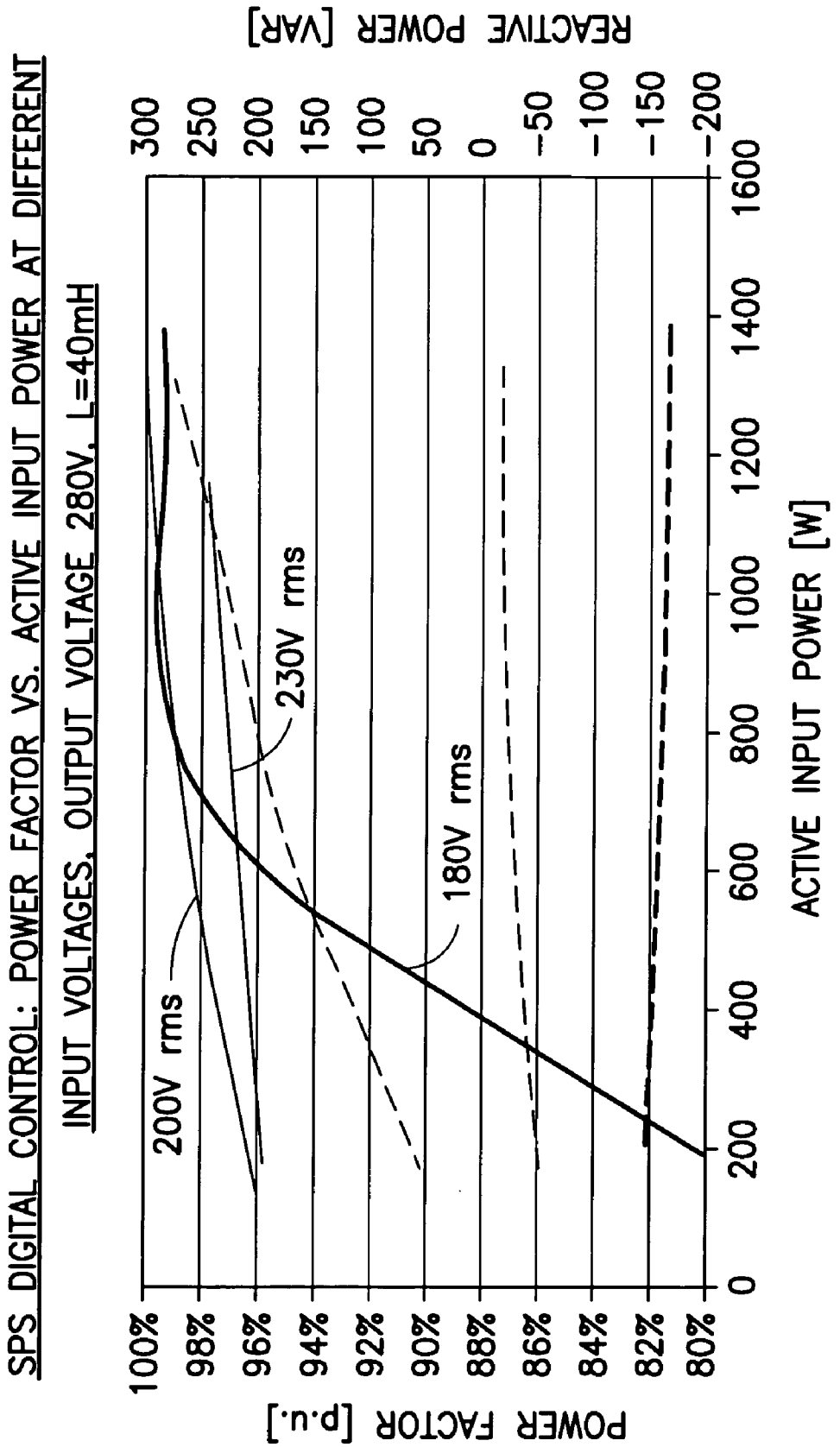

SPS DIGITAL CONTROL: POWER FACTOR VS. ACTIVE INPUT POWER AT DIFFERENT
INPUT VOLTAGES, OUTPUT VOLTAGE 280V, L=40mH
POWER FACTOR [p.u.]
100%
98%
96%
94%
92%
90%
88%
86%
84%
82%
80%
0
200
400
600
800
1000
1200
1400
1600
ACTIVE INPUT POWER [W]
REACTIVE POWER [VAR]
300
250
200
150
100
50
0
-50
-100
-150
-200
200V rms
230V rms
180V rms

FIG.19

SIMPLE PARTIAL SWITCHING POWER FACTOR CORRECTION CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims the benefit and priority of U.S. Provisional Application No. 60/635,921 filed Dec. 14, 2004 and entitled PHASE AND PULSE WIDTH MODULATION CONTROL FOR SIMPLE PARTIAL SWITCHING (SPS) POWER FACTOR CORRECTION (PFC) CIRCUITS, the entire disclosure of which is incorporated by reference herein.

BACKGROUND OF THE INVENTION

[0002] The present application relates to power supplies with active power factor correction circuits and in particular, simple partial switching (SPS) power factor correction circuits. Even more particularly, the present invention relates to such a power factor correction circuit based on output voltage feedback and discloses an embodiment having a digital controller.

[0003] The motor control market, including electric appliances such as air-conditioners, requires significant power from the AC line mains, for example, for air conditioners on the order of 300 to 2500 kw. The need for continuous service at these power levels from domestic outlets requires high power factor in order not to overload the local power network and to provide compliance with standards such as IEC 61000-3-2 Class A standard for harmonic current emissions.

[0004] Cost and size issues are driving the choice of active power factor correction circuits toward low-cost, reduced performance systems like the SPS (simple partial switching) topology, known in the literature since 1992. These circuits typically rely on input current feedback to provide power factor correction.

SUMMARY OF THE INVENTION

[0005] An object of the present invention is to provide a converter circuit using the SPS topology which does not require input current feedback for PFC.

[0006] Another object of the present invention is to provide a digital control of the SPS PFC control.

[0007] It is also an object of the present invention to improve upon the existing simple partial switching power factor correction by providing a digital control for the SPS control function and in particular, a controller which uses a single pulse control to control the power factor correction function.

[0008] In accordance with the invention, a boost type power supply circuit for providing a DC output voltage is provided comprising first and second semiconductor switches coupled between respective input lines and a common connection, an AC input voltage from an AC source being supplied across the input lines; first and second diodes coupled in series with respective ones of the switches; third and fourth diodes coupled across respective ones of the switches in a free-wheeling relationship with the switches, an inductance coupled in at least one of the input lines; a controller for controlling the conduction times of the switches by providing a pulse width and phase modulated control signal to each of the switches; whereby the controller turns on at least one of the switches during a positive half cycle of the AC voltage to allow energy storage in the inductance and turns off the at least one switch to allow the energy stored in the inductance to be supplied to an attached load through one of the first and second diodes and one of the third and fourth diodes; and the controller turns on at least one of the switches during a negative half cycle of the AC voltage to allow energy storage in the inductance and turns off the at least one switch to allow the energy stored in the inductance to be supplied to the attached load through one of the first and second diodes and one of the third and fourth diodes; and wherein the controller determines an on-time and an off-time of a pulse of the pulse width modulated control signal during each half cycle of the AC voltage based on at least one input without requiring sensing of input current from the AC source; the on-time and off-time of the pulse being controlled to regulate said output voltage and to provide power factor correction of said AC input voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The invention will now be described in greater detail in the following detailed description with reference to the drawings in which

[0010] **FIG. 1** shows a simplified schematic for a bridgeless boost converter with SPS power factor correction according to the invention;

[0011] **FIG. 2** shows a circuit diagram of a bridgeless boost converter with PFC according to the present invention incorporating digital control together with a waveform showing the positive AC half cycle;

[0012] **FIG. 3** shows the timing diagram of a control pulse provided to the switches of the circuit of **FIG. 2**;

[0013] **FIG. 3A** shows exemplary low power waveforms for the input current I and AC half cycle voltage V;

[0014] **FIG. 3B** shows exemplary high power current I and AC voltage waveforms;

[0015] **FIG. 4** shows the control system structure for the digital control of the circuit of **FIG. 2**;

[0016] **FIG. 5** shows the firmware main loop flow chart for the circuit of **FIG. 2**;

[0017] **FIGS. 6A and 6B** show the firmware subroutine flow charts for the circuit of **FIG. 2**;

[0018] **FIG. 7** shows power factor as a function of the on times and off times for the pulse provided to the switches;

[0019] **FIG. 8** shows the input RMS current as a function of the on times and off times of the pulse provided to the switches;

[0020] **FIG. 9** shows the optimized trend for on-time and off-time for the pulses provided to the switches versus input current for the circuit of **FIG. 2**;

[0021] **FIGS. 10-18** show input waveforms and power parameters for the circuit of **FIG. 2** as follows:

[0022] **FIG. 10** V_{in}=180 V_{rms} P_{in}=190 W

[0023] **FIG. 11** V_{in}=180 V_{rms} P_{in}=700 W

[0024] **FIG. 12** V_{in}=180V_{rms} P_{in}=1380 W

[0025] **FIG. 13** V_{in}=200 V_{rms} P_{in}=170 W

[0026] **FIG. 14** V_{in}=200 V_{rms} P_{in}=690 W

[0027] **FIG. 15** V_{in}=200 V_{rms} P_{in}=1350 W

[0028] **FIG. 16** V_{in}=230 V_{rms} P_{in}=185 W

[0029] **FIG. 17** V_{in}=230 V_{rms} P_{in}=675 W and

[0030] **FIG. 18** V_{in}=230V_{rms} P_{in}=1350 W; and

[0031] **FIG. 19** shows a summary chart of SPS digital control showing power factor versus active input power at different input voltages (180 Vrms, 200 Vrms and 230 Vrms) with an output voltage of 280 volts DC and an input inductance of 40 millihenries.

DETAILED DESCRIPTION

[0032] With reference now to **FIG. 1**, this shows a system schematic of a bridgeless boost power supply with SPS power factor correction according to the invention. The circuit is simpler than traditional boost type converter circuits with PFC which require an input rectifying bridge to convert the AC main current into a DC current, and a PFC switch coupled between the output of the input inductor and ground. The standard power factor correction circuit has higher conduction losses due to the diode bridge and has redundant rectification in that rectification occurs both in the diode bridge and in the boost diode.

[0033] In contrast, the circuit of **FIG. 1** is simpler and is often called a bridgeless boost circuit with PFC. There are only four diodes, not five, and if the transistor switches are implemented with FETs, two of the diodes can be eliminated because of the presence of the body diodes of the FETs.

[0034] In the circuit shown in **FIG. 1**, IGBTs M1 and M2 are employed together with diodes D1 and D2 and D1A and D2A. If M1 and M2 are FETs, diodes D1A and D2A can be dispensed with and would be the body diodes of the FETs.

[0035] The circuit shown in **FIG. 1** operates in the following way: For the positive AC input half cycle, initially, the switch M1 is turned on to allow current to flow through the inductor L thereby storing energy in the inductor L. The current path is through the switch M1 which is turned on and then through the diode D2A to the return AC input line. When switch M1 is turned off, the energy stored in the inductor is released as current flows through the diode D1, charging up the output capacitor C and flowing through the load and returning to the AC main line return through the free-wheeling diode D2A.

[0036] In the negative half cycle, current flows through the inductor L storing energy when the transistor M2 is turned on by the SPS controller. The current path returns to the AC line through the diode D1A. When switch M2 is turned off, energy is released in the inductor as current flows through diode D2 charging the capacitor C and flowing through the load and returning to the AC line through the free-wheeling diode D1A.

[0037] As shown in **FIG. 1**, the two switches M1 and M2 can be driven simultaneously because of the presence of the freewheeling diodes D1A and D2A. When transistors M1 and M2 are on, the inductor charges through one of the transistors and the return path is through the freewheeling diode or body diode of the other transistor. This greatly simplifies the control process.

[0038] The PFC function requires controlling the current drawn from the main AC line and shaping it like the input voltage waveform. In order to accomplish this, the output voltage is sensed by the controller and the zero crossing of the AC line waveform is sensed by the zero crossing detector ZC. The sensed output voltage is used both to regulate the output voltage within the prescribed range and to provide power factor correction at the AC input. In particular, when the output voltage decreases (increased loading), the switches M1 and M2 are driven into conduction for longer periods of time by increasing the pulse width of the gate drive pulses, thereby storing more energy in the inductor for transfer to the output capacitor. If the load lightens and the output voltage increases, the transistors M1 and M2 are driven by a reduced pulse width gate drive signal to bring the output voltage back into regulation. By control of the PWM and the timing of the gate drive pulse in the half cycle, both the output regulation and the power factor can be regulated. In prior art circuits of this type, the input current is sensed, for example, by placing a resistor in the emitter circuits of the IGBTs to control the PFC. In the circuit of **FIG. 1**, current sensing is not necessary.

[0039] As is evident also from **FIG. 1**, there is one less diode drop than in the standard boost converter circuit with PFC, where there are always three diode drops, two in the bridge in each half cycle and in the boost diode. In the circuit of **FIG. 1**, there are only two diode drops in each half cycle, thus resulting in peak efficiency. Further, the IGBTs can be smaller since they conduct alternate half cycles even though they are driven simultaneously.

[0040] Turning now to **FIG. 2**, a bridgeless boost converter with SPS power factor correction employing digital control is shown and includes IGBTs M1 and M2, as in the circuit of **FIG. 1**, diodes D1, D1A, D2 and D2A, output capacitor C, input inductance L which is divided amongst two inductances L1 and L1A provided in the two AC input lines. The output of the converter circuit supplies DC power to the load.

[0041] The control circuit **10** includes a resistor divider comprising resistors R1, R2 and R3 coupled across the load. The voltage divider output is provided through a resistor R4 to the control chip C which in the illustrated embodiment is a PIC 12F675 microcontroller. A voltage regulator VR provides power for the microcontroller UC. The output of the microcontroller is provided at GP1 which controls an FET M3 which is turned on and off to provide appropriate gate drive pulses through the transistors M1 and M2. The drain of M3 is coupled through a resistor R5 to the 15 volt supply for the voltage regulator VR. The gate of the switch M3 is coupled to the output of the microcontroller GP1 through a diode D3 and coupled to the 5 volt output of the regulator VR through a resistor R6. Accordingly, when the output of the processor UC goes low, transistor M3 is turned off, generating a pulse at the gates of transistors M1 and M2. When GP1 goes high again, diode D3 is back biased, turning switch M3 on, and turning off the transistors Q1 and Q2. Accordingly, the time when the processor output is low determines the pulse width duration provided to the gates of the transistors M1 and M2.

[0042] Zero crossing detection is provided by an opto-coupler integrated circuit IC1 which determines when the

input voltage is zero. The output of IC**1** is provided to input GP**2** of the microcontroller. IC**1** is also coupled to the logic voltage supply line (+5V DC) and ground for power.

[**0043**] When the input voltage AC waveform is zero volts corresponding to a zero crossing of the input AC voltage, the output of the integrated circuit IC**1** goes low, back biasing diodes D**4** and D**5**, and thus driving the input GP**2** to ground through a pull down resistor R**7**. When the input AC waveform is non-zero, the output IC**1** will be high forward biasing diodes D**4** and D**5** and input GP**2** will therefore be high as shown in **FIG. 2** by the waveform adjacent to diodes D**4** and D**5**. As described with reference to **FIG. 3**, the UC will issue an on-time signal a certain time after zero crossing detection and an off-time signal a certain time later after the zero crossing.

[**0044**] **FIG. 3** shows the switch pulse timing driving the gates switches of M**1** and M**2**. According to the invention, the switches M**1** and M**2** are controlled by single pulse control. The pulse does not begin until after the zero crossing as shown in **FIG. 3** and the pulse width does not continue after the sine wave peak, that is ¼ of a period. **FIG. 3** shows the switch timing. T-ON defines the time between the zero crossing of the AC voltage and the switch turn on. T-OFF determines the time to switch turn off with respect to the zero main AC voltage zero crossing.

[**0045**] **FIGS. 3A and 3B** show simulation examples of the operation of the circuit. At low power (**FIG. 3A**), the input current I is shown, corresponding to a small pulse duration. In this example t_{ON}=100 usec, t_{OFF}=1.4 ms, V=287 V_{OUT} and V_{IN}=120 Vrms.

[**0046**] In **FIG. 3B**, which shows a higher power example, it can be observed that the input current I closely matches and is in phase with the input AC voltage waveform for the entire half cycle. In the example, t_{ON}=100 u secs, t_{OFF}=2.8 msec, V_{OUT}=180V and V_{IN}=120 Vrms.

[**0047**] According to the invention, a program was written to generate a table of on-times and off-times to provide high power factors at various currents. This program was structured as follows:

[**0048**] First, a small time step was chosen (t_{step}), not bigger than the microcontroller resolution over the chosen time interval (8 bit microcontroller on 1/(4·60) ms time-frame means $t_{step} \leqq 16$ μs). Then, a diagonal matrix was constructed, with same value in each column and $t_{n+1}=T_n+t_{step}$

$$P = \begin{bmatrix} t_1 & t_2 & t_3 & t_4 & \cdots & t_n \\ & t_2 & t_3 & t_4 & \cdots & \vdots \\ & & t_3 & t_4 & \cdots & \vdots \\ & & & t_4 & \cdots & \vdots \\ & & & & & \vdots \\ & & & & & t_n \end{bmatrix}$$

[**0049**] Subroutines were then run building several other matrixes (Irms, cosfi, input power) for each possible pulse, defined assigning row index to t_{on} and column index to t_{off}

$$\lfloor t_{on}, t_{off} \rfloor_{ij} = \lfloor P_{ii}, P_{ij} \rfloor i = 1, n$$

$$j = i + 1, n$$

[**0050**] **FIGS. 7 and 8** show the power factor as a function of T-ON and T-OFF and input RMS current as a function of T-ON and T-OFF.

[**0051**] From these figures, it is apparent that there are several possible pulses which can be used to obtain a high power factor greater than 0.85 and which allow a significant input current variation and thus regulation range.

[**0052**] In order to have a wider regulation range at the maximum power factor, the program sorted out the minimum and maximum input current for pulses achieving power factors higher than 0.9. Afterward, this current range was subdivided equally and for each current value, the maximum power factor was chosen. The outcome of this operation is an optimal turn on and turn off time for each possible current value at given input and output voltage and inductor value. This is shown in **FIG. 9**. A table can be implemented in a digital memory based upon the graph shown in **FIG. 9**. Indexing the current values, the digital control can feed forward current and power factor having only a feedback based on output voltage. Moreover, the calculated timing curves allow linearizing the voltage integral across the inductor.

[**0053**] **FIG. 4** shows the control system architecture for the digital controller implemented in the microprocessor of **FIG. 2**. As shown, the output voltage V_{OUT} is compared to the desired output voltage V_{OUT*} and an error signal is generated. The error signal is then used to address the look-up table T by the UC, which provides the pulse on and off times which are fed to switch M**3** as a pulse and then to the gates of the switches M**1** and M**2**.

[**0054**] The control scheme can be implemented on a PIC12F675 microcontroller. The basic flow chart for the firmware is shown in **FIG. 5**. The flow chart of **FIG. 5** is the main loop while the two flow charts of **FIGS. 6A and 6B** show subroutines for zero crossing trigger digital filtering and analog to digital conversion respectively.

[**0055**] At the start, shown in **FIG. 5**, a start up sequence detects the main AC frequency through the zero crossing input and addresses the proper timing table. Several parameters are loaded as constants. Two parallel routines comprising an ADR analog to digital routine (**FIG. 6A**) and ISR interrupt service routine (**FIG. 6B**) are then continuously running and provide proper inputs to the main program. In the ISR routine **FIG. 6A**, in order to avoid false triggering due to noise and disturbances, the digital filter properly acknowledges the zero crossing trigger pulse given by the opto coupler IC**1** of **FIG. 2**

[**0056**] In the ADR routine **FIG. 6B**, the analog to digital converter samples the output voltage feedback through the resistor divider comprising resistors R**1**, R**2** and R**3** and stores the maximum value cycle by cycle, passing this value to the main routine as a feedback.

[**0057**] An initial fixed delay parameter is needed to properly compensate the external trigger pulse normally in advance because of the simple zero crossing circuitry.

[0058] The main routine is triggered by zero crossing detection and thus has a frequency of twice the main AC voltage. Before applying any pulse to the gates of the switches M1 and M2, the firmware checks any output voltage for an over voltage condition avoiding any further increase in output voltage by resetting the pulse sequence.

[0059] **FIGS. 10-18** show the input waveforms, various input voltages and input powers. The parameters identified include

[0060] U1 RMS input voltage;

[0061] I1 RMS current;

[0062] P1 active power;

[0063] S1 apparent power;

[0064] Q1 reactive power;

[0065] $\lambda 1$ power factor;

[0066] $\phi 1$ displacement angle; and

[0067] Uthd1 total harmonic distortion

[0068] The waveforms shown are input voltage and input current, three power levels, 180, 720 and 1400 watts, and three input main voltages, 180, 200 and 230 volts rms as shown. The output voltage is set to 280 volts in each case. With the exception of **FIG. 10**, the power factor $\lambda 1$ in each case is well above 0.85.

[0069] It is noticeable that there is a negative sign on reactive power for the lower voltage, almost unity power factor at medium voltage and a positive sign at higher voltage. This occurs because the calculated table is optimal for a 200 volt rms main line voltage. Below the optimization value the converter shows capacitive behavior while above the optimization value the circuit shows inductive behavior. This provides criteria on how to optimize the system. At 230 volt rms light load, the pulse is jittery, i.e., either zero pulse width or the smallest possible pulse width is selected. See **FIG. 16**.

[0070] At 180 volt rms low load, the power factor drops because of the relatively large pulse needed to boost the output voltage to 280 volts. This is the intrinsic limit in this kind of control. It is difficult to avoid because of the absence of any feedback suitable for identifying this particular condition. See **FIG. 10**.

[0071] For 180 volt rms high load, see **FIG. 12**, the standard IC61000-3-2 is not satisfied because of a few harmonics over the limits as shown by Uthd1.

[0072] **FIG. 19** summarizes the **FIGS. 10-18** showing power factor versus active input power at different AC input voltages as shown and with the output voltage at 280 volts DC and with an input inductance of 40 millihenries.

[0073] The control system can achieve high power factors and stable DC output bus voltage complying with the harmonic rule IEC 61000-3-2 with one exception at high power, low AC input voltage condition as explained above, that is, at high power, 180 volt rms AC input (**FIG. 12**). With the AC input at 200 Vrms or higher, the power factor is always above 95% as shown in **FIG. 19**. It only drops below this level, as explained above, at the lower input voltage at low power levels.

[0074] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. Therefore the present invention should be limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. A boost type power supply circuit for providing a DC output voltage comprising:

first and second semiconductor switches coupled between respective input lines and a common connection, an AC input voltage from an AC source being supplied across the input lines;

first and second diodes coupled in series with respective ones of the switches;

third and fourth diodes coupled across respective ones of the switches in a free-wheeling relationship with the switches,

an inductance coupled in at least one of the input lines;

a controller for controlling the conduction times of the switches by providing a pulse width and phase modulated control signal to each of the switches;

whereby the controller turns on at least one of the switches during a positive half cycle of the AC voltage to allow energy storage in the inductance and turns off the at least one switch to allow the energy stored in the inductance to be supplied to an attached load through one of the first and second diodes and one of the third and fourth diodes; and

the controller turns on at least one of the switches during a negative half cycle of the AC voltage to allow energy storage in the inductance and turns off the at least one switch to allow the energy stored in the inductance to be supplied to the attached load through one of the first and second diodes and one of the third and fourth diodes; and wherein

the controller determines an on-time and an off-time of a pulse of the pulse width modulated control signal during each half cycle of the AC voltage based on at least one input without requiring sensing of the input current from the AC source;

the on-time and off-time of the pulse being controlled to regulate said output voltage and to provide power factor correction of said AC input voltage.

2. The circuit of claim 1, wherein the controller comprises a microprocessor and the microprocessor determines an on-time and off-time of a pulse of the pulse width modulated control signal during each half cycle of the AC voltage based on at least one input by accessing a memory storing a table of said on-times and off-times.

3. The circuit of claim 1, further comprising a detection circuit providing an input to said controller to determine a beginning of each half cycle of said AC voltage and wherein said on-times represent a first time period following said beginning of each half cycle and said off-times represent a second time period following said beginning of said half cycle, said pulse having a pulse width determined by the

time difference between said on-time and said off-time; and said on-times and off-times being selected to provide power factor correction.

4. The circuit of claim 3, wherein said detection circuit to determine a beginning of each half cycle comprises a zero crossing voltage detection circuit.

5. The circuit of claim 4, wherein one of said inputs to said controller comprises an output of said zero crossing voltage detection circuit.

6. The circuit of claim 1, wherein the at least one input to said controller comprises a voltage related to the output voltage of said circuit, whereby the output voltage is regulated within a predefined regulation range by controlling said pulse width.

7. The circuit of claim 6, wherein the at least one input comprises a signal determining the beginning of each half cycle of said AC input voltage, said controller providing a pulse width modulated signal with said determined on-time and off-time to provide power factor correction of said AC input voltage.

8. The circuit of claim 2, wherein said controller comprises a memory having stored therein said on-times and off-times corresponding to a predefined range of power factor.

9. The circuit of claim 8, wherein said predefined range of power factor comprises a range between a predefined number less than 1 and 1.

10. The circuit of claim 8, wherein said memory comprises a look-up table.

11. The circuit of claim 1, wherein said third and fourth free-wheeling diodes comprise body diodes of respective one of said switches.

12. The circuit of claim 1, wherein said switches comprise bipolar transistors IGBTs, or FETs.

13. The circuit of claim 1, wherein said switches comprise FETs and said third and fourth diodes comprise body diodes of the FETs.

14. The circuit of claim 1, further comprising an output capacitor across which said output voltage is developed.

15. The circuit of claim 1, wherein said inductance comprises first and second inductors disposed in each of said input lines.

16. The circuit of claim 6, wherein the voltage related to the output voltage is developed across a voltage divider circuit.

17. The circuit of claim 2, wherein said memory has stored therein on-times and off-times for selected current values at specified input and output voltages and inductance values.

18. The circuit of claim 1, wherein said first and second switches are turned on and off substantially simultaneously.

* * * * *

FURTHER READING

Click any one of the following links to be taken to a website which contains the following documents.

There appears to be a lot of recent patent activity in the area of building "bridgeless PFC convertors". The following are some of the patents.

11_584_983_Method_and_apparatus_for_high_efficieny_rectifier
11_204_307_AC_to_DC_power_supply_with_PF
11_302_544_Simple_partial_switching_power_factor_correction
11_474_712_BRIDGELESS_BI_DIRECTIONAL_FORWARD_TYPE_CONVERTER
11_480_004_High_efficiency_power_converter_system
11_706_645_AC_to_DC_voltage_converter_as_power_supply
12_401_983_BRIDGELESS_PFC_CIRCUIT_FOR_CRM
12_798_682_Bridgeless_PFC_converter

3295043_MASSEY_D_C__TO_D_C__REGULATED_CONVERTER
4183079_DC_AC_inverter
4523266_AC_to_DC_conversion_system
4943902_AC_to_DC_power_converter_and_method
5570276_Switching_converter_with_open_loop_input_regulation
5815380_Switching_converter_with_open_loop_Primary_regulation
5815384_Transformer_uses_bi_directional_synch_Rectifiers
6115267_AC_DC_converter_with_no_input_rectifiers
6157182_DC_DC_converter_with_multiple_operating_modes
6608522_DC_to_DC_converter_providing_stable_operation
7250742_Digital_control_of_bridgeless_power_factor_correction
7265591_CMOS_driver_with_minimum_shoot_through

And here is some more information for those who may be interested.

A BIDIRECTIONAL PWM THREE-PHASE STEP-DOWN RECTIFIER
A bidirectional, sinusoidal, high-frequency inverter
A DUAL INPUT BIDIRECTIONAL POWER CONVERTER
A new structure for bidirectional Power flow
BI-DIRECTIONAL INVERTER-CHARGER
Bi-directional single-phase half-bridge rectifier for power quality
BiDirectional Converter
Bidirectional_UP_Inverter
Synthesis of Input-Rectifierless AC/DC

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