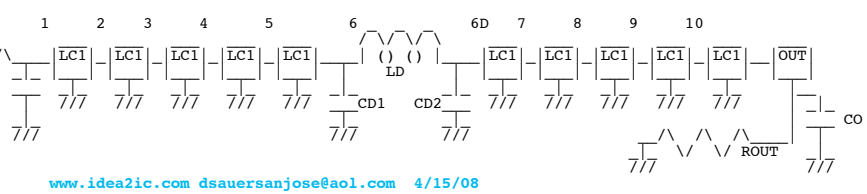
LC_transLine_Tweek




```
.OPTIONS  GMIN=1e-18    METHOD=euler   ABSTOL=1e-18  TEMP=27 srcsteps = 1  gminsteps = 1
VIN       VIN    0      PWL( 0 0 2n 0 3.0n 1  18n 1 19.0n 0)
RIN       VIN    1      50
C1        VIN    0      1.6p
XLC1      1      2      LC1
XLC2      2      3      LC1
XLC3      3      4      LC1
XLC4      4      5      LC1
XLC5      5      6      LC1
CD1       6      0      3f
LD        6      6D     16n
CD2       6D     0      3f
XLC6      6D     7      LC1
XLC7      7      8      LC1
XLC8      8      9      LC1
XLC9      9      10     LC1
XLC10     10     OUT    LC1
C2        OUT    0      -1.6p

ROUT      OUT    0      50
C3        OUT    0      10f
.tran     0.01n   30n 0 30n

*#1===What_To_Do_About_Reflection=================
.control
*#1==First_The_Addition_Of_16nH_of_Stray_Inductance===
run
plot    v(1) v(6) out   title  L_16n_1f_1f
*#2===Then_Capacitance_Is_Added_to_tweek_It_Out==
alter   CD1               capacitance  =   1.6p
alter   CD2               capacitance  =   4.8p
run
plot    v(1) v(6) out   title  L_16n_1.6p_4.8p
*#3===Try_Other_Capacitance_Ratios==============
alter   CD1               capacitance  =   1.8p
alter   CD2               capacitance  =   5.4p
run
plot    v(1) v(6) out   title  L_16n_1.8p_5.4p
*#4===Try_Other_Capacitance_Ratios==============
alter   CD1               capacitance  =   1.8p
alter   CD2               capacitance  =   5.0p
run
plot    v(1) v(6) out   title  L_16n_1.8p_5p
*#5===What_Happens_With_Balanced_Capacitance_?===
alter   CD1               capacitance  =   3.2p
alter   CD2               capacitance  =   3.2p
run
plot    v(1) v(6) out   title  L_16n_3.2p_3.2p


.endc

.SUBCKT   LC1   IN     OUT
L1        IN    OUT   8n
C1        OUT   0     3.2p
.ENDS     LC1
```

```
*                                      .SUBCKT LC1 IN OUT
*                        L1
*              _  _  _
*             / \/ \/ \                             _________
*   |IN |_| () () |___|OUT|        |IN |__|          |___|OUT|
*                  |                       |   LC1   |
*                 _|_                      |_________|
*                 ___  C1                       |
*                  |                           ///
*                  |
*                 ///    8nH_3.2pF =>50Ohms @ 1Ghz  50*3.2p =160ps
*
*    http://www.idea2ic.com/PlayWithJavascript/L_C_R_F.html
*
```

.end

=====================END_OF_SPICE============================

***#1===What_To_Do_About_Reflection=================**

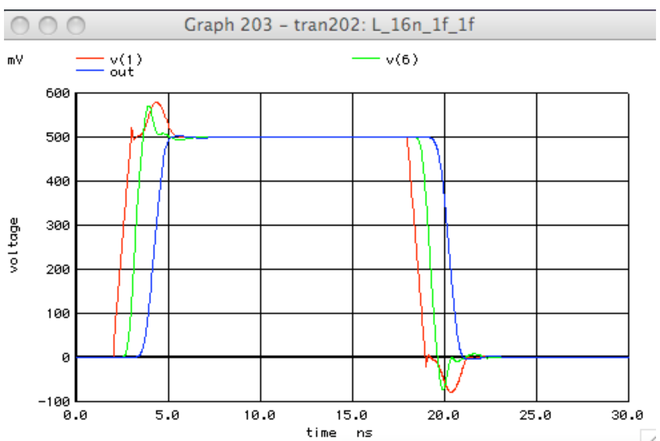
The question is whether a discontinuity in a 50 ohm transmission line can be tweeked out.

The transmission line is depending on everything resonating at 50 ohms.

If anything introduces inductance in the path, can some stray capacitance be added such that the reflections can be tweeked out?

With the 16nH stray inductance in place, the reflection is apparent.

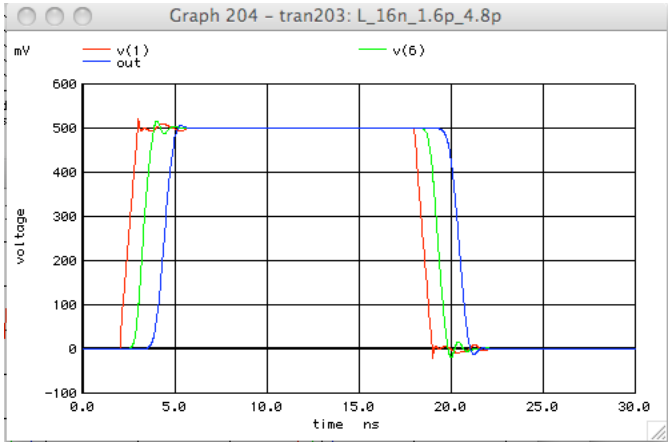
***#1===First_The_Addition_Of_16nH_of_Stray_Inductance=====**
run
plot v(1) v(6) out title L_16n_1f_1f



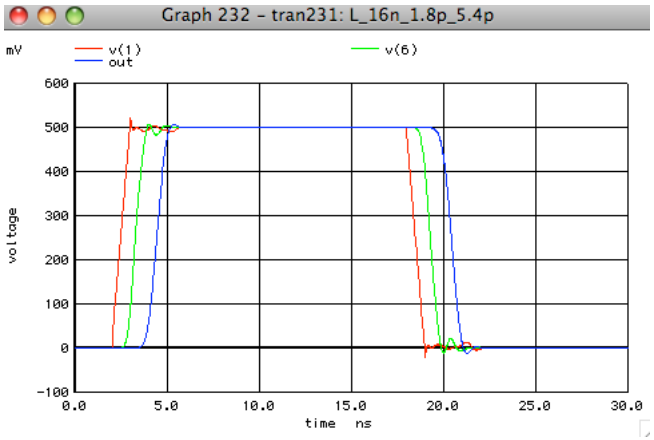
The reflection happens at v(6).

But stray capacitors CD1 and CD2 are next added to get all nodes to resonate at 50 Ohms.

```
*#2===Then_Capacitance_Is_Added_to_tweek_It_Out==
alter   CD1                capacitance  =   1.6p
alter   CD2                capacitance  =   4.8p
run
plot    v(1) v(6) out   title  L_16n_1.6p_4.8p
```




```
*#3===Try_Other_Capacitance_Ratios==============
alter   CD1                capacitance  =   1.8p
alter   CD2                capacitance  =   5.4p
run
plot    v(1) v(6) out   title  L_16n_1.8p_5.4p
```




```
*#4===Try_Other_Capacitance_Ratios==============
alter   CD1                capacitance  =   1.8p
alter   CD2                capacitance  =   5.0p
run
plot    v(1) v(6) out   title  L_16n_1.8p_5p
```

```
*#5===What_Happens_With_Balanced_Capacitance_?===
alter   CD1                capacitance  =   3.2p
alter   CD2                capacitance  =   3.2p
run
plot    v(1) v(6) out   title  L_16n_3.2p_3.2p
```

Having CD1 = CD2 does not appear to be optimum.