LC_transLine_1speed

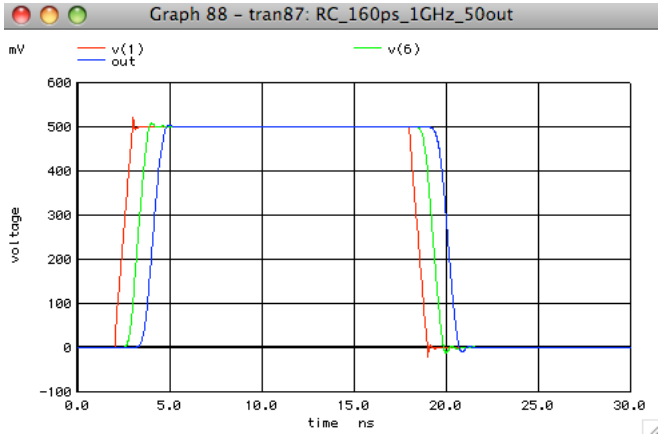
```
*
*           RIN         1     2    3     4      5     6    7     8     9     10
*   VIN
*       ___/\  /\  /\____|LC1|_|LC1|_|LC1|_|LC1|_|LC1|_|LC1|_|LC1|_|LC1|_|LC1|_|LC1|__|OUT|
*     _|__   \/  \/   _|_ |___| |___| |___| |___| |___| |___| |___| |___| |___| |___|  |___|
*    /    \          ___   _|_   _|_   _|_   _|_   _|_   _|_   _|_   _|_   _|_   _|_     |__
*   //\    \    CIN   |    ///   ///   ///   ///   ///   ///   ///   ///   ///   ///     |  _|_
*   \   \_//         _|_                                                                | ___  COUT
*    \____/          ///                                               __/\  /\  /\____|  |
*      _|_                                                            _|_  \/  \/ ROUT   _|_
*      ///                                                            ///                ///
*
*              www.idea2ic.com dsauersanjose@aol.com  4/15/08

.OPTIONS  GMIN=1e-18    METHOD=euler   ABSTOL=1e-18  TEMP=27 srcsteps = 1  gminsteps = 1
VIN       VIN    0      PWL( 0 0 2n 0 3.0n 1  18n 1 19.0n 0)
RIN       VIN    1      50
C1        VIN    0      1.6p
XLC1      1      2      LC1
XLC2      2      3      LC1
XLC3      3      4      LC1
XLC4      4      5      LC1
XLC5      5      6      LC1
XLC6      6      7      LC1
XLC7      7      8      LC1
XLC8      8      9      LC1
XLC9      9      10     LC1
XLC10     10     OUT    LC1
C2        OUT    0      -1.6p

ROUT      OUT    0      50
C3        OUT    0      10f
.tran     0.01n   30n 0 30n
.control
*#1===First_Test_Reflection_at_50_Ohms=====
run
plot    v(1) v(6) out   title  RC_160ps_1GHz_50out
*#2===First_Test_Reflection_at_100_Ohms=====
alter   ROUT              resistance   =    100
run
plot    v(1) v(6) out   title  RC_160ps_1GHz_100out
*#3===First_Test_Reflection_at_20_Ohms=====
alter   ROUT              resistance   =    20
run
plot    v(1) v(6) out   title  RC_160ps_1GHz_20out
.endc

.SUBCKT  LC1  IN     OUT
L1      IN   OUT   8n
C1      OUT  0     3.2p
.ENDS   LC1

*                              .SUBCKT LC1 IN OUT
*          _ _ _    L1
*         / \/ \/ \
*   |IN |_| () () |___|OUT|     |IN |__|         |___|OUT|
*   |___|             |   |___|     |___|  |   LC1   |   |___|
*                     |                    |_________|
*                    _|_  C1                    |
*                    ___                       _|_
*                     |                        ///
*                    _|_
*                    ///    8nH_3.2pF =>50Ohms @ 1Ghz  50*3.2p =160ps
*
*   http://www.idea2ic.com/PlayWithJavascript/L_C_R_F.html
.end

=====================END_OF_SPICE============================
```

***#1===First_Test_Reflection_at_50_Ohms=====**

Capacitors C1 and C2 are added such that each inductor see 1.6pF on each of its sides. The subcircuit is modeled as a simple LC

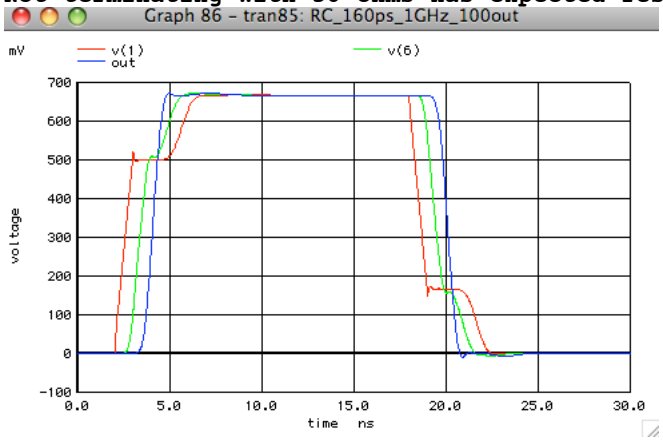
for simplity sake.

**Thinking in terms of 50 OHms and 3.2ps,
the total delay is 10 time constants
of 160ps whcih is 1.6nsec.**



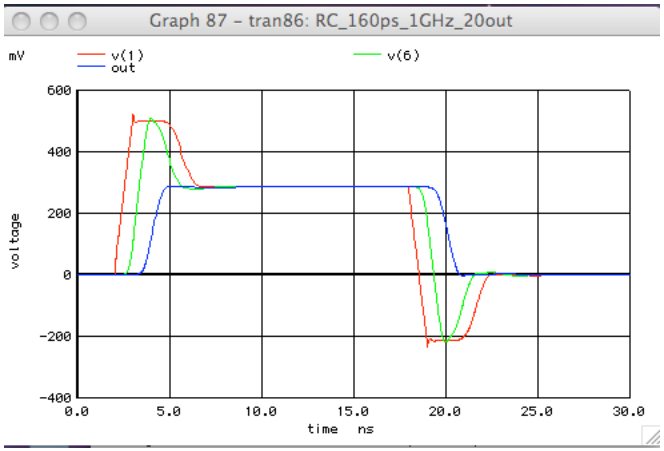
***#2===First_Test_Reflection_at_100_Ohms=====**

Not terminating with 50 ohms has expected results.



**The voltage divider effect for any voltage
has a effective 10*(50_Ohms)(3.2pF) delay
from the output reflected back to the input.**

***#3===First_Test_Reflection_at_20_Ohms=====**


Graph 87 - tran86: RC_160ps_1GHz_20out
mV
v(1)
out
v(6)
600
400
200
0
-200
-400
voltage
0.0
5.0
10.0
15.0
20.0
25.0
30.0
time ns