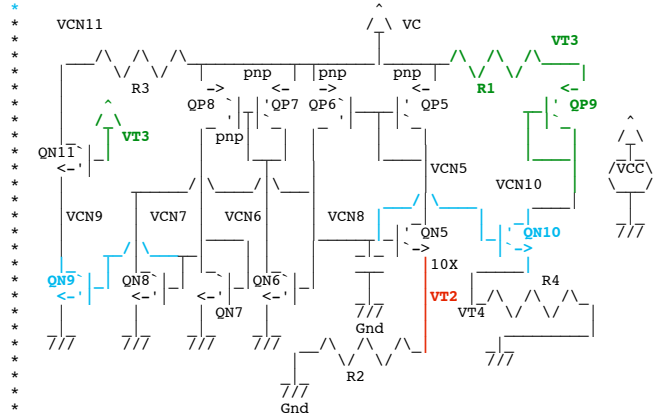


**Balanced\_BandGap\_4\_Biasing.cir**

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 \* www.idea2ic.com



Patent No.: US 6,614,293 B1

```
.OPTIONS gminsteps = 1
*****
VCC      VC      0      DC      5
QN5      VCN5   VCN8   VT2      NPN1   10
QN6      VCN6   VCN8   0        NPN1   1
QN7      VCN7   VCN7   0        NPN1   1
QN8      VCN8   VCN7   0        NPN1   1
QN9      VCN9   VCN7   0        NPN1   1
QN10     VCN10  VCN8   VT4     NPN1   10
QN11     VCN11  VT3     VCN9    NPN1   1
QP5      VCN5   VCN5   VC      PNP1   1
QP6      VCN8   VCN5   VC      PNP1   1
QP7      VCN6   VCN6   VC      PNP1   1
QP8      VCN7   VCN6   VC      PNP1   1
QP9      VCN10  VCN10  VT3     PNP1   10
R2      VT2     0        60K
R1      VT3     VC      60K
R3      VCN11  VC      60K
R4      VT4     0        60K
C2      VCN8   0        1P
.dc      VCC      .8      5      .05
```

\*#0====Can\_The\_Balanced\_BandGap\_Balances\_Out\_A\_Load====

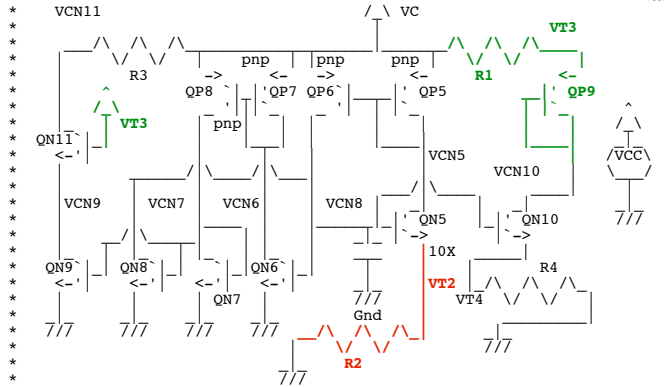
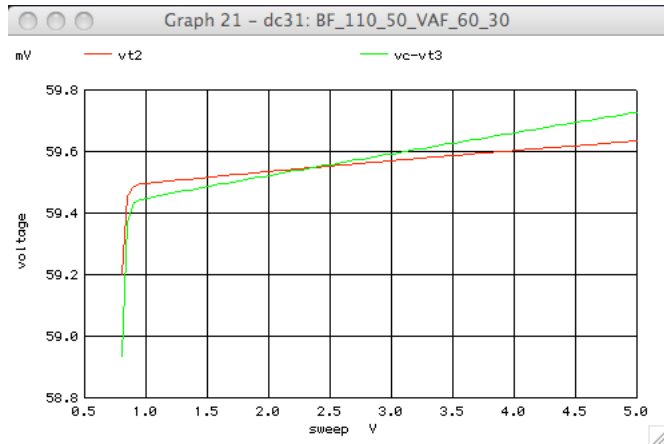
```

.control
*#1====Start_Off_With_Normal_Levels_Of_Beta_And_VAF====
run
echo "====bf set to 110 for NPN===="
plot vt2 vc-vt3 title BF_110_50_VAF_60_30
*#2====Test_The_Effects_Of_Cutting_NPN_Beta_BY_50%====
altermod npn1 bf=50
run
plot vt2 vc-vt3 title BF_50_50_VAF_60_30
echo "====set bf to 50 for NPN===="
*print vt2 vc-vt3
*#3====Test_The_Effects_Of_Cutting_PNP_Beta_BY_50%====
altermod npn1 bf=110
altermod pnp1 bf=25
run
plot vt2 vc-vt3 title BF_110_25_VAF_60_30
*#4====Test_The_Effects_Of_Cutting_NPN_VAF_BY_50%====
altermod pnp1 bf=50
altermod npn1 vaf=30
run
plot vt2 vc-vt3 title BF_110_50_VAF_30_30
*#5====Test_The_Effects_Of_Cutting_PNP_VAF_BY_50%====
altermod npn1 vaf=60
altermod pnp1 vaf=15
run
plot vt2 vc-vt3 title BF_110_50_VAF_60_15
echo "====set bf to 25 for PNP===="
.endc
.model NPN1 NPN( BF=110 VAF=60 )
.model PNP1 PNP( BF=50 VAF=30 )
.end

```

```
*#1====Start_Off_With_Normal_Levels_Of_Beta_And_VAF====
```

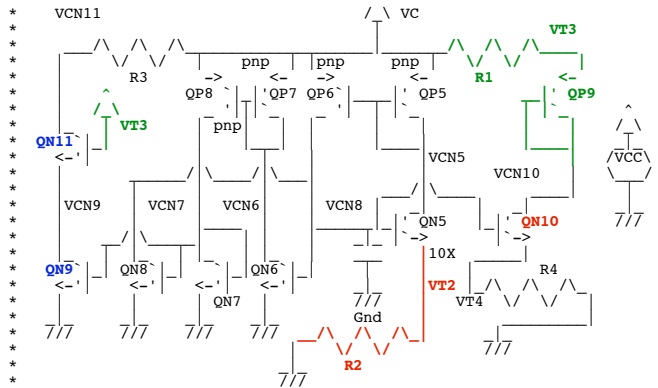
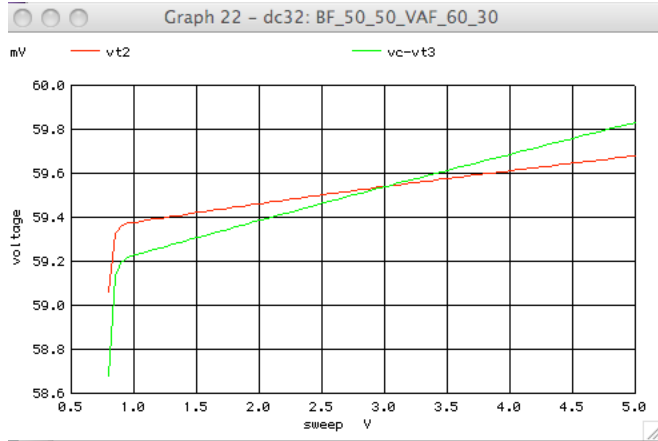
```
run
plot vt2 vc-vt3 title BF_110_50_VAF_60_30
```



The Goal is to make a current through R1 always equal R2

```
*#2====Test_The_Effects_Of_Cutting_NPN_Beta_BY_50%====
```

```
altermod npn1 bf=50
run
plot vt2 vc-vt3 title BF_50_50_VAF_60_30
```



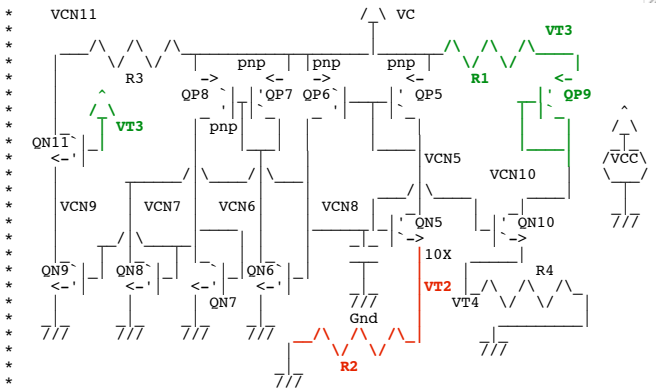
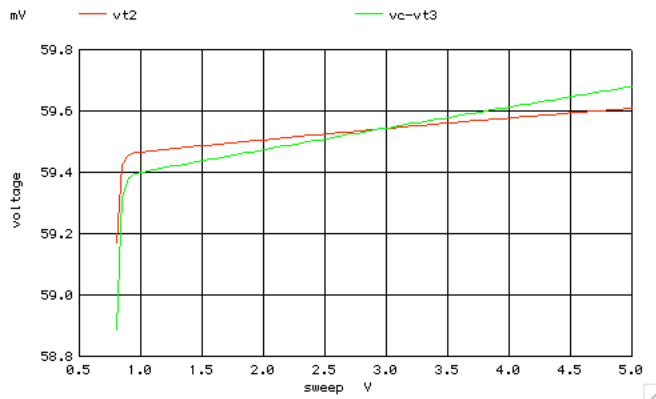
Transistors QN9, QN11 and QN10 are balanced NPN Beta Loads

```

*#3====Test_The_Effects_Of_Cutting_PNP_Beta_BY_50%====
altermod npn1 bf=110
altermod pnp1 bf=25
run
plot vt2 vc-vt3 title BF_110_25_VAF_60_30

```

Graph 23 - dc33: BF\_110\_25\_VAF\_60\_30

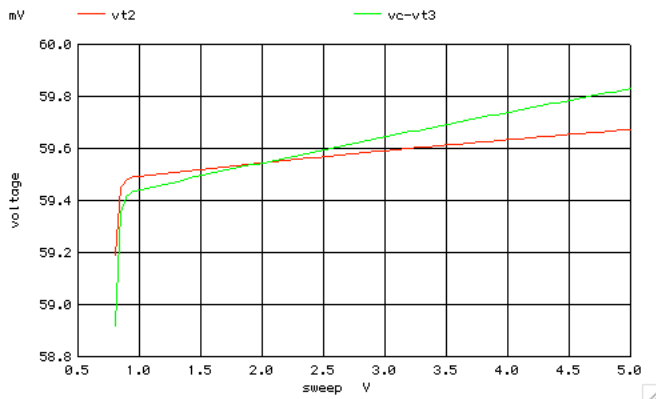


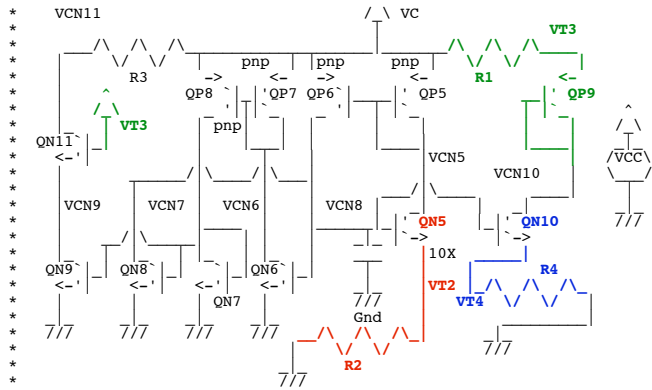
Similar methods could be used to balanced PNP Beta Loads

```

*#4====Test_The_Effects_Of_Cutting_NPN_VAF_BY_50%====
altermod pnp1 bf=50
altermod npn1 vaf=30
run
plot vt2 vc-vt3 title BF_110_50_VAF_30_30
    
```

Graph 24 - dc34: BF\_110\_50\_VAF\_30\_30





Transistors QN10 and QN5 are biased the exact same

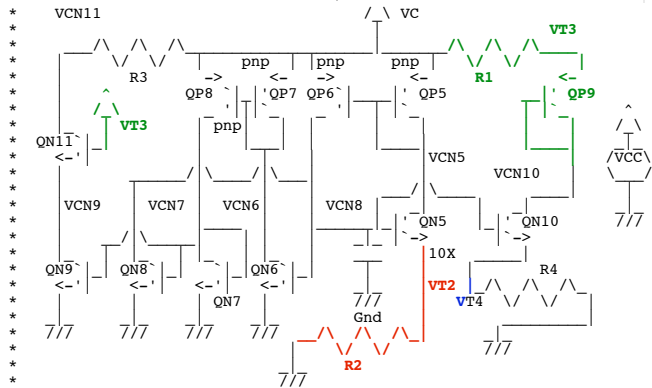
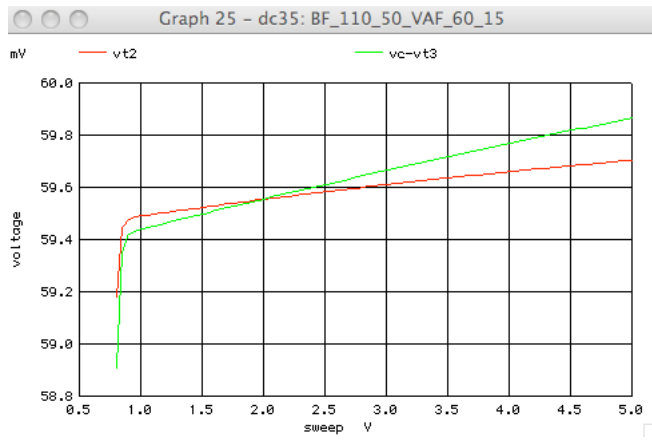
\*#5====Test\_The\_Effects\_Of\_Cutting\_PNP\_VAF\_BY\_50%====

altermod npn1 vaf=60

altermod pnp1 vaf=15

run

plot vt2 vc-vt3 title BF\_110\_50\_VAF\_60\_15



Similar methods could be used to balanced PNP VAF

A BandGap can be made as precise as it errors can be known.  
Any Known Errors can be "balanced"out.  
Precision modeling of silicon is the next step.