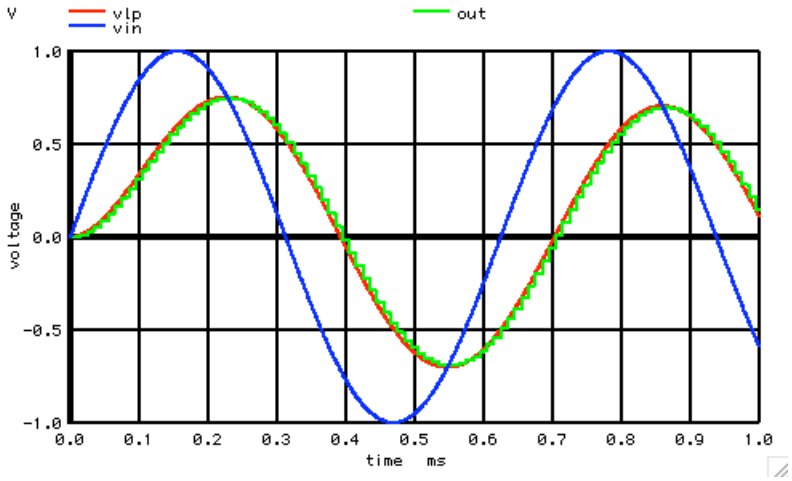
*==========Switch_Cap==========

A switch capacitor circuit shows why discreet time analog signal processing circuits need a two phase clock.

```
*
*      ______/\  /\  /\_______|VLP|
*     |       \/  \/     _|_   |___|
*     |      R1        C3 ___
*     |                    _|_
*                         7//
*     |VIN       V1
*     |_____/ _____/ _______|OUT|
*    _|_ S1 ^   |S2 ^   |    |___|
*   /_  \     |  _|_  |  _|_
* //\   \ VRE  ___ VFE  ___       R_eq  =  1/(freq_clock*C)
* \   \//       |C1      |C2            =  1/100KHz*1p
*  \___/        _|_     _|_            =  10Meg
*    _|_       7//     7//             =  1.6KHz
*   7//
```

Capacitor C1 in the circuit above is switching charge from VIN to C2. Switch S1 is closed only a short period during a rising edge of the clock. And switch S2 is on only during the falling edge.



Capacitor C1 is in effect acting just like a resistor. In this case it resembles a 10Meg resistor. Notice it has the same wave form as R1 and C3.

```
.Options  gmin = 1e-15
*V_PULSE# NODE_P NODE_N DC     VALUE  PULSE( VINIT  VPULSE TDELAY TRISE  TFALL  PWIDTH PERIOD )
VCLK      VCLK   0      DC     0      PULSE( 0      5      1n     1n     1n     5u     10u    )
XRE       VCLK   VRE    RISE_E
XFE       VCLK   VFE    FALL_E
*V_SIN#   NODE_P NODE_N DC     VALUE  SIN(    V_DC   AC_MAG FREQ   DELAY  FDamp)
VIN       VIN    0      DC     0      SIN(   0      1      1.6k                )
*SXXXXXX  N+     N-     NC+    NC-    MODEL        <ON><OFF>
S1        VIN    V1     VRE    0      SWP
S2        V1     OUT    VFE    0      SWP
C1        V1     0      1p
C2        OUT    0      10p
R1        VIN    VLP    10Meg
C3        VLP    0      10p
.MODEL    SWP    SW(    VT=2.6 VH=.2  RON=1m  ROFF=100MEG)
.control
*TRAN     TSTEP  TSTOP  TSTART TMAX
tran      1u     1m     0       1u
set       pensize = 2
plot      vlp out vin
.endc
```

```
===========Full_Netlist_For_Copy_Paste=======================
Switch_Cap
*      ________________________
*    _|_     _|__           __|_
*   /_  \   |    |         |    |
*  //\   \  |RISE|_|VRE|   |FALL|_|VFE|
*  \   \//  |____| |___|   |____| |___|
*   \___/
*    _|_  VIN
*    ///
*
*     ______/\  /\  /\________|VLP|
*    |        \/  \/     _|_  |___|
*    |      R1        C3 ___
*    |                    _|_
*    |                    ///
*    |VIN      V1
*    |_____/ ______/ ________|OUT|
*   _|_ S1 ^     |S2 ^   |   |___|
*  /_  \   |    _|_ |   _|_
* //\   \ VRE   ___ VFE ___        R_eq  =  1/(freq_clock*C)
* \   \//        |C1     |C2              =  1/100KHz*1p
*  \___/        _|_     _|_               =  10Meg
*   _|_         ///     ///               =  1.6KHz
*   ///
.Options  gmin = 1e-15
*V_PULSE# NODE_P NODE_N DC     VALUE  PULSE( VINIT  VPULSE TDELAY TRISE  TFALL  PWIDTH PERIOD )
VCLK      VCLK   0      DC     0      PULSE( 0      5      1n     1n     1n     5u     10u    )
XRE       VCLK   VRE    RISE_E
XFE       VCLK   VFE    FALL_E
*V_SIN#   NODE_P NODE_N DC     VALUE  SIN(   V_DC   AC_MAG FREQ   DELAY  FDamp)
VIN       VIN    0      DC     0      SIN(   0      1      1.6k                 )
*SXXXXXX  N+     N-     NC+    NC-    MODEL         <ON><OFF>
S1        VIN    V1     VRE    0      SWP
S2        V1     OUT    VFE    0      SWP
C1        V1     0      1p
C2        OUT    0      10p
R1        VIN    VLP    10Meg
C3        VLP    0      10p
.MODEL    SWP    SW(    VT=2.6 VH=.2  RON=1m  ROFF=100MEG)
.control
*TRAN     TSTEP  TSTOP  TSTART TMAX
tran      1u     1m     0       1u
set       pensize = 2
plot      vlp out vin
.endc
*=========Rising_Edge========================
.SUBCKT   RISE_E VIN    OUT
 R1       VIN    VTD    200k
 C1       VTD    0      1p
 BRE      OUT    0      V = 5*u(V(VIN)-V(VTD)-.1)
.ENDS     RISE_E
*
* |VIN|_/\  /\  /\_ VTD    ___|OUT|
* |___|   \/  \/  _|_     _|_ |___|
*              C1 ___    /BRE\
*      R1          |     \___/
*                 _|_     _|_
*                 ///     ///
*=========Falling_Edge========================
.SUBCKT   FALL_E VIN    OUT
 R1       VIN    VTD    200k
 C1       VTD    0      1p
 BRE      OUT    0      V = 5*u(V(VTD) -V(VIN)-.1)
.ENDS     FALL_E
*
* |VIN|_/\  /\  /\_ VTD    ___|OUT|
* |___|   \/  \/  _|_     _|_ |___|
*              C1 ___    /BRE\
*      R1          |     \___/
*                 _|_     _|_
*                 ///     ///
*=============================================
.end


4.11.10_4.54PM
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