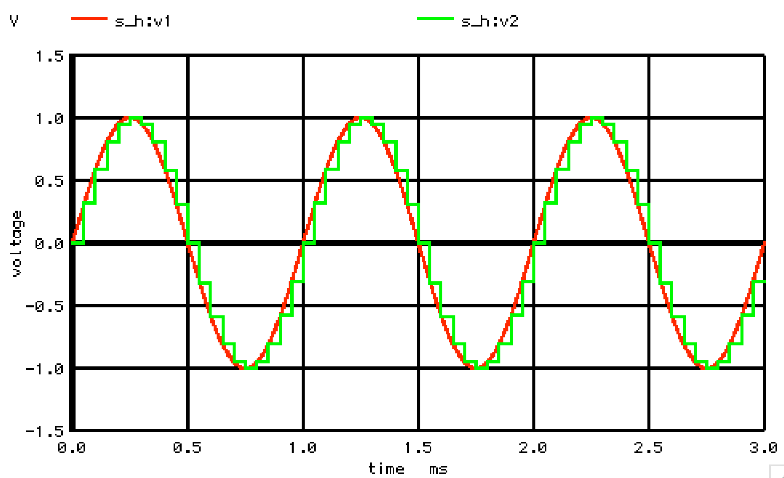
```
*=============Sample_Hold_SubCircuit=========================
```

Perhaps the simplest discreet time format of analog signal processing is a sample-an-hold. This function is just a switch and a capacitor followed by a buffer.

```
*=========Sample_And_Hold========================
.SUBCKT   S_HOLD  IN     OUT    CNT
*SXXXXXX  N+      N-     NC+    NC-    MODEL        <ON><OFF>
 S1       V1      V2     CNT    0      SWP
 BIN      V1      0      V =    V(IN)
 C1       V2      0      30n
 BOUT     OUT     0      V =    V(V2)
.ENDS     S_HOLD
*
*                                               |CNT|
*        |\          S1         |\              |___|
*  |IN|_|  \___/  ________|  \__|OUT|         ___|___
*  |___|  |  /      :       _|_  |  /  |___|   |IN|__|S+H|_|OUT|
*        |/      CNTL      ___  |/           |___|  |____|  |___|
*                           |
*      BIN               /// BOUT
*
============================================================================
```

The switch is usually controlled by a short pulse such that most of the time the switch is open.




```
============================================================================
Sample_Hold_SubCircuit
*
*                      |CNT|
*                      |___|
*                       _|_
*         _____|IN|__|S+H|_|OUT|
*       _|_   |___|  |____| |___|
*      /   \
*     //\   \
*     \   \//
*      \___/
*       _|_
*       ///
*
.Options  gmin = 1e-15
*V_SIN    NODE_P NODE_N DC     VALUE  SIN(   V_DC   AC_MAG FREQ   DELAY  FDamp)
VIN       IN     0      DC     0      SIN(   0      1      1k            )
*V_PULSE  NODE_P NODE_N DC     VALUE  PULSE( VINIT  VPULSE TDELAY TRISE  TFALL  PWIDTH PERIOD )
VCNTL     VCNT   0      DC     0      PULSE( 0      5      1n     1n     1n     1u     50u    )
XS_H      IN     OUT    VCNT   S_HOLD
.MODEL    SWP    SW(    VT=2.6 VH=.2  RON=1m  ROFF=10MEG)
.control
*TRAN     TSTEP  TSTOP  TSTART TMAX
 tran     1u     3m     0       1u
 set      pensize = 2
 plot     s_h:v1 s_h:v2
 plot     in out
.endc
============================================================================
```

```
============Full_Netlist_For_Copy_Paste========================
Sample_Hold_SubCircuit
*
*                  |CNT|
*                  |___|
*                  __|__
*       _____|IN |__|S+H |_|OUT|
*    _|_     |___|  |____| |___|
*   / _ \
*  //  \ \
*  \    \//
*   \___/
*    _|_
*    ///
*
.Options  gmin = 1e-15
*V_SIN    NODE_P NODE_N DC     VALUE  SIN(   V_DC   AC_MAG FREQ   DELAY  FDamp)
VIN       IN     0      DC     0      SIN(   0      1      1k                  )
*V_PULSE  NODE_P NODE_N DC     VALUE  PULSE( VINIT  VPULSE TDELAY TRISE  TFALL  PWIDTH PERIOD )
VCNTL     VCNT   0      DC     0      PULSE( 0      5      1n     1n     1n     1u     50u    )
XS_H      IN     OUT    VCNT   S_HOLD
.MODEL    SWP    SW(    VT=2.6 VH=.2  RON=1m  ROFF=10MEG)
.control
*TRAN     TSTEP  TSTOP  TSTART TMAX
 tran     1u     3m     0       1u
 set      pensize = 2
 plot     s_h:v1 s_h:v2
 plot     in out
.endc
*=========Sample_And_Hold=========================
.SUBCKT   S_HOLD IN     OUT    CNT
*SXXXXXX  N+     N-     NC+    NC-    MODEL        <ON><OFF>
 S1       V1     V2     CNT    0      SWP
 BIN      V1     0      V =    V(IN)
 C1       V2     0      30n
 BOUT     OUT    0      V =    V(V2)
.ENDS     S_HOLD
*
*                                                   |CNT|
*          |\       S1       |\                     |___|
*  |IN |_| \___/ ________| \__|OUT|              __|__
*  |___| | /      :    _|_ | /  |___|   |IN |__|S+H |_|OUT|
*        |/     CNTL   ___ |/           |___|  |____| |___|
*                      _|_
*      BIN             /// BOUT
*
*==============================================
.end
```

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