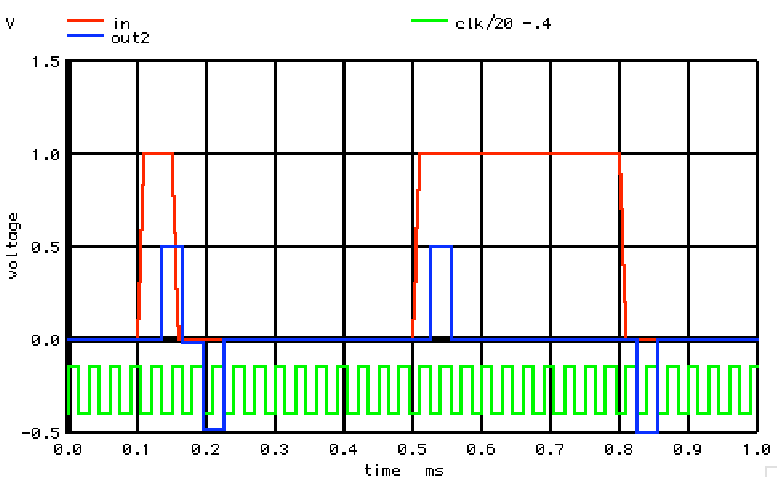
*=============**Running_Delta**========================

High pass filters are looking for inconsistency in the input signal. A common technique is to do a lowpass filter of a signal, and then subtract the lowpass from the input

```
================================================================
RUNNING_DELTA
*
*
*                  |CLK|           |CLK|
*                  |___|           |___|
*                ___|___         ___|___
*      ___|IN  |__|ADELAY|_|V2  |__|ADELAY|_|V3  |
*     _|_ |____|  |______| |____|  |______| |____|
*    /   \        XDELAY1           XDELAY2
*   //‾\  \
*   \   \//
*    \___/
*     _|_              1K           R 500
*     ///       R1               __/\  /\  /\_
*          V2 __/\  /\  /\__|      \/  \/    |
*                 \/  \/    |                |
*                R2         | |\             |
*          V3  __/\  /\  /\_|__|-\           |
*                  \/  \/      |  \_________|_|OUT|
*                  -1K         |  /           |___|
*                            __|+/
*                           _|_|/ BOPA
*                           ///
================================================================
```

The example above is doing a simple running subtraction of the input signal. Its output wave form below shows it detects rising and falling edges.

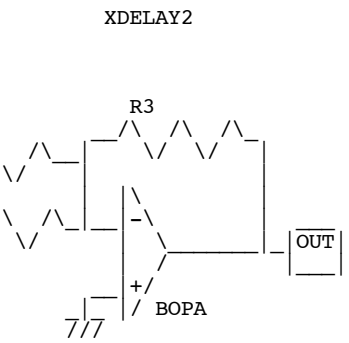


==

If one uses enough delay elements, and combine their values together in such a way that an impulse response will produce a sin(x)/x waveform, then subtracting that sinc signal from the input signal will produce something like a perfect brick-wall high pass filter.

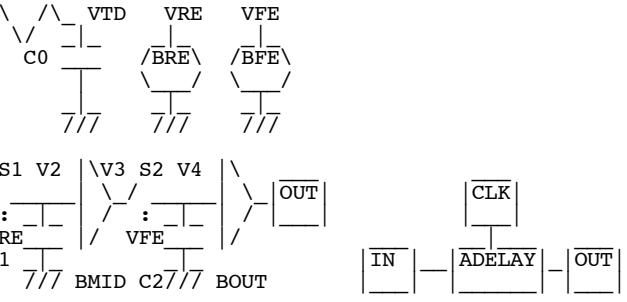
===========**Full_Netlist_For_Copy_Paste**=======================

```
RUNNING_DELTA
*
*
*                  |CLK|           |CLK|
*                  |___|           |___|
*                ___|___         ___|___
*      ___|IN  |__|ADELAY|_|V2  |__|ADELAY|_|V3  |
*     _|_ |____|  |______| |____|  |______| |____|
```




```
*
*V_PULSE# NODE_P NODE_N DC     VALUE  PULSE( VINIT  VPULSE TDELAY TRISE  TFALL  PWIDTH PERIOD )
VCLK      CLK    0      DC     0      PULSE( 0      5       1n     1n     1n     15u     30u    )
*V_PWL#   NODE_P NODE_N DC     VALUE  PWL(   T1     V1      T2     V2     T3     V3      ...>)
VIN       IN     0      DC     0      PWL(   0 0    .1m 0   .11m 1 .15m 1 .16m 0 .5m 0  .51m 1 .8m 1  .81m 0
)
XDELAY1   IN     V2     CLK    ADelay
XDELAY2   V2     V3     CLK    ADelay
BOPA      OUT    0      V=     5*tanh( V(VINN)*1000)
R1        V2     VINN   1K
R2        V3     VINN   -1K
R3        VINN   OUT    500

.MODEL    SWP    SW(    VT=2.6 VH=.2  RON=1  ROFF=10MEG)
.control
*TRAN     TSTEP  TSTOP  TSTART TMAX
 tran     1u     1m     0      1u
 set      pensize = 2
 let      out2   = -out
 plot     in     clk/20 -.4   out2    ylimit -.5 1.5
.endc
*=========Analog_Delay=========================
.SUBCKT   ADelay IN     OUT    CLK
 R0       CLK    VTD    100k
 C0       VTD    0      1p
 BRE      VRE    0      V = 5*u(V(CLK) -V(VTD)-.1)
 BFE      VFE    0      V = 5*u(V(VTD) -V(CLK)-.1)
*SXXXXXX  N+     N-     NC+    NC-    MODEL
 S1       V1     V2     VRE    0      SWP
 S2       V3     V4     VFE    0      SWP
 C1       V2     0      30n
 C2       V4     0      30n
 BIN      V1     0      V =    V(IN)
 BMID     V3     0      V =    V(V2)
 BOUT     OUT    0      V =    V(V4)
.ENDS     ADelay
*
```




```
*
*==============================================
.end
```

4.11.10_4.54PM
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