*==========**Running_Average**==========

A Finite Impulse Response (FIR) Digital filter involves combining signals from a finite number of delay elements. Three delay elements are being used in the case below. This example is doing a running average of the three delays.

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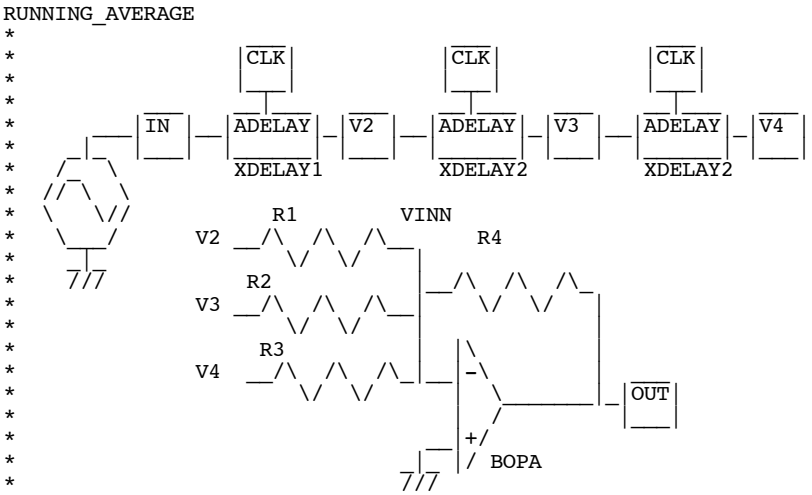
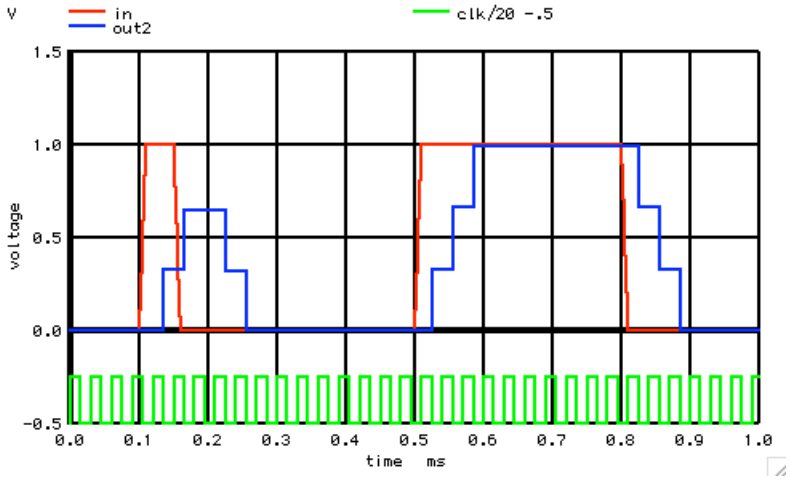
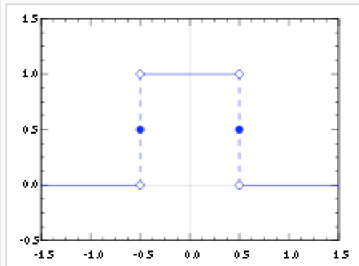


==========

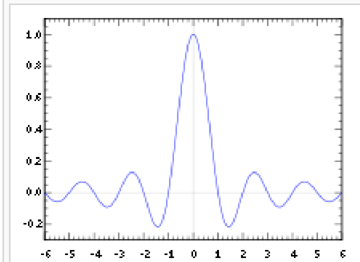
The output waveforms are simple averages. The first analog input pulse is longer than a delay, so at one point in time, signal will be in two delay elements. The second analog input pulse is long enough to show the averaging of analog signal over three delay elements.



If one uses enough delay elements, and combine their values together in such a way that an impulse response will produce a sin(x)/x waveform at the output, then the filter will behave something like a perfect brick-wall lowpass filter.



The rectangular function, the frequency response of the sinc filter.



The normalized sinc function, the impulse response of the sinc filter.

In general, low pass filtering is mainly averaging a signal with a signal's past. An RC filter just averages the input signal. Low pass filters are looking for consistency in the input signal.

```
===========Full_Netlist_For_Copy_Paste========================
RUNNING_AVERAGE
*
*
*                   |CLK|              |CLK|              |CLK|
*                   |___|              |___|              |___|
*                     |                  |                  |
*          ___|IN |__|ADELAY|_|V2 |__|ADELAY|_|V3 |__|ADELAY|_|V4 |
*       _|_   |___|  |______| |___|  |______| |___|  |______| |___|
*      /_  \          XDELAY1             XDELAY2            XDELAY2
*     //\ \
*     \   \//                R1         VINN
*      \___/        V2  __/\  /\  /\__       R4
*        _|_                  \/  \/   |
*        ///              R2           |__/\  /\  /\_
*                   V3  __/\  /\  /\__ |      \/  \/  |
*                             \/  \/   |              |
*                           R3         |  |\          |
*                   V4   __/\  /\  /\_|__|-\          |
*                              \/  \/      \________|_|OUT|
*                                         /           |___|
*                                     ___|+/
*                                   _|_  |/ BOPA
*                                   ///
*
*V_PULSE# NODE_P NODE_N DC     VALUE   PULSE( VINIT  VPULSE TDELAY TRISE  TFALL  PWIDTH PERIOD )
VCLK      CLK    0      DC     0       PULSE( 0      5      1n     1n     1n     15u    30u    )
*V_PWL#   NODE_P NODE_N DC     VALUE   PWL(   T1     V1     T2     V2     T3     V3     ...>)
VIN       IN     0      DC     0       PWL( 0 0 .1m 0 .11m 1 .15m 1 .16m 0 .5m 0 .51m 1 .8m 1 .81m 0 )
XDELAY1   IN     V2     CLK    ADelay
XDELAY2   V2     V3     CLK    ADelay
XDELAY3   V3     V4     CLK    ADelay
BOPA      OUT    0      V=     5*tanh( V(VINN)*1000)
R1        V2     VINN   1K
R2        V3     VINN   1K
R3        V4     VINN   1K
R4        VINN   OUT    330

.MODEL    SWP    SW(    VT=2.6 VH=.2  RON=1  ROFF=10MEG)
.control
*TRAN     TSTEP  TSTOP  TSTART TMAX
 tran     1u     1m     0      1u
 set      pensize = 2
 let      out2   = -out
 plot     in     clk/20 -.5   out2    ylimit -.5 1.5
.endc
*=========Analog_Delay========================
.SUBCKT   ADelay IN     OUT    CLK
 RO       CLK    VTD    100k
 CO       VTD    0      1p
 BRE      VRE    0      V = 5*u(V(CLK) -V(VTD)-.1)
 BFE      VFE    0      V = 5*u(V(VTD) -V(CLK)-.1)
*SXXXXXX  N+     N-     NC+    NC-    MODEL
 S1       V1     V2     VRE    0      SWP
```

```
 S2       V3     V4     VFE    0      SWP
 C1       V2     0      30n
 C2       V4     0      30n
 BIN      V1     0      V =    V(IN)
 BMID     V3     0      V =    V(V2)
 BOUT     OUT    0      V =    V(V4)
.ENDS     ADelay
*  ___
* |CLK|_/\  /\  /\_ VTD   VRE   VFE
* |___|   \/  \/  _|_    _|_   _|_
*              C0 ___   /BRE\  /BFE\
*       R0         |    \___/  \___/
*                 _|_    _|_    _|_
*                 ///    ///    ///
*
*  ___  |\V1 S1 V2 |\V3 S2 V4 |\   ___            ___
* |IN |_| \_/ _____| \_/ _____| \_|OUT|          |CLK|
* |___| | /  : _|_ | /  : _|_ | / |___|          |___|
*       |/  VRE___ |/  VFE___ |/          ___    __|___   ___
*           C1 _|_         _|_            |IN |__|ADELAY|_|OUT|
*      BIN     /// BMID C2/// BOUT       |___|  |______| |___|
*
*==============================================
.end
```

4.11.10_4.54PM

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