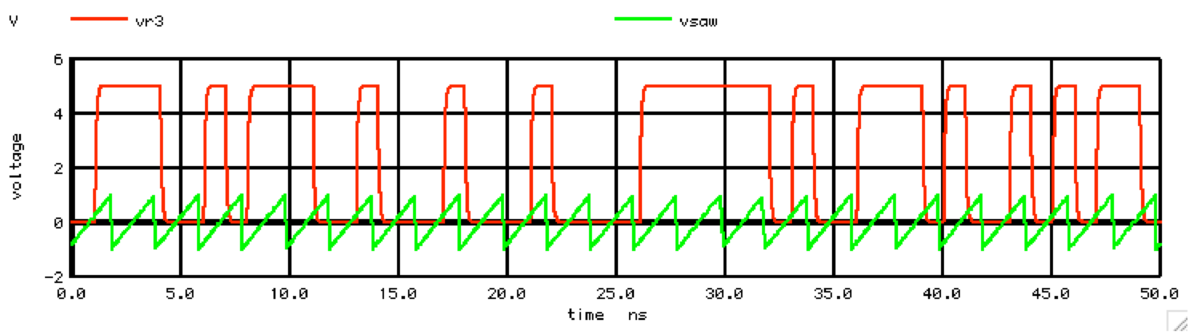
=============**Eye_Diagram_Degrade**=====================================

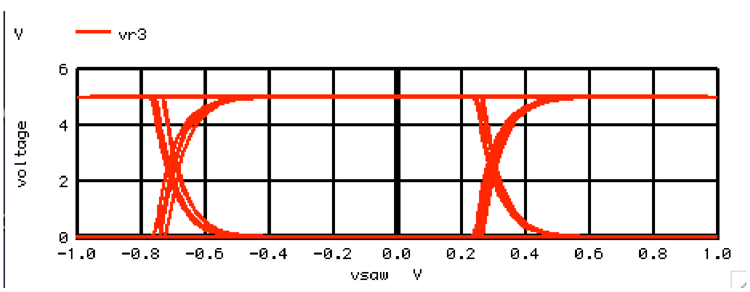
Simulating Eye Diagrams can be done using random data. Create and import a PWL_file. Clip its output and latch it with a D flip flop.

```
Eye_Diagram
*                                        XINVR1
*            V1                         |\             |\
*                 _____|  D    Q  |__|V2  |_|  \/\_|VR2|_|  \/\_|VR3|
*                   _|_  |            |   |___|  |  /\/ |___|  |  /\/ |___|
*         _____/B1 \  __|>CLK     |            |/             |/
*          _|_   \___/  |  |          | XDFF
*        /   \    _|_   |  |VCLK                    VT      VSAW
*       //   \ \  ///   |                                  _____|VR3|
*       \     \//     _|_                       _|____  |   _|____|___|
*        \___/       //   \                VT   /   \   |  /   \
*          _|_      \     \//                 //   \ \  |_//   \ \  BSAW
*          ///       \___/ VCLK               \     \//    \     \//
*       PWL_File      _|_                      \___/      \___/
*                     ///                       _|_        _|_
*                                               ///        ///
*
```



===

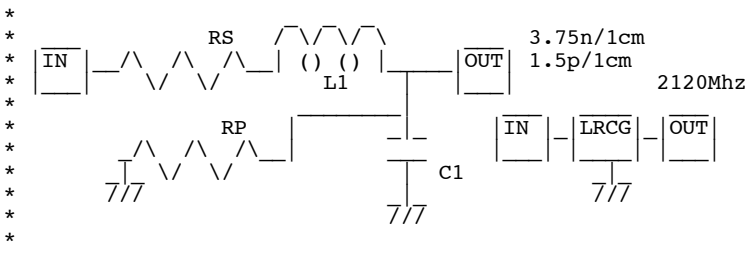
A sawtooth waveform can next be generated and the digital signal can be plotted versus the sawtooth waveform.



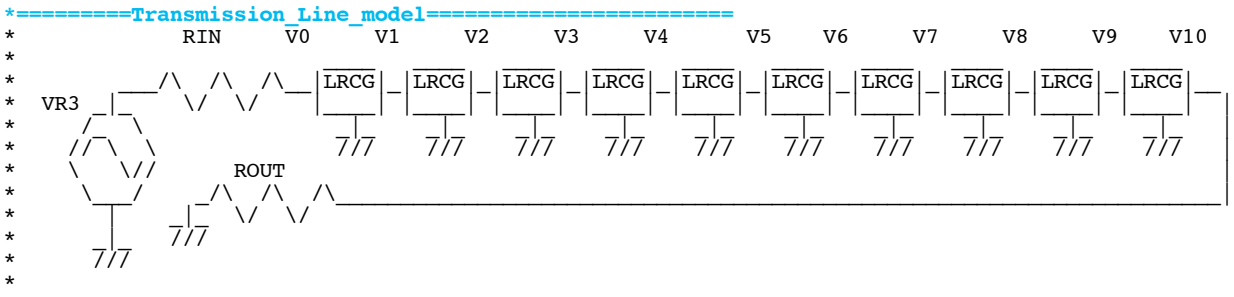
===

It might be dangerous to assume that Spice's transmission line models work correctly. In theory the transmission line is just a series of LRC circuits. Resistors Rs and Rp are often described as setting the bandwidth. But increasing the values of L1 and C1 may make it easier to see the challenges.

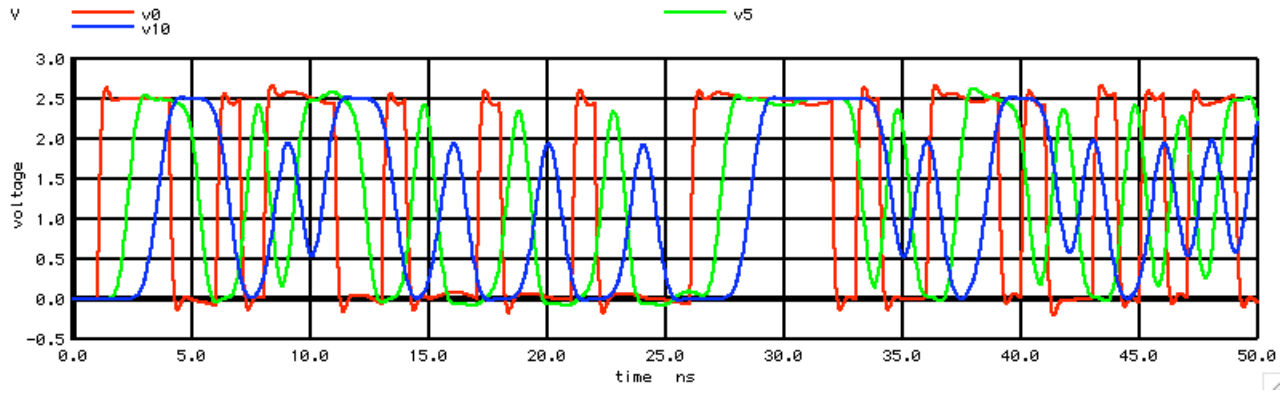
```
*=========LRCG_SubCircuit=========================
.SUBCKT    LRCG   IN     OUT
 RS        IN     INS    1m
 RBP       IN     OUT    200
 L1        INS    OUT    12n
 C1        OUT    0      4.8p
 RP        OUT    0      1meg
.ENDS      LRCG
```



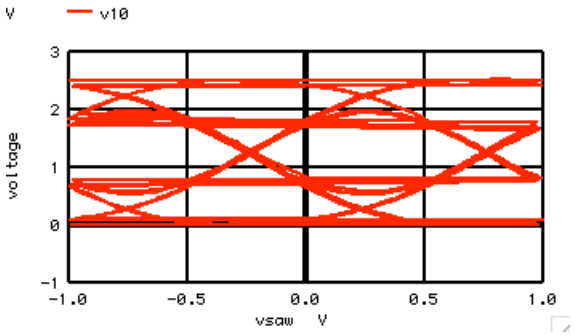
The random digital signal is inputed to a series of LRCG elements and looking at various points along the series makes it easy to see what is going on.



Low pass filtering is primarily an averaging process. All low pass filters average signal with signal that happened in the past. So a sharp pulse gets spread out over time.



This means that what happens in the past clock cycle is beginning to interfere with what is being received at present clock cycle.



When the lowpass filtering is not too complex, a high pass filter can be applied to cancel out this effect. This high pass filter can be applied at either the transmitter or receiver.

As long as the spreading out of signal over time is not too great,

one can still make out the intended transmission. And as long as one can see things in the waveform, it should be possible to apply a high pass filter. But things get a bit more challenging when the time spread out gets greater than two clock cycles.

```
===========Full_Netlist_For_Copy_Paste=======================
Eye_Diagram_degrade
* www.idea2ic.com
* dsauersanjose@aol.com  1/20/10   replace(OPT-SPACE)=>SPACE
*          XINVR1          BR2        BR3
*   ___   |\           |\          |\
*  |VIN|_|  \/\_|VR2|_|  \/\_|VR3|_|  \/\_|VR3|
*  |___| |  /\/ |___| |  /\/ |___| |  /\/ |___|
*    |   |/           |/          |/
*    |
*   _|_
*  /   \      _|_
* //\   \    /VCC\
* \   \//    \___/
*  \___/      _|_
*   _|_       ///
*   ///
*             RIN     V0     V1     V2     V3     V4      V5     V6     V7     V8     V9    V10
*
*         ___/\  /\  /\__|LRCG|_|LRCG|_|LRCG|_|LRCG|_|LRCG|_|LRCG|_|LRCG|_|LRCG|_|LRCG|_|LRCG|__
*  VR3  _|_   \/  \/     |____| |____| |____| |____| |____| |____| |____| |____| |____| |____|  |
*      /   \              _|_    _|_    _|_    _|_    _|_    _|_    _|_    _|_    _|_    _|_    |
*     //\   \             ///    ///    ///    ///    ///    ///    ///    ///    ///    ///    |
*     \   \//      ROUT                                                                        |
*      \___/    _/\  /\  /\________________________________________________________________|
*        |     _|_  \/  \/
*       _|_    ///
*       ///
*
.options srcsteps = 1 set gminsteps = 1
*=========Test_Circuit=========================
.include  PWL_File.inc
Rload     OUT    0      1k
V2PI      V2PI   0      DC     6.283185307179586
VP        VPI    0      DC     3.141592653589793
VT        VT     0      PWL    ( 0 0 1 1 )
BSAW      VSAW   0      V =    2*atan(tan(v(V2PI)*250meg*v(VT)-v(VPI)*.4))/v(VPI)
VCC       VCC    0      DC     5V
*V_PULSE  NODE_P NODE_N DC     VALUE  PULSE( VINIT  VPULSE TDELAY TRISE  TFALL  PWIDTH PERIOD )
VIN       VIN    0      DC     0      PULSE( 0      5      1p     5p     5p     .5n    1n )
VCLK      VCLK   0      DC     0      PULSE( 0      5      1p     1p     1p     50p    1n )
B1        V1IN   0      V      =      u(v(out))
XDFF      V1IN   VCLK   V2IN   VCC    D_FF
*=========MODEL_Inverters=========================
XINVR1    V2IN   VR2    VCC    INV_B
XINVR2    VR2    VR3    VCC    INV_B
C1        VR3    0      5f
*=========MODEL_Cable=========================
RIN       V2IN   V0    50
CIN       V0     0    5p
XLRCG0    V0     V1   LRCG
XLRCG1    V1     V2   LRCG
XLRCG2    V2     V3   LRCG
XLRCG3    V3     V4   LRCG
XLRCG4    V4     V5   LRCG
XLRCG5    V5     V6   LRCG
XLRCG6    V6     V7   LRCG
XLRCG7    V7     V8   LRCG
XLRCG8    V8     V9   LRCG
XLRCG9    V9     V10  LRCG
ROUT      V10    0    50
*=========Run_Sim=========================
.control
*TRAN     TSTEP  TSTOP  TSTART TMAX   ?UIC?
tran      1n     50n     0     1n
set       pensize =  2
plot      vclk  out  v2in
plot      vr3  vsaw
*plot     dff:e dff:f dff:f
plot      vr3 vs vsaw
plot      v10 vs vsaw
plot      v0 v5 v10
.endc

*=========LRCG=========================
.SUBCKT   LRCG  IN    OUT
```

```
 RS       IN    INS   1m
 RBP      IN    OUT   200
 L1       INS   OUT   12n
 C1       OUT   0     4.8p
 RP       OUT   0     1meg
.ENDS     LRCG
*
*                      _  _  _
*  ___          RS    / \/ \/ \      ___  3.75n/1cm
* |IN |__/\  /\  /\___| () () |_____|OUT| 1.5p/1cm
* |___|    \/  \/        L1     |    |___|            2120Mhz
*
*                      ________|       ___   ____   ___
*                RP    |       _|_     |IN |_|LRCG|_|OUT|
*        _/\  /\  /\___|       ___     |___| |____| |___|
*       _|_ \/  \/              |  C1          _|_
*       ///                    _|_             ///
*                              ///
*
*=========INV_B=========================
.SUBCKT   INV_B  IN     OUT    VCC
 BINV     VOUT   0      V =    .5*V(VCC)*tanh(-30*(V(IN)-.5*V(VCC))) +.5*V(VCC)
 ROUT     VOUT   OUT    300
 CIN      IN     0      1f
 COUT     OUT    0      190f
.ENDS     INV_B
*
*            VOUT
*  ___  |\                 ___
* |IN |_| \/\__/\  /\  /\_|OUT|  ROUT=600 @5V , 900@3V
* |___| | /\/    \/  \/   |___|  480ps at 6 stages
*  _|_  |/        ROUT     _|_   80ps
*  ___                     ___   rc=114  -3dBof RC
*  _|_ CIN            COUT _|_
*  ///                     ///
*
*=========D_FF=========================
.SUBCKT   D_FF   D      CLK    Q     VCC
 B5       E      0      V =    u( v(CLK)*v(D) -.5) -u( (.9-v(D))*v(CLK)-.5)
 D1       E      F      DD
 D2       F      E      DD
 C1       F      0      .5p
 B6       Q      0      V =     v(VCC)*u( v(F ))
.ends
*        _______
*   ____| D   Q |__
*
*   ____|>CLK   |
*       |_______|
*
*         E ______________
*   ___     |   D1 _|_  _|_D2     ______
*  |D  |____|_     \ /   ^       _|_   |  ___
*  |___|  /_  \    _v_  /_\  F  /_  \  |_|Q  |
*        // \  \    |____|_____// \  \   |___|
*   ___    \  \//     _|_       \  \//
*  |CLK|__\___/      ___ C1     \___/
*  |___|   _|_       _|_         _|_
*          ///       ///         ///
*
*==================Doide_Models=========================
.model            DD                 D(IS=3.15e-18 RS=100 CJO=10f )
.end
```

4.11.10_4.54PM

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