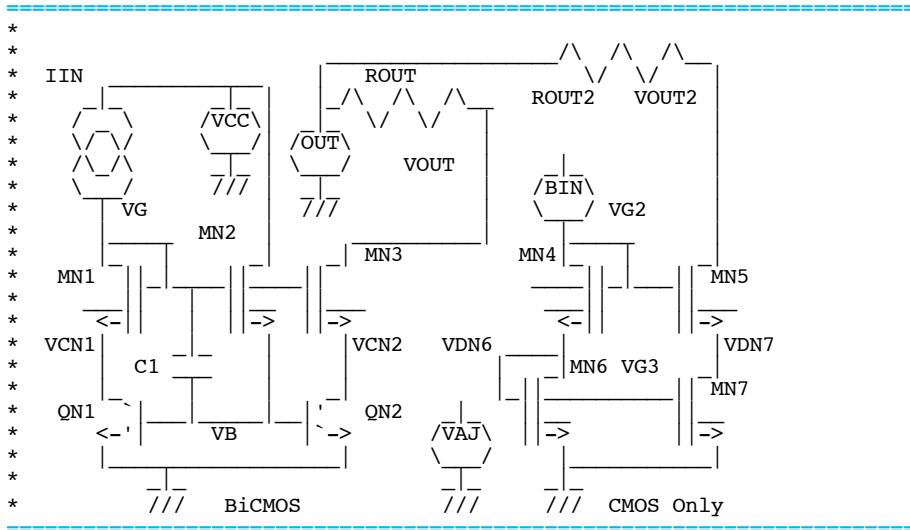


## \*=====BiCMOS\_MIRROR\_CASCODE=====

The early voltage of CMOS transistors is not very high for short channel lengths. As a result, CMOS transistors are usually in series which cascode stages. The quality of a current mirror stage could include the following.

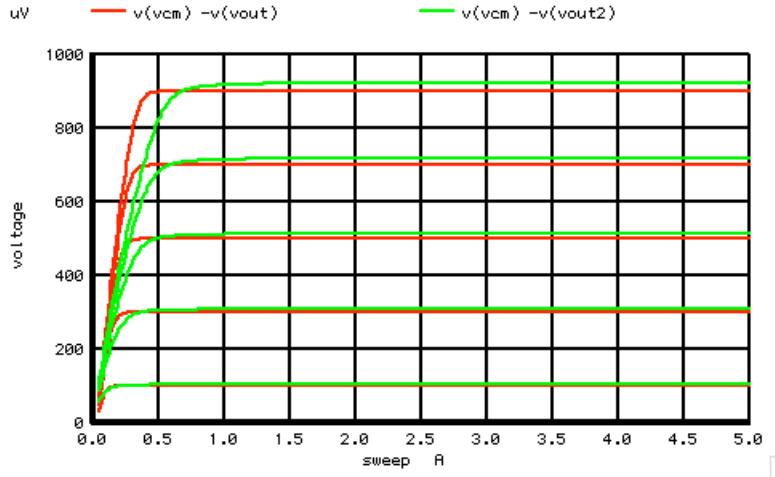
- 1) How high is the output **impedance**?
- 2) How good is the current **match**?
- 3) What is the **current dynamic range**?
- 4) How low can the **output swing**?
- 5) How much **supply voltage** is required?
- 6) How much **silicon area** is required?

A simple CMOS cascode mirror shown below on the right is being simulated next to a BiCMOS Cascode current mirror on the left. This BiCMOS current mirror is being used as a standard for comparison. Both are being done using about the same area.



Both current mirrors have **high output impedance**.

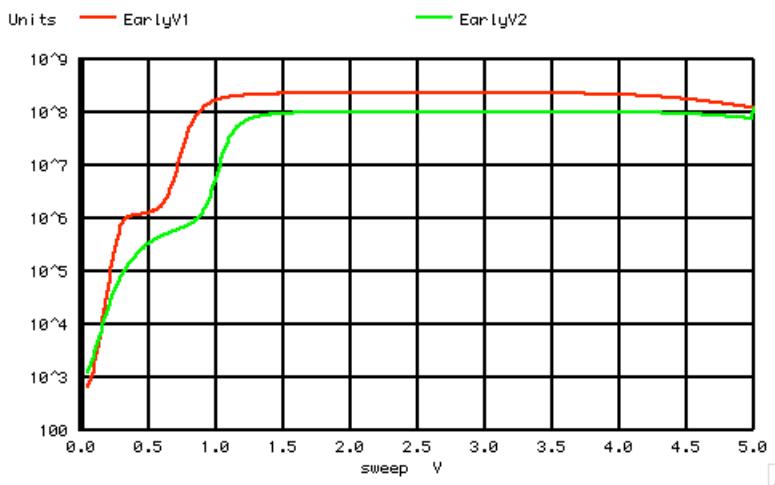
The BiCMOS current mirror is coming a lot closer to perfection since for their size bipolar transistors have much **better match**, much higher early voltage, much lower resistances, and much higher current dynamic range. Having this BiCMOS output as a background makes it easy to see whether any adjust in L or W improve the CMOS current mirror. What does it take for instance for the CMOS only stage to **swing closer to ground**? Well it takes **area**.



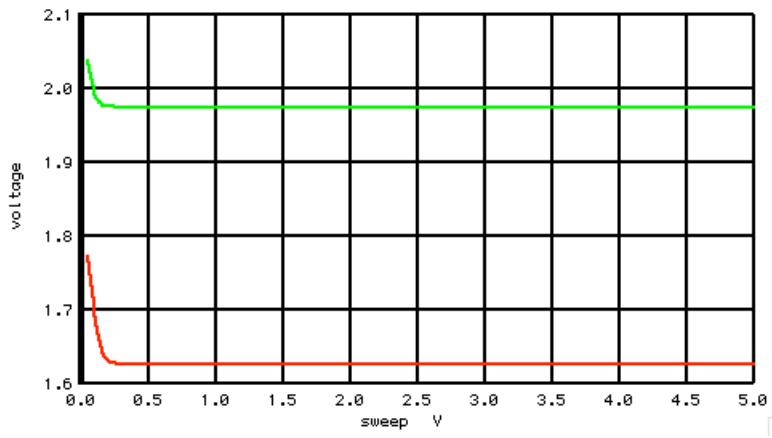
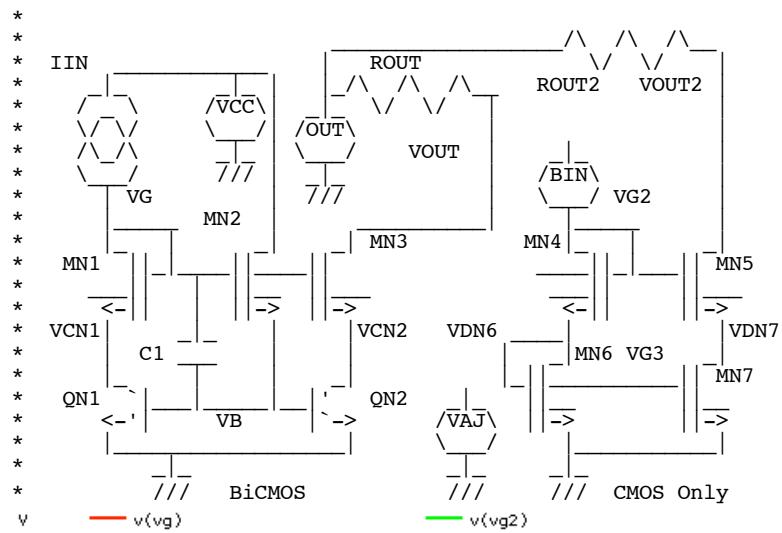
Spice has a derivative function which can make it possible to view the effective early voltage of each stage.

```
let EarlyV1 = 1/deriv(v(vcm) -v(vout))
let EarlyV2 = 1/deriv(v(vcm) -v(vout2))
```

The early voltages of both current mirrors are pretty high. When the output stage's voltage drops, the CMOS cascodes are going from current mode to resistor mode, and this shows up on the early voltage plots.



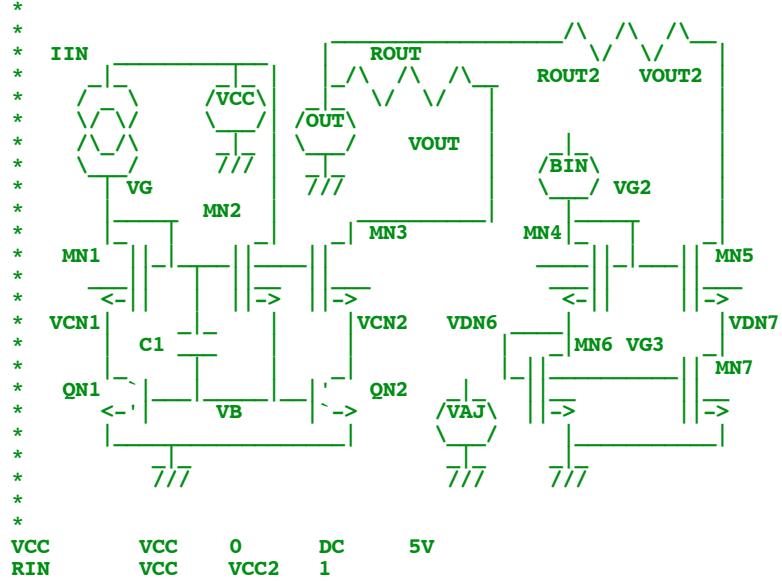
This CMOS cascode stage is making no effort to lower the **required supply voltage**. Two threshold voltages are required compared to the BiCMOS's need of a diode and a threshold.



What is not being plotted is **current dynamic range** because CMOS operation may be questionable in the subthreshold region. Bipolar transistors in a BiCMOS process can work from several millamps to pico-amps.

## =====Full\_Netlist\_For\_Copy\_Paste=====

BiCMOS\_MIRROR\_TESTS\_0



```

IIN      VCC2    VG      DC      100u
VCM      VCM     O       DC      5V
IB       VB      O       DC      1u
BIN      VCC     VG2     I       = v(vcc)-v(vcc2)
ROUT     VCM     VOUT    1
C1       VG      VB      1p
IA       VB2    O       600u
MN1      VG      VCN1   0       NMOSC   W=100u  L=1u
MN2      VCC2   VGN1   0       NMOSC   W=30u   L=1u
MN3      VOUT   VCN2   0       NMOSC   W=100u  L=1u
MN4      VG2    VDN6   0       NMOSC   W=100u  L=1u
MN5      VOUT2  VG2    VDN7   0       NMOSC   W=100u  L=1u
MN6      VDN6   VDN6   0       NMOSC   W=100u  L=1u
MN7      VDN7   VDN6   0       NMOSC   W=100u  L=1u
VAJ      VG3    O       DC      2
ROUT2    VCM     VOUT2  1
*MN1     VG      VCN1   0       NMOSC   W=300u  L=1u AD=7p AS=7p PD=10u PS=10u
QN1      VCN1   VB      0       NPNV    10.00
QN2      VCN2   VB      0       NPNV    10.00
.model   NPN1   NPN( BF=2100  VAF=216 )
.control
*DC      SOURC1  VSTART  VSTOP   VSTEP  SOURC2  START2 STOP2  STEP2
dc       vcm     .05V    5V     .01V   iin    100uA  1000uA 200uA
plot    v(vcm) -v(vout) v(vcm) -v(vout2)
*DC      SOURC1  VSTART  VSTOP   VSTEP  SOURC2  START2 STOP2  STEP2
dc       vcm     .05V    5V     .01V
let     EarlyV1 = 1/deriv(v(vcm) -v(vout))
let     EarlyV2 = 1/deriv(v(vcm) -v(vout2))
plot    EarlyV1 EarlyV2      ylog
plot    v(vg)   v(vg2)
.endc

.MODEL   NPNV   NPN(
+ IS=15.51E-18 NF=1.005  BF=110    VAF=130.2   IKF=0.0057
+          NR=1.006  BR=0.4822  VAR=4.286   IKR=0.0002472
+ ISE=9.15E-17 NE=2
+ ISC=1E-21   NC=2
+ RB=732      RBM=441.2
+ RE=15.33    RC=109.1
+ CJE=1.727E-14 VJE=0.6408 MJE=0.2563
+ CJC=1.826E-14 VJC=0.6399 MJC=0.3531
+ CJS=2.939E-14 VJS=0.3488 MJS=0.1813 XCJC=0.4201
+ TF=1.65E-11  XTF=1.25  VTF=1
+ TR=6E-09    FC=0.88  PTF=205
+ KF=1.000E-16 AF=1
+ XTB=2       EG=1.11  XTI=5    TNOM=25
.model   NMOSC   NMOS(
+ Level= 8   Tnom=27.0
*-----Process-----
+ tox=160e-10 xj=0.25e-06 nch=0.5e+17
*-----V_threshold-----
+ vth0=0.72  nlx=0.12e-06
*-----Bulk-----
+ k1=1.04    k2=-1.209E-01
+ cdsc=-2.4E-4 cdscd=-1.506E-04 cdscb=-2.219E-04
*-----mobility-----
+ u0=678     ua=8.964e-10
+ ub=1.472e-18 uc=-4.441E-17 vsat=86000
*-----Subthreshold-----
+ nfactor=1.8
+ cit=-5.0E-04 voff=-7.862E-02
+ eta0=4.441e-16 etab=-2.E-01 dsub=0.7
*-----Hot electrons-----
* alpha0=1.61e-05 beta0=36.68
*-----VAF-----
+ lint=.12e-06 pclm=.19 pscbel=3.79e+08 pscbe2=9.4e-05
+ delta=0.01655 pvag=0.4484
*-----Bulk_diode-----
+ js=5.858e-08
*-----Resistance-----
+ rsh=70     rdsw=375
+ wr=0.7586 prwb=0 prwg=-4.441E-17
*-----Capacitance-----
+ cj=0.0002424 cjsw=2.73e-10 mj=0.3551 mjsw=0.3873
+ cgso=9e-13  cgdo=9e-13 cgbo=7e-10
+ pb=0.5614   pbsw=0.8 xpart=0
+ dlc=5e-08   dwc=1.5e-07
*-----BulkChargeEffect-----
* a0=0.7     a1=0 a2=1 ags=0.05583
* b0=6.305e-08 b1=6.579e-08 keta=-1.531E-02
*-----ShortChannel-----
+ dvt0=2.2    dvt1=0.53 dvt2=-1.521E-01 drout=0.76
+ pdiblcb=.4 pdiblcl1=0.00886 pdiblcl2=0.00029
*-----NarrowChannel-----

```

```
+ w0=2.6e-04      wint=0.16e-06
+ ww=-9.525E-14   wwn=1.0
+ dvt0w=0          dvt1w=5.3e6      dvt2w=-1.E-01
+ k3=2.53          k3b=-5          dwg=0          dwb=0
*-----Noise-----
* af=1            kf=1e-28        ef=0.95
*-----Temperature-----
* pvsat=0          ute=-1.258E+00  kt1=-3.85E-01
* kt1l=0           kt2=-3.098E-02  ual=5.705e-09
* ub1=-1.147E-17   uc1=-1.302E-01 at=20380
* prt=-3.287E+02  lk1=0          lk2=0
* lvsat=0          la0=0          lags=0          lute=0
* luc=0
.end
```

4.11.10\_4.54PM  
dsauersanjose@aol.com  
Don Sauer  
<http://www.idea2ic.com/>