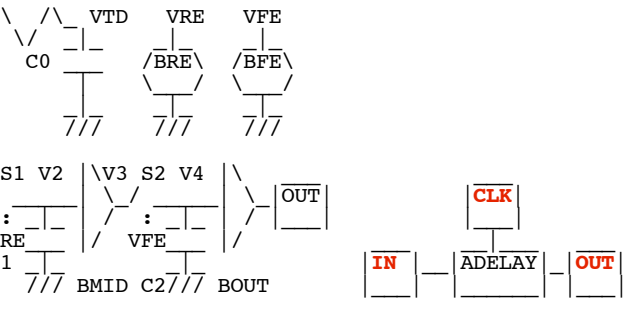
*==========Analog_Delay_Line==========

Perhaps the simplest way to use analog delay lines is to build an element that has an input, an output, and runs off of a square wave clock. A purely digital version of an analog delay line would be a multi-bit shift register. The software version might use an array of memory byte locations. The switch capacitor element is more of an analog version.

*=========Analog_Delay_Subcircuit=========

```
.SUBCKT   ADelay IN     OUT    CLK
 R0       CLK    VTD    100k
 C0       VTD    0      1p
 BRE      VRE    0      V = 5*u(V(CLK) -V(VTD)-.1)
 BFE      VFE    0      V = 5*u(V(VTD) -V(CLK)-.1)
*SXXXXXX  N+     N-     NC+    NC-    MODEL
 S1       V1     V2     VRE    0      SWP
 S2       V3     V4     VFE    0      SWP
 C1       V2     0      30n
 C2       V4     0      30n
 BIN      V1     0      V =    V(IN)
 BMID     V3     0      V =    V(V2)
 BOUT     OUT    0      V =    V(V4)
.ENDS     ADelay
```



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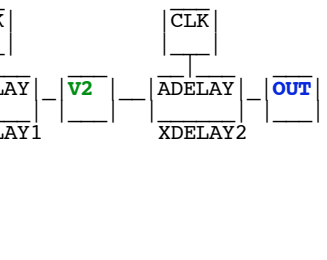
Connecting a number of such elements in series simulates shift registers in the analog world.

*=========Analog_Delay========



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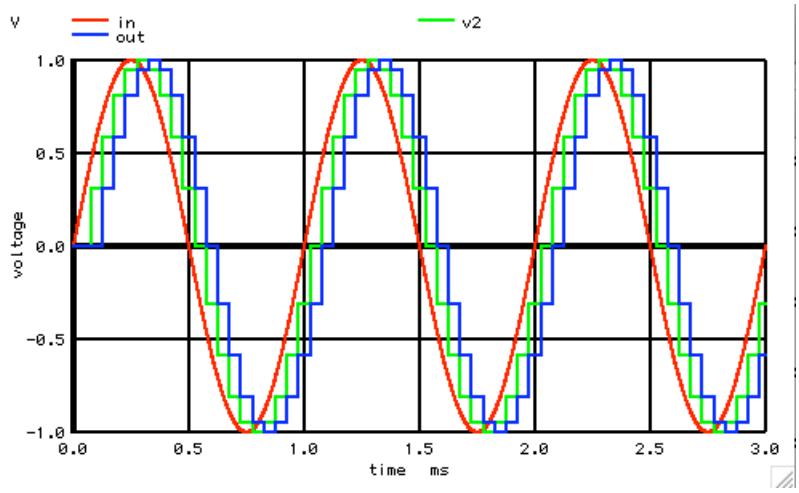
Being able to do discreet time delays of signal is a requirement for doing digital filtering.



==========Full_Netlist_For_Copy_Paste==========

```
Analog_Delay
*
*                  |CLK|            |CLK|
*                  |___|            |___|
*                    |                |
*      ___|IN |__|ADELAY|_|V2 |__|ADELAY|_|OUT|
*    _|_          XDELAY1          XDELAY2
*   /   \
*  //\   \
*  \    \//
*   \___/
*    |
*    ///
*
*V_SIN#   NODE_P NODE_N DC     VALUE  SIN(   V_DC   AC_MAG FREQ   DELAY  FDamp)
VIN       IN     0      DC     0      SIN(   0      1      1k                )
*V_PULSE# NODE_P NODE_N DC     VALUE  PULSE( VINIT  VPULSE TDELAY TRISE  TFALL  PWIDTH PERIOD )
VCLK      CLK    0      DC     0      PULSE( 0      5      1n     1n     1n     25u    50u    )
XDELAY1   IN     V2     CLK    ADelay
XDELAY2   V2     OUT    CLK    ADelay
.MODEL    SWP    SW(    VT=2.6 VH=.2  RON=1  ROFF=10MEG)
.control
*TRAN     TSTEP  TSTOP  TSTART TMAX
 tran     1u     3m     0      1u
 set      pensize = 2
 plot     in     v2     out
.endc
*=========Analog_Delay_Subcircuit=========================
.SUBCKT   ADelay IN     OUT    CLK
 R0       CLK    VTD    100k
 C0       VTD    0      1p
 BRE      VRE    0      V = 5*u(V(CLK) -V(VTD)-.1)
 BFE      VFE    0      V = 5*u(V(VTD) -V(CLK)-.1)
*SXXXXXX  N+     N-     NC+    NC-    MODEL
 S1       V1     V2     VRE    0      SWP
 S2       V3     V4     VFE    0      SWP
 C1       V2     0      30n
 C2       V4     0      30n
 BIN      V1     0      V =    V(IN)
 BMID     V3     0      V =    V(V2)
 BOUT     OUT    0      V =    V(V4)
.ENDS     ADelay
*
* |CLK|_/\  /\  /\_ VTD   VRE   VFE
* |___|   \/  \/  _|_    _|_   _|_
*              C0 ___   /BRE\  /BFE\
*       R0        |     \___/  \___/
*                 |      |     |
*                ///    ///   ///
*
*      |\V1 S1 V2 |\V3 S2 V4 |\
* |IN |_| \_/ ____| \_/ ____| \_|OUT|          |CLK|
* |___|   /  :  _|_ /  :  _|_ /   |___|          |___|
*        /  VRE___ /  VFE___ /                    |
*           C1 _|_    _|_                 |IN |__|ADELAY|_|OUT|
*      BIN     /// BMID C2/// BOUT        |___|  |_______| |___|
*
*==========================================
```

```
.end

4.11.10_4.54PM
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```