



```

.model          nchannel          NMOS
+ Level= 8      Tnom=27.0
*-----Process-----
+ tox=160e-10  xj=0.25e-06      nch=0.5e+17
*-----V_threshold-----
+ vth0=0.72    nlx=0.12e-06
*-----Bulk-----
+ k1=1.04      k2=-1.209E-01
+ cdsc=-2.4E-4  cdsd=-1.506E-04  cdsb=-2.219E-04
*-----mobility-----
+ u0=678      ua=8.964e-10
+ ub=1.472e-18  uc=-4.441E-17    vsat=86000
*-----Subthreshold-----
+ nfactor=1.8
+ cit=-5.0E-04  voff=-7.862E-02
+ eta0=4.441e-16  etab=-2.E-01    dsub=0.7
*-----Hot electrons-----
+ alpha0=1.61e-05  beta0=36.68
*-----VAF-----
+ lint=.12e-06  pclm=.19        psobel=3.79e+08  psobe2=9.4e-05
+ delta=0.01655  pvag=0.4484
*-----Bulk_diode-----
+ js=5.858e-08
*-----Resistance-----
+ rsh=70      rdsw=375
+ wr=0.7586   prwb=0          prwg=-4.441E-17
*-----Capacitance-----
+ cj=0.0002424  cjsw=2.73e-10   mj=0.3551        mjsw=0.3873
+ cgso=9e-13   cgdo=9e-13      cgbo=7e-10
+ pb=0.5614    pbsw=0.8        xpart=0
+ dlc=5e-08    dwc=1.5e-07
*-----BulkChargeEffect-----
+ a0=0.7      a1=0            a2=1             ags=0.05583
+ b0=6.305e-08  b1=6.579e-08   keta=-1.531E-02
*-----ShortChannel-----
+ dvt0=2.2     dvt1=0.53       dvt2=-1.521E-01  drout=0.76
+ pdiblc1cb=.4  pdiblc1=0.00886  pdiblc2=0.00029
*-----NarrowChannel-----
+ w0=2.6e-04   wint=0.16e-06
+ ww=-9.525E-14  wwn=1.0
+ dvt0w=0      dvt1w=5.3e6     dvt2w=-1.E-01
+ k3=2.53      k3b=-5          dwg=0            dwb=0
*-----Noise-----
+ af=1         kf=1e-28        ef=0.95
*-----Temperature-----
+ pvsat=0      ute=-1.258E+00  kt1=-3.85E-01
+ kt1l=0       kt2=-3.098E-02  ual=5.705e-09
+ ub1=-1.147E-17  uc1=-1.302E-01  at=20380
* prt=-3.287E+02  lk1=0           lk2=0
+ lvsat=0      la0=0           lags=0           lute=0
+ luc=0

```

```
.control
set pensize = 2
tran      1u    .2m    0    10n
plot      v(clk1)  v(clk2)
plot      v(in1)   xlimit 99u 104u ylimit -1m 1m
```

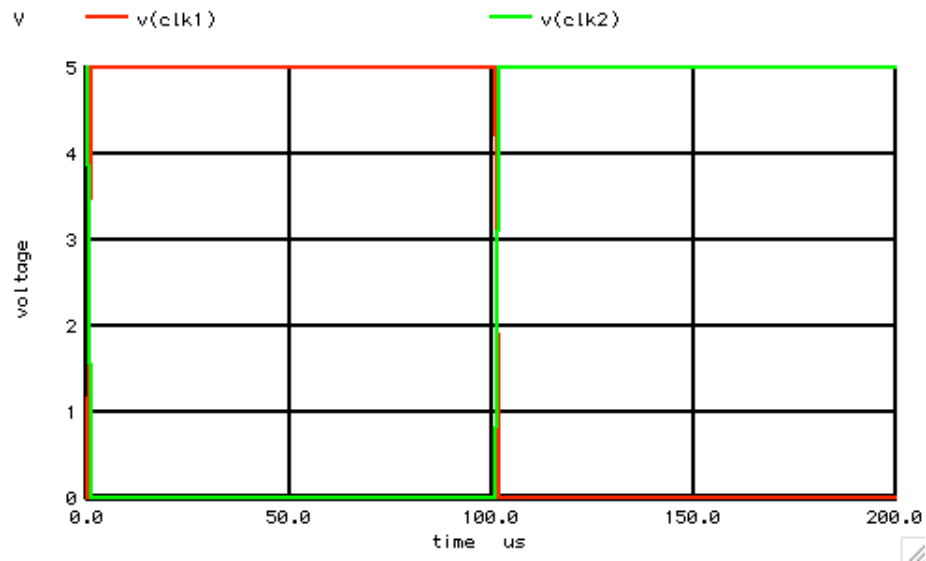
.endc

.end

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At the time that the LMC2001 was being designed, CMOS models that followed charge conservation were just being installed at National Semiconductor. Since then a lot of papers and a lot of model development has gone into reducing feedthru in a CMOS switch.



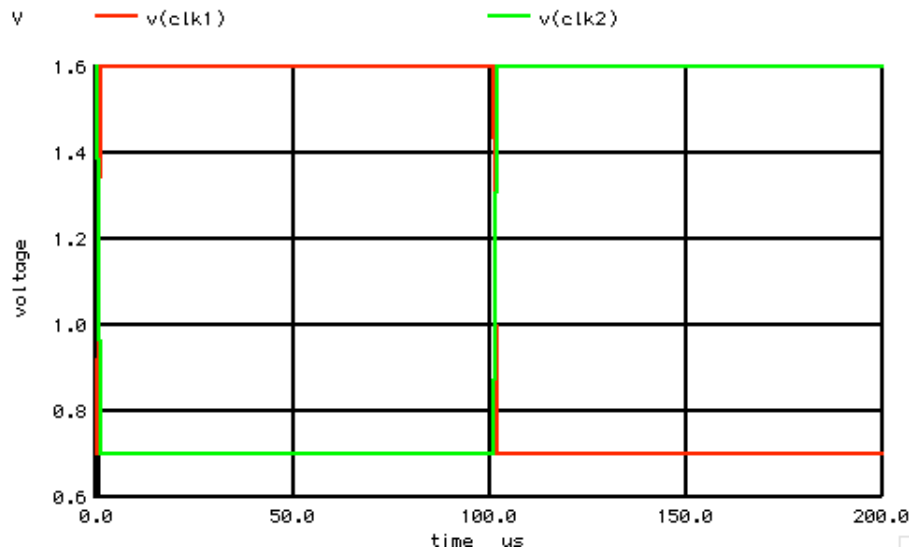
There looks like there should be a balancing act going on. Whenever something get turned on,



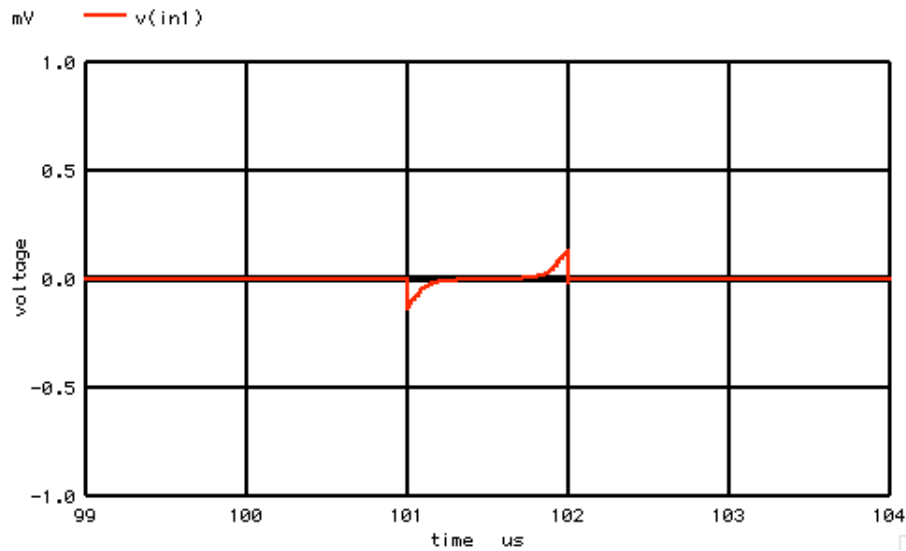


something new. The input chopper doesn't have to be a chopper with switches that turn completely off. If the gate voltages were adjusted such that the CMOS switches shifted between a 1k Ohm ON Resistance to a 1Meg Ohm ON Resistance, the "chopper" would still work just fine. If the full Op Amp has an effective input offset of a few micro volts, then a few pico amps will flow as dc current across the inputs.

Switches go thru the ultimate in non linear operation. They go from On to completely off. Simulates suggest that is is possible. But only silicon can be trusted.



The experiment only involve changing what kind of voltage are applied as the gates,



The results are plotted to the same 1mV scale.  
Again, silicon needs to be built to trust  
this apparent improvement.

If it were possible to reduce chopper noise current  
spikes at the input, would that buy further applications  
for amplifiers like the LMC2001? Could the ability  
to reduce chopper noise at the inputs open up some new  
opportunities?