RRIO_requirements

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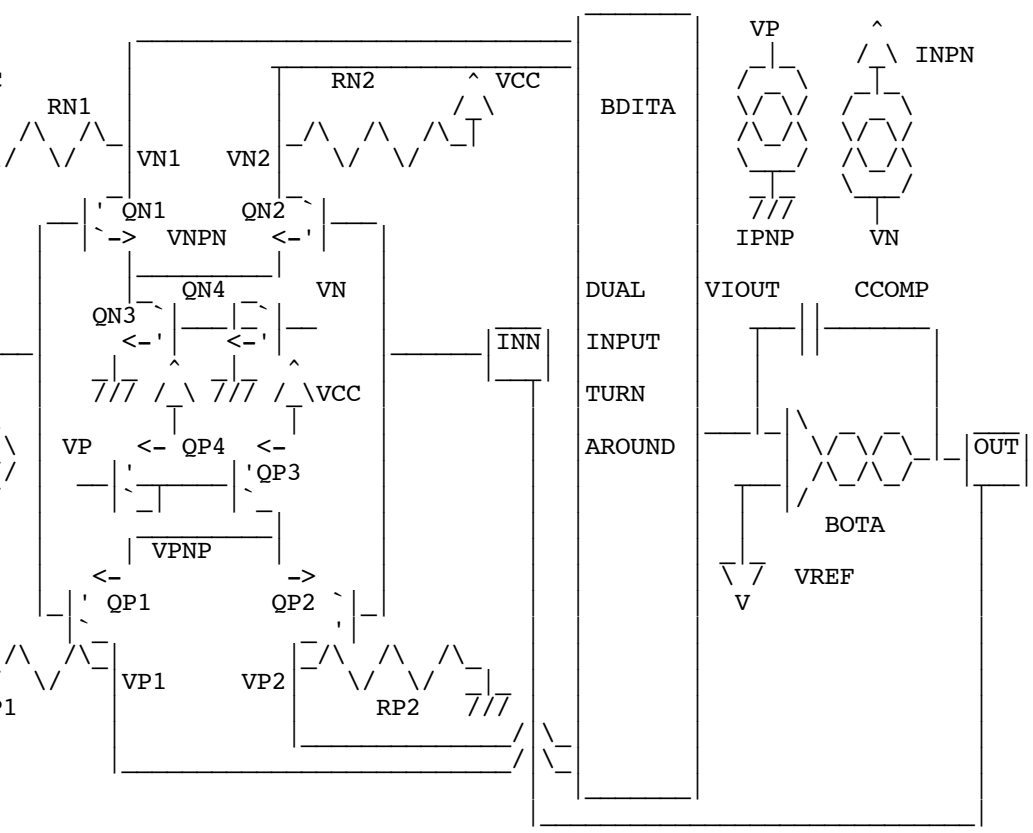
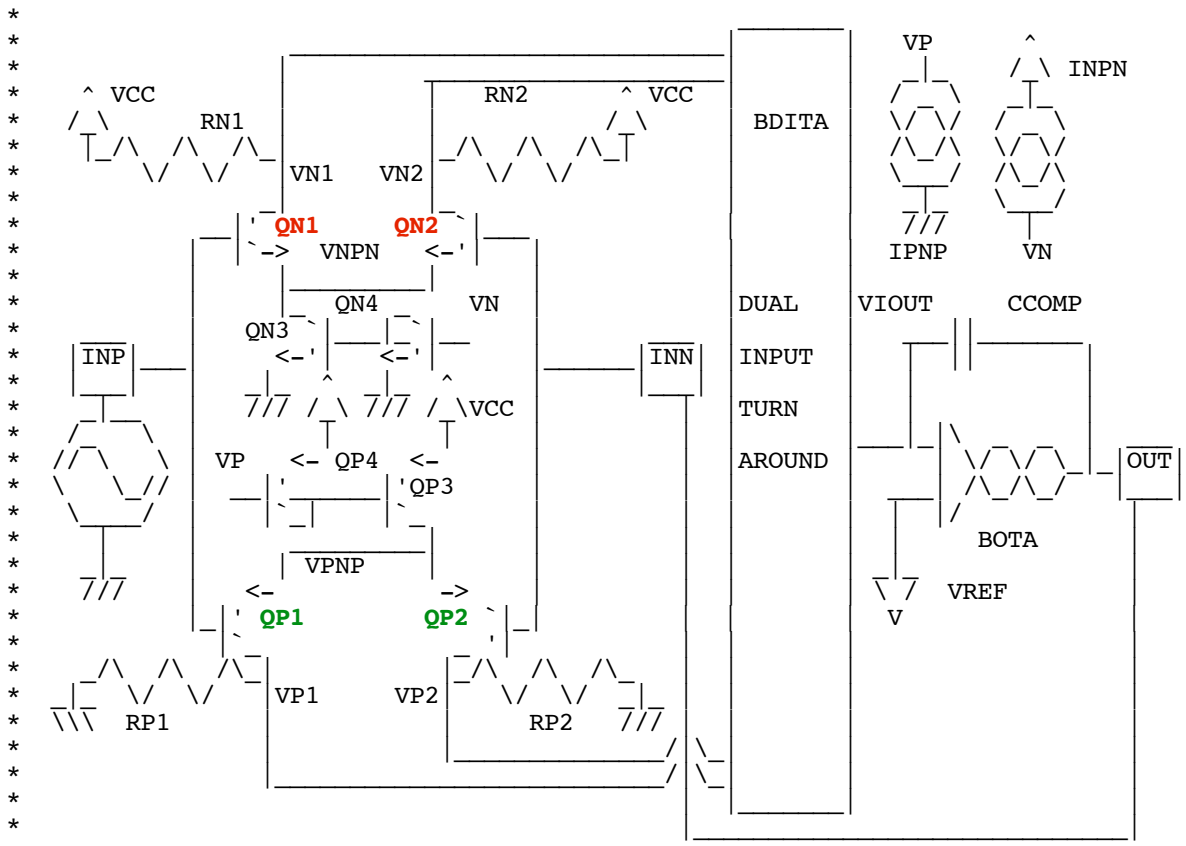



```
.OPTIONS  method=gear  GMIN=1e-18

VIN       INP     0       SIN(6   6       1K )
QP1       VP1     INP     VPNP    PNPL    1.04
QP2       VP2     OUT     VPNP    PNPL    1
QP3       VPNP    VP      VCC     PNPL    1
QP4       VP      VP      VCC     PNPL    1
RP1       VP1     0        5K
RP2       VP2     0        5K

QN1       VN1    INP      VNPN    NPNV    1.02
QN2       VN2    OUT      VNPN    NPNV    1
QN3       VNPN   VN       0       NPNV    1
QN4       VN     VN       0       NPNV    1
```

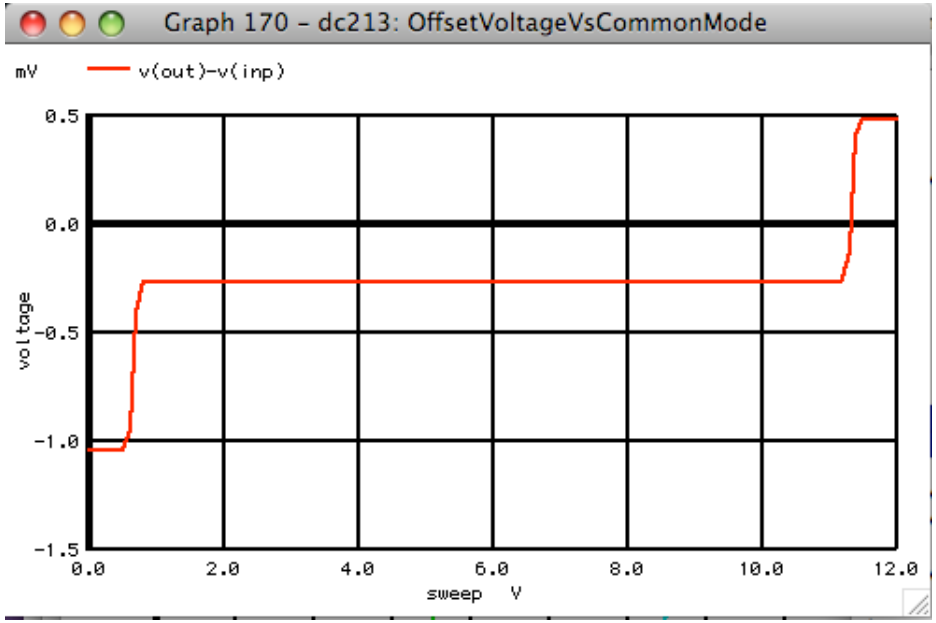
```
RN1       VCC   VN1     5K
RN2       VCC   VN2     5K
IBIAS     VIOUT 0       -.01u

VCC       VCC    0      12
VREF      VREF   0      6
IPNP      VP     0      20u
INPN      VCC    VN     20u

BDITA     VIOUT  0     I = ( V(VP2) - V(VP1) + V(VN2) - V(VN1)  )/5000
BOTA      OUT    0     I = -1*( V(VIOUT) - V(VREF) )/5000
CCOMP     OUT    VIOUT 3p

.tran     1u     2m     0      1u

.model      NPNV npn BF=150
.model      PNPL pnp BF=150

.control
run
set        pensize = 2
*plot       v(out) v(inp)
dc         vin  0    12     100m
plot       v(out)-v(inp) title  OffsetVoltageVsCommonMode
plot       v(vp1)   v(vp2)  v(vcc)-v(vn1)  v(vcc)-v(vn2) title  TailCurrentsVsCommonMode
alter      vcc   dc = 1
dc         vin  0    1     1m
plot       v(out)-v(inp)  title  OffsetVoltageVsCommonMode
plot       v(vp1)   v(vp2)  v(vcc)-v(vn1)  v(vcc)-v(vn2) title  TailCurrentsVsCommonMode

.endc
.end
```

*** ====================END==================================**

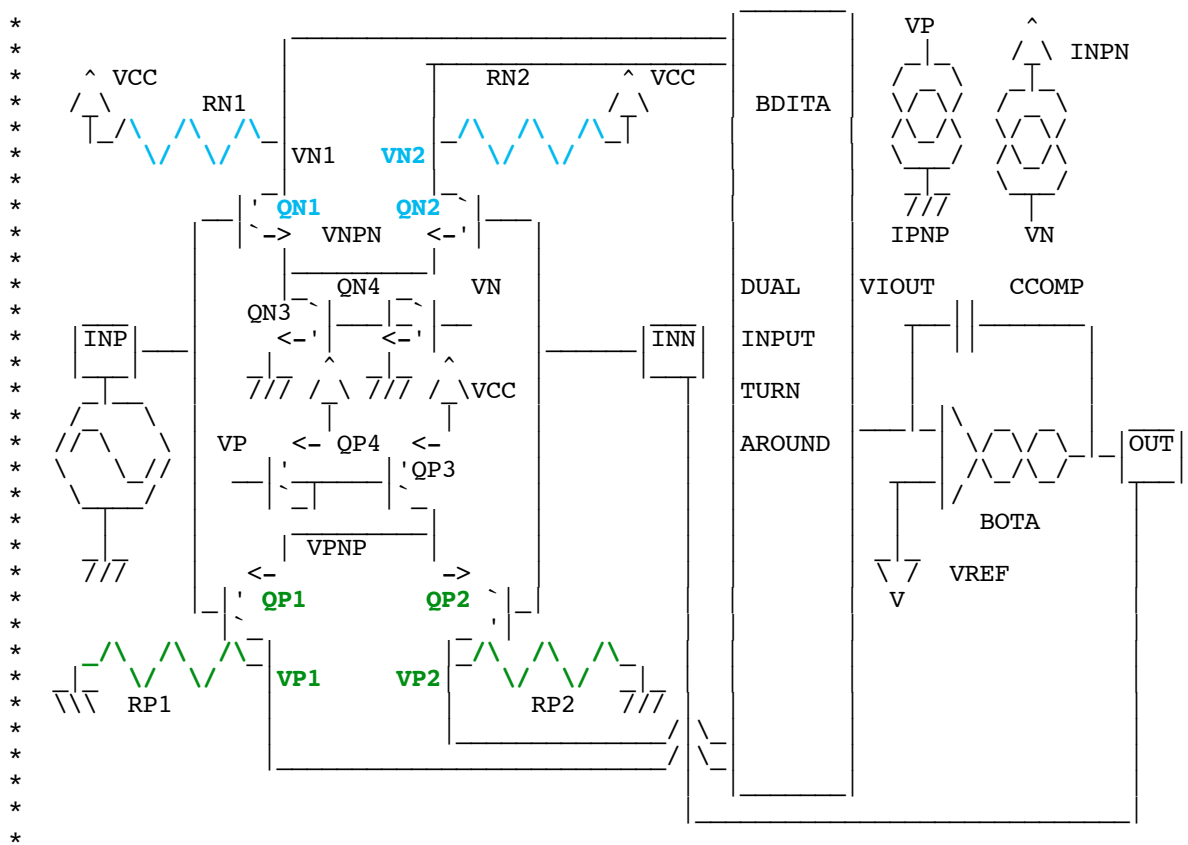
As time went on the supply voltage levels kept dropping which encouraged the development of Rail to Rail input and output Op Amps to be able to use all of the supply voltage range.

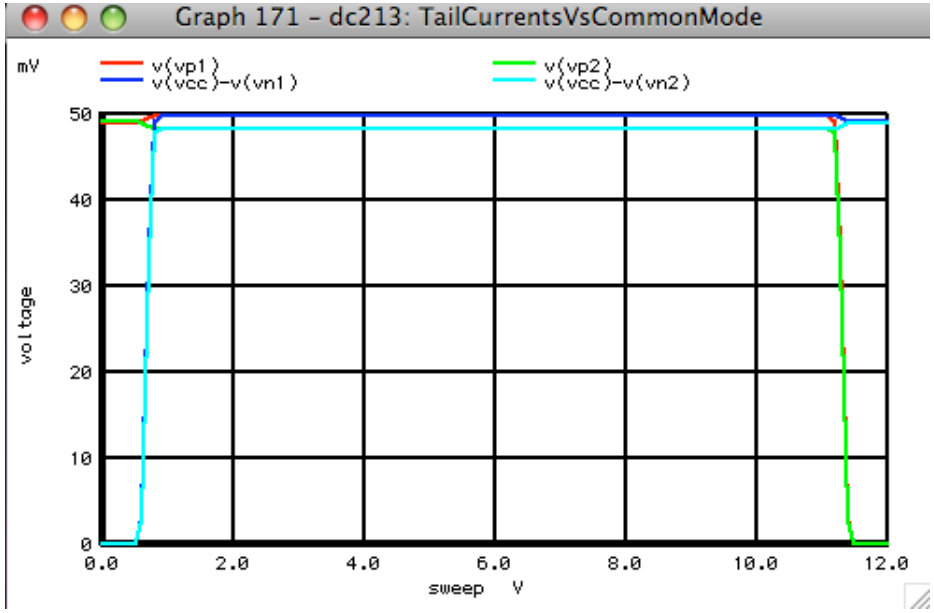


For the case of Bipolar transistors, this meant that two input stages need to be connected in parallel. Just doing so means most of the time both input stages are on and depending on which rail the inputs approach, one of the input stages will turn off.



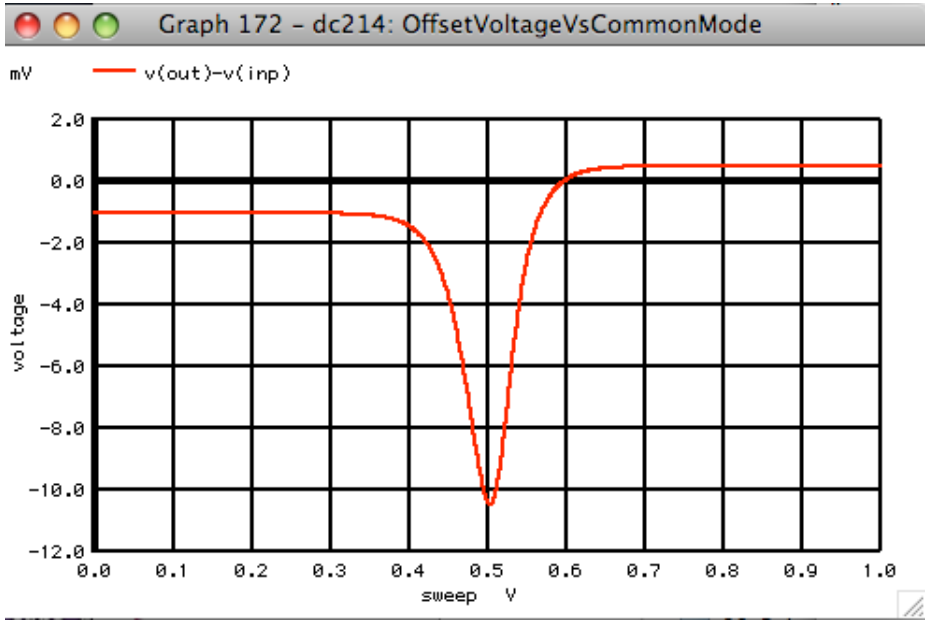
In this simulation, a 1mV mismatch was introduced to the input pnps and a +.5mV mismatch was introduced to the npns. So for most of the common mode input range, there is a partial offset cancelation. At zero volts the npns are off and the pnp's offset dominates. At 12Volts the npn's dominate.


VCC
RN1
RN2
VCC
VN1
VN2
QN1
QN2
VNPN
QN4
VN
QN3
INP
INN
VP
QP4
QP3
VPNP
QP1
QP2
VP1
VP2
RP1
RP2
BDITA
DUAL
INPUT
TURN
AROUND
VP
INPN
IPNP
VN
VIOUT
CCOMP
OUT
BOTA
VREF

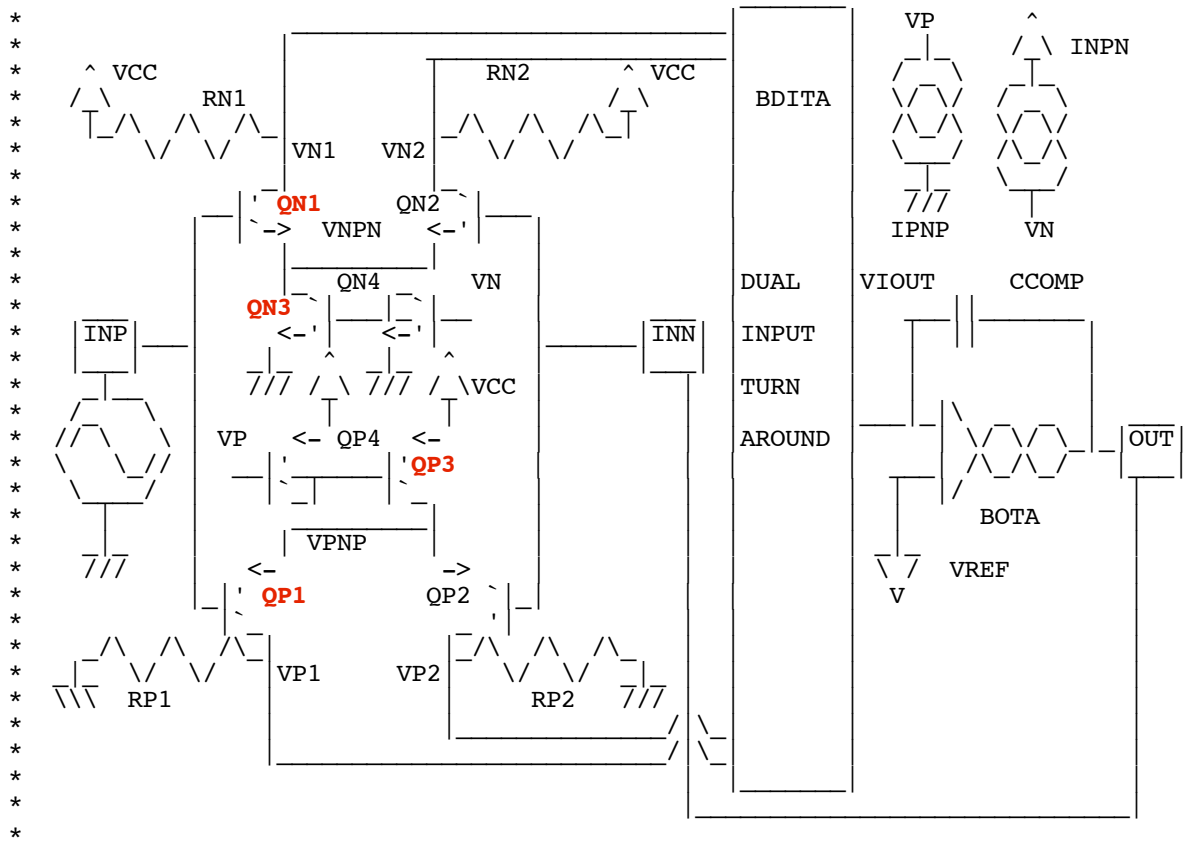


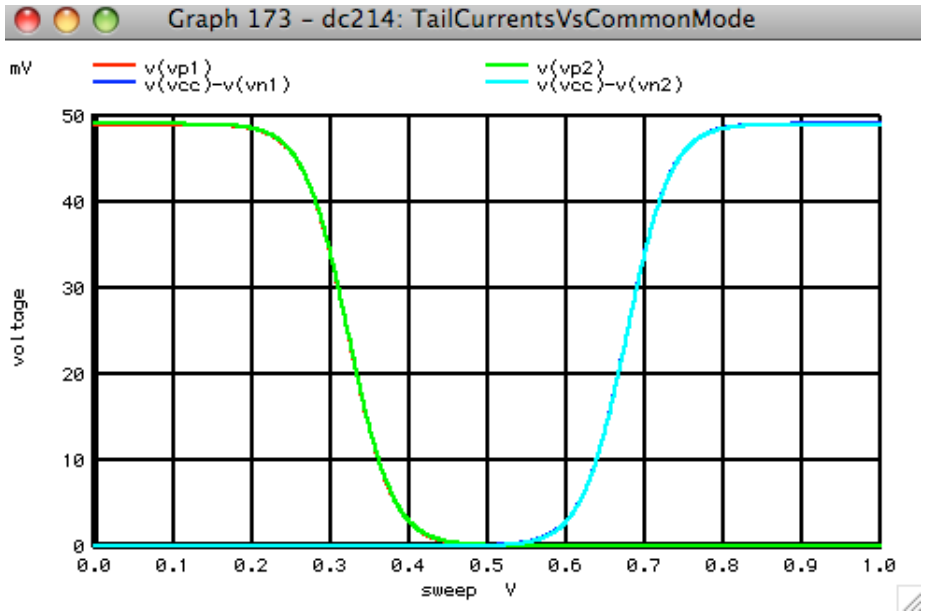
Another place to view things is the IR drop at the collector resistors for input transistors. If the resistors are small enough, the inputs can easily swing 200mV past both rails. This nodes later get fed into a dual input turn around circuit which converts the differential input signal from either input into a output current.

The rail to rail feature sort of assumes that the the supply voltage is high enough so that either input stage is on.



On a 1volt supply, both pnp and npns are off at 500mV. Above and below this level will turn on one stage.


VCC
RN1
RN2
VCC
VN1
VN2
QN1
QN2
VNPN
QN4
VN
QN3
INP
INN
VP
QP4
QP3
VPNP
QP1
QP2
VP1
VP2
RP1
RP2
VCC
BDITA
DUAL
INPUT
TURN
AROUND
VP
INPN
IPNP
VN
VIOUT
CCOMP
OUT
BOTA
VREF
V



For a bipolar Rail To Rail Op Amp, this implies that there is a minimum supply voltage of two diodes and to sats in order that neither input stage is turned off.