RRIO_Clamp_requirements

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* dsauersanjose@aol.com  12/17/08
* www.idea2ic.com
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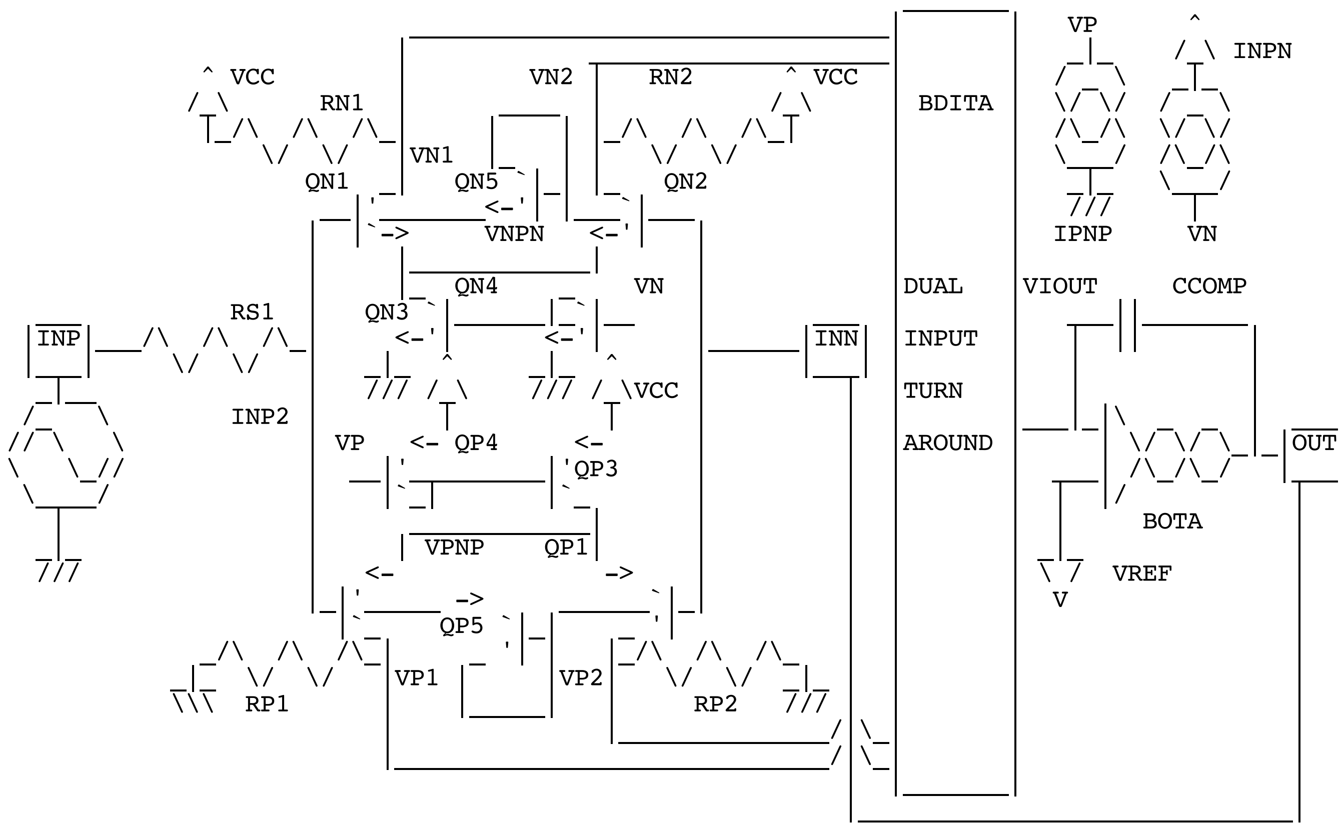


```
.OPTIONS  method=trap

VIN       INP     0       PULSE( 1 9 1n 1n 1n 10u 20u )
RS1       INP     INP2    7000
QP5       OUT     OUT     INP2    PNPV    1
QN5       OUT     OUT     INP2    NPNV    1

QP1       VP1     INP2     VPNP    PNPV    1
QP2       VP2     OUT     VPNP     PNPV    1
QP3       VPNP    VP      VCC      PNPV    1
QP4       VP      VP      VCC      PNPV    1
RP1       VP1     0        5K
RP2       VP2     0        5K

QN1       VN1    INP2     VNPN     NPNV    1
QN2       VN2    OUT      VNPN     NPNV    1
```

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QN3       VNPN  VN     0      NPNV   1
QN4       VN    VN     0      NPNV   1
RN1       VCC   VN1    5K
RN2       VCC   VN2    5K

VCC       VCC    0     12
VREF      VREF   0     6
IPNP      VP     0     20u
INPN      VCC    VN    20u

BDITA     VIOUT  0     I = ( V(VP2) - V(VP1) + V(VN2) - V(VN1)  )/5000
BOTA      OUT    0     I = -1*( V(VIOUT) - V(VREF) )/50
CCOMP     OUT    VIOUT 20p

.tran     100n   50u    0      100n

.model    NPNV npn BF=150
.model    PNPV pnp BF=150

.control
run
set        pensize = 2
plot       v(out) v(inp)
.endc
.end
```

```
* ====================END==================================
```

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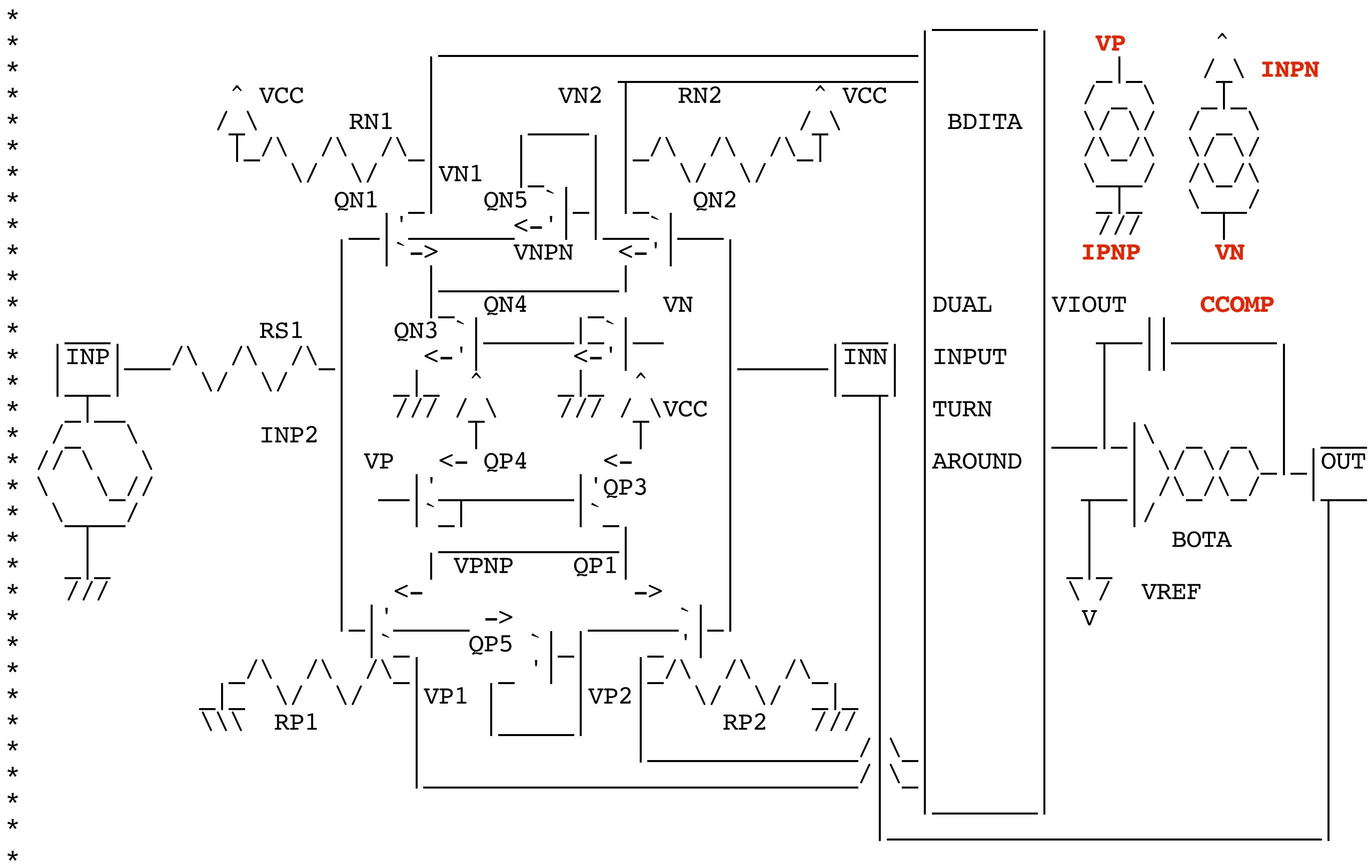
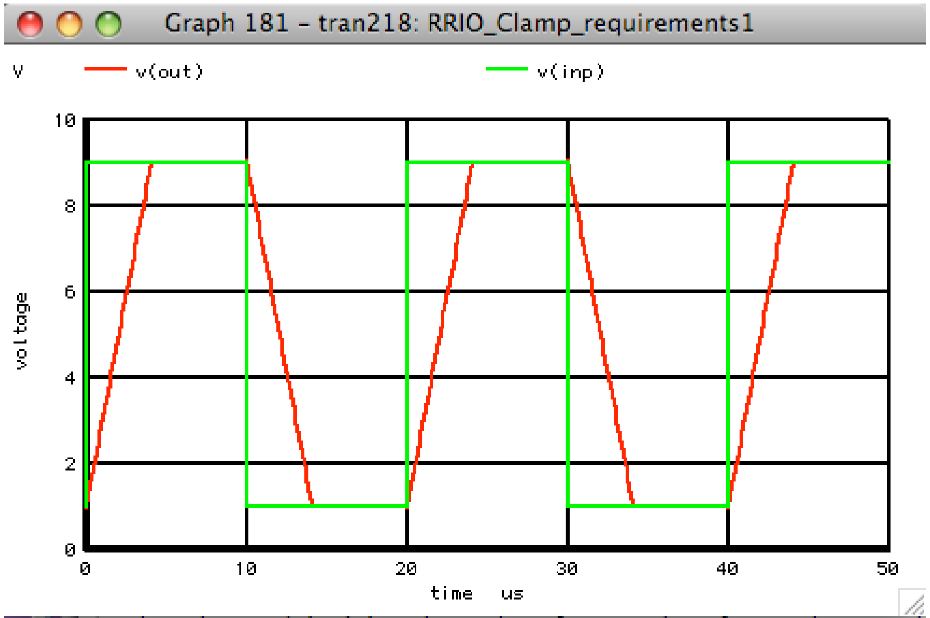
The development of vertical pnps was a natural for RRIO Op Amp Design. The vertical pnps are about a thousand times faster and have at least ten times better beta than lateral pnps.



For the LM6142, the tail currents IPNP of the input stages was chosen by weighing an input bias current spec against a process beta spec. That chosen, the desired GainBandWidth for the Op Amp defines the magnitude of the compensation capacitor CCOMP used. This in turn

defines the slew of the Op amp which is simply +/- full tail current into the compensation capacitor CCOMP.

Connecting the Op Amp up as a simple voltage follower demonstrates why the input clamp diodes are needed. Both vertical npns and pnps will be destroyed with reverse emitter base voltages above a few volts. Just supplying a square wave to a voltage follower application will do that because the output of the Op Amp may not be able to slew as fast as the input signal.



In the case of this simulation, current limiting resistor RS1 and clamp diodes QN5 and QP5 keep the voltages across the input transistors to within reason during the slewing period.