OUTPUT_REQUIREMENTS

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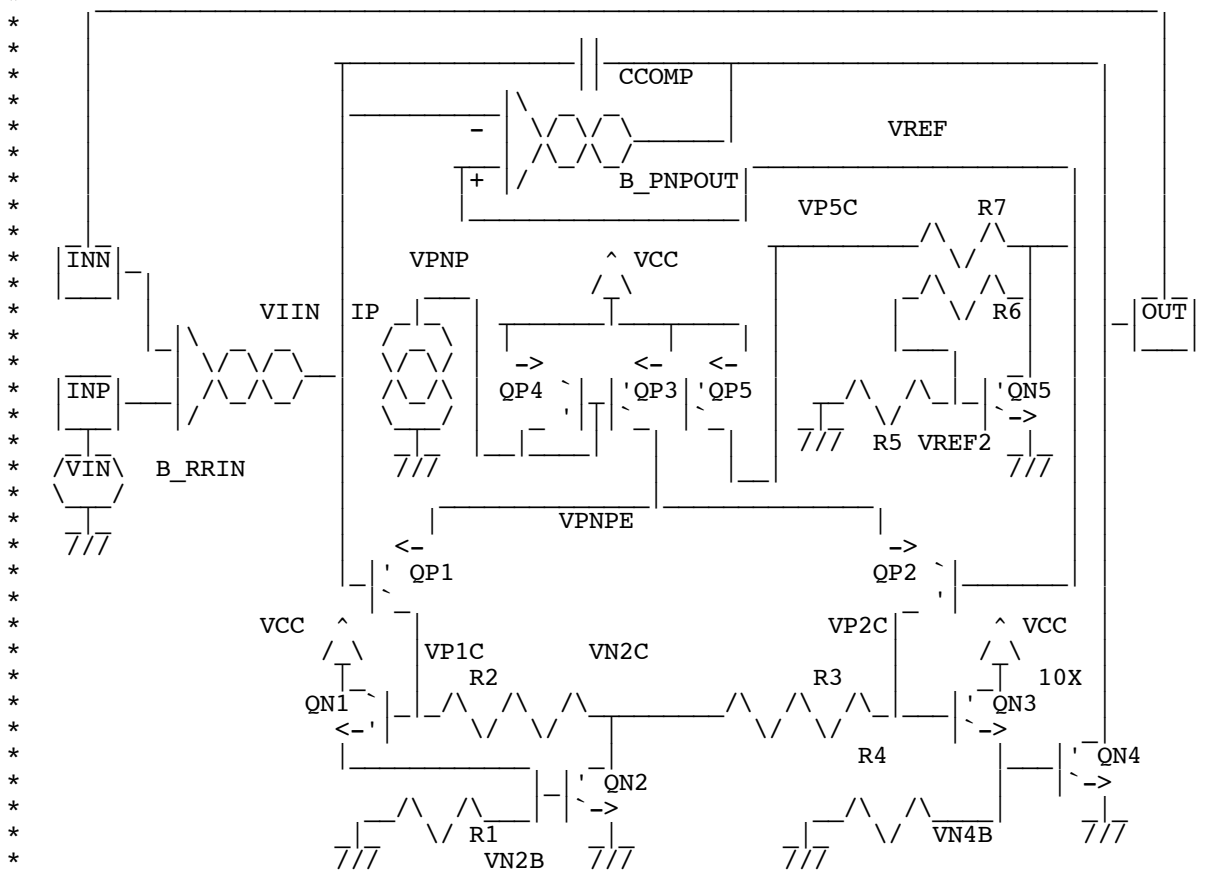
* www.idea2ic.com

* US Patent # 5546045

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.OPTIONS  method=gear  GMIN=1e-18

VIN       INP    0      SIN(6   3      1K )

VCC       VCC    0      12
IP        VPNP   0      40u

B_RRIN    VIIN   0       I = ( V(INP) - V(OUT) )/5000
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```
QP1       VP1C   VIIN   VPNPE   PNPV   1
QP2       VP2C   VREF   VPNPE   PNPV   1
QP3       VPNPE  VPNP   VCC     PNPV   1
QP4       VPNP   VPNP   VCC     PNPV   1
QP5       VP5C   VPNP   VCC     PNPV   4

QN1       VCC    VP1C   VN2B    NPNV   1
QN2       VN2C   VN2B   0       NPNV   1
QN3       VCC    VP2C   VN4B    NPNV   1
QN4       OUT    VN4B   0       NPNV   10

QN5       VREF   VREF2  0    NPNV   1
R5        VREF2  0      6K
R6        VREF   VREF2  12K
R7        VP5C   VREF   18K

R1       VN2B    0      20K
R2       VP1C    VN2C   5K
R3       VP2C    VN2C   5K
R4       VN4B    0      10K

CCOMP     OUT    VIIN    10p
BOTA      OUT    0       I = -200u


.tran     1u     2m     0      1u

.model      NPNV  npn BF=150
.model      PNPV pnp BF=60

.control
run
set pensize = 2
plot v(inp)  v(out)

dc        vCC  1    12    100m
plot      v(vref)  v(vp5c)
.endc
.end
```

* ==========END==========

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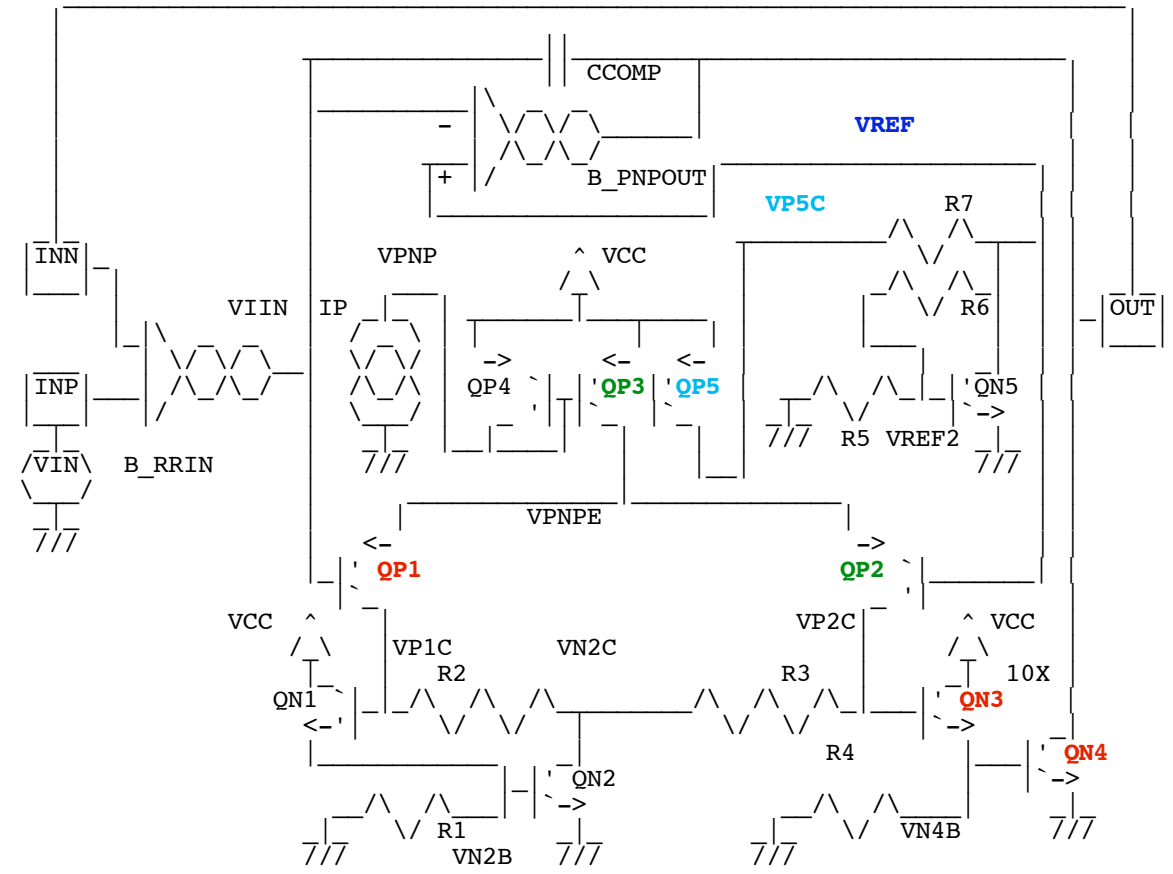
The output stage introduces a number of requirements. First off, the actual outputs are collectors of transistor. Then there is a need to have a lot of input to output current gain. Then there is this need to work down to the same voltage requirements as the input stage. That is to work down to a supply voltage of 2 diodes and two sats. Then there is the low supply current requirement. Then there is high bandwidth requirement. Then there is the unity gain stability with a 200pF cap load requirement.



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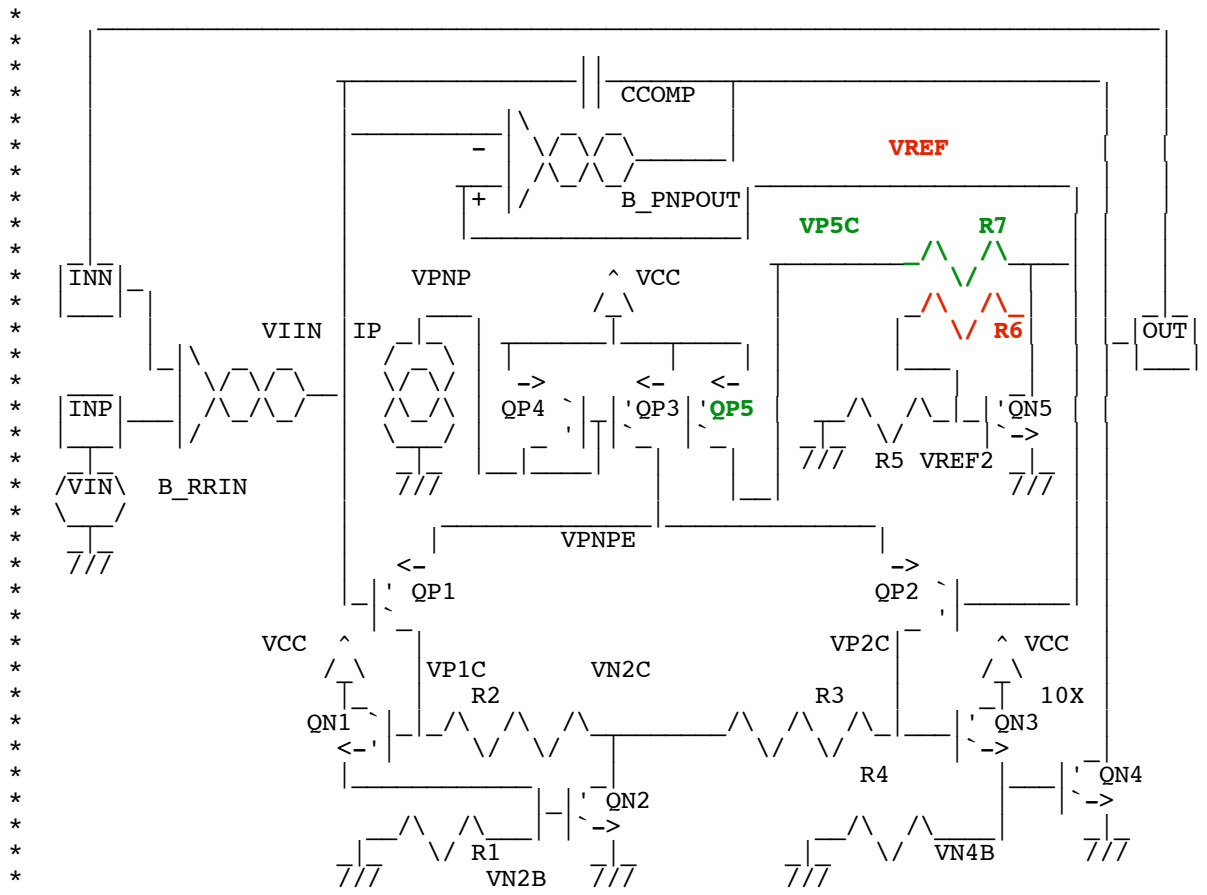
The bottom NPN half of the output stage is shown above. The top PNP half is an exact mirror image of the NPN half and is represented by B_PNPOUT. The current gain supplied by QN4, QN3, and QP1. If VREF is at half supply, then QP3, QP2, QN3 and QN4 can work down to two diodes and two sats.

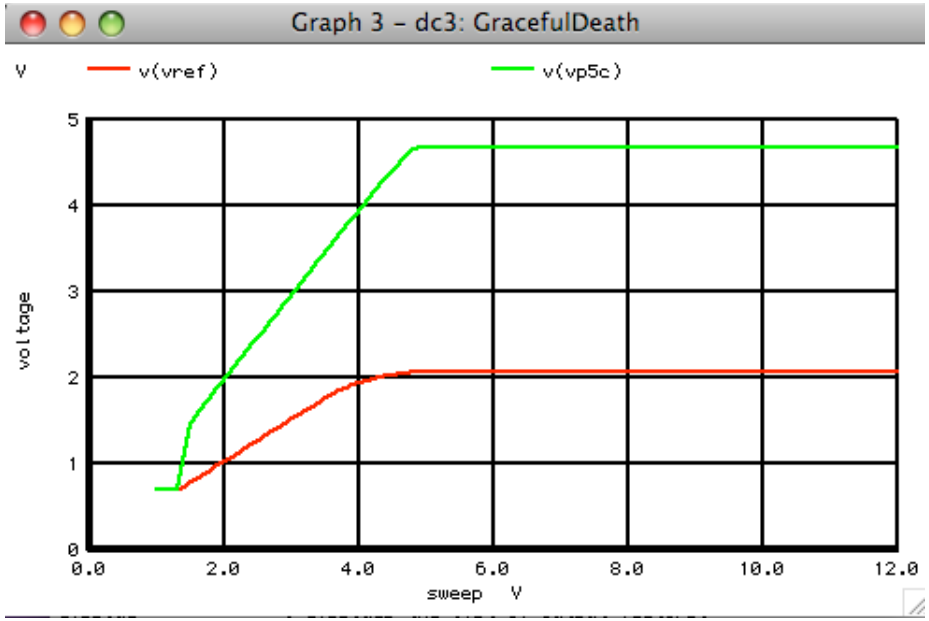
For supply rejection reasons, it is not desirable that VREF should be modulated by VCC. The circuit above shows a simplified version used in the LM6142.

There is an unwritten spec that an Op Amp should have a "graceful death" when the supply voltage is lowered. Ideally what this means is the the Op Amps should still function but progressively degrade in performance as the supply voltage is lowered. Having an Op Amp go crazy at low voltages does not go unfixed.

The LM6142 was originally designed for the 5V and 12V market. Below 5 volts, it was OK to start graceful death at the output stage. While the circuit below is not exact, it shows the details under consideration.



Above 5 volts a current source biases up a diode multiplier to provide at stable VREF. The plot of VP5C and Vref versus VCC shown below somewhat resembles the LM6142. Transistor QP5 is set up to saturate such that a 2.4V supply voltage generates a VREF which is at 1.2V.



This feature worked so well that it was found that the part was solid at both 2.4Volts and 24volts. So the data sheet specs were extended to those supply specs as well.