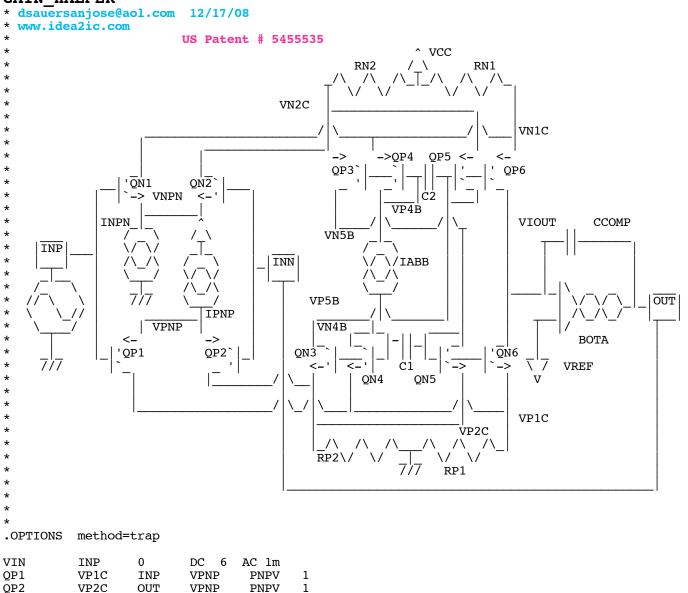
GAIN HALFER



QPZ	VPZC	001	VPNP	PNPV	1
RP1	VP1C	0	5K		
RP2	VP2C	0	5K		
QN1	VN1C	INP	VNPN	NPNV	1
QN2	VN2C	OUT	VNPN	NPNV	1
RN1	VCC	VN1C	5K		
RN2	VCC	VN2C	5K		

To Covert PDF to plain text click below

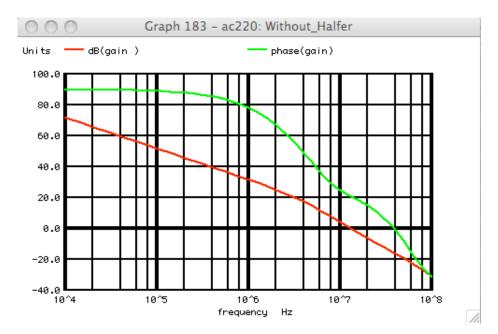
```
VCC
          VCC
                 0
                        12
VREF
          VREF
                 0
                        6
          VCC
                 VPNP
                        20u
IPNP
                        20n
INPN
          VNPN
                 0
QP3
          VN5B
                 VP4B2
                         VN2C
                                  PNPV
                                        1
RP3
          VP4B2
                 VP4B
                         1000
QP4
          VP4B
                 VP4B
                         VN1C
                                  PNPV
                                         1
QP5
          VP5B
                 VP5B
                         VN2C
                                  PNPV
                                         1
RP5
          VP5B2 VP5B
                         1000
QP6
          VIOUT VP5B2
                          VN1C
                                  PNPV
                                         1
QN3
          VP5B VN4B2
                         VP2C
                                  NPNV
                                         1
RN3
          VN4B2 VN4B
                         1000
QN4
          VN4B VN4B
                         VP1C
                                  NPNV
                                         1
QN5
          VN5B VN5B
                         VP2C
                                  NPNV
                                         1
RN5
          VN5B2 VN5B
                         1000
QN6
          VIOUT VN5B2
                          VP1C
                                 NPNV
                                        1
IABB
          VP4B
                 VN4B
                         5u
BOTA
          OUT
                 0
                         I = -1*(V(VIOUT) - V(VREF))/1
CCOMP
          OUT
                 VIOUT
                         1p
                  VP5B2
C2
          VP4B2
                          3f
C1
          VN4B2
                  VN5B2
                          3f
.model
          NPNV
                 npn
                          BF=150 CJE=.6p CJC=.3p CJS=1p
.model
          PNPV
                 pnp
                          BF=60
                                  CJE=.6p CJC=.3p CJS=1p
.control
run
              10
                      10k
                               100000K
ac
          dec
set
          pensize = 2
let
          gain = v(out)/(v(out) - v(inp))
plot
          dB(gain ) phase(gain) title Without_Halfer
alter
          C1 capacitance = 3p
alter
          C2 capacitance = 3p
              10
ac
          dec
                      10k
                               100000K
          pensize = 2
set
let
          gain = v(out)/(v(out) - v(inp))
plot
          dB(gain ) phase(gain) title With Halfer
.endc
.end
```

http://www.fileformat.info/convert/doc/pdf2txt.htm

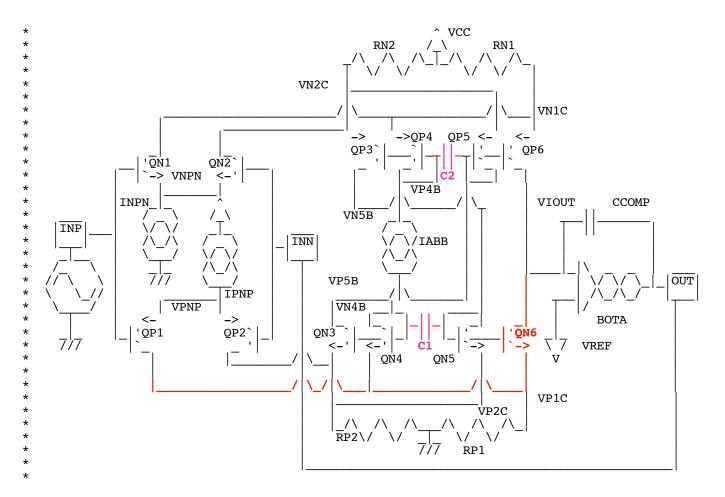
The LM6142 is a current starved design. The idea was to design a 10MHz unity gain stable Op Amp which drew less than 1mA per amplifier using a process very close to the standard analog process.

The main challenge was the size of transistors. The process was a 30volt process. The dimensions were such that stray capacitance was in terms of pico farads instead of femto farads.

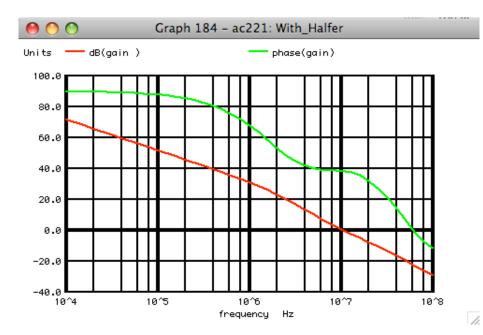
Perhaps the dominate challenge was the emitter base stray capacitance which was around 0.5pF. A transistor will have a junction impedance of 26Kohm at 1uA of emitter current. That puts ftau at 10MHz. The problem is that a large number of such transistors running minimum current need to be put into the signal path. Each transistor contributes time delay to the signal and the goal is to have the total overall time delay small enough that there is less that 180 of phase shift at 10MHz in order for the Op Amp to be unity gain stable.



The simulation above is looking at the phase shift due to the dual input turn around just modeling stray capacitance. The unity gain cross is around 15Mhz. At that frequency there may be a little more than 20degrees of phase margin.



The input transistors are already driving the dual input turn around in a common base mode configuration anyway. This is a faster way to drive transistors. Adding capacitor C1 will lower the impedance at the base of QN6 and adding C2 as well effectively kills the high frequency signal path of all other transistors except QN6. High frequency signal has only one path and that is to common base drive QN6 to the output.



The result is a bit counter intuitive looking at the resulting gain phase plot. Both gain and phase delay are reduced at higher frequencies. For a normal lowpass, a gain decrease normally results in a phase delay increase. What is happening in the circuit is half of the dual turn around's signal path which has the most transistors and therefore the most delay has been removed at the higher frequencies. This is the "shorten the signal path" technique.