BETA_BALANCE

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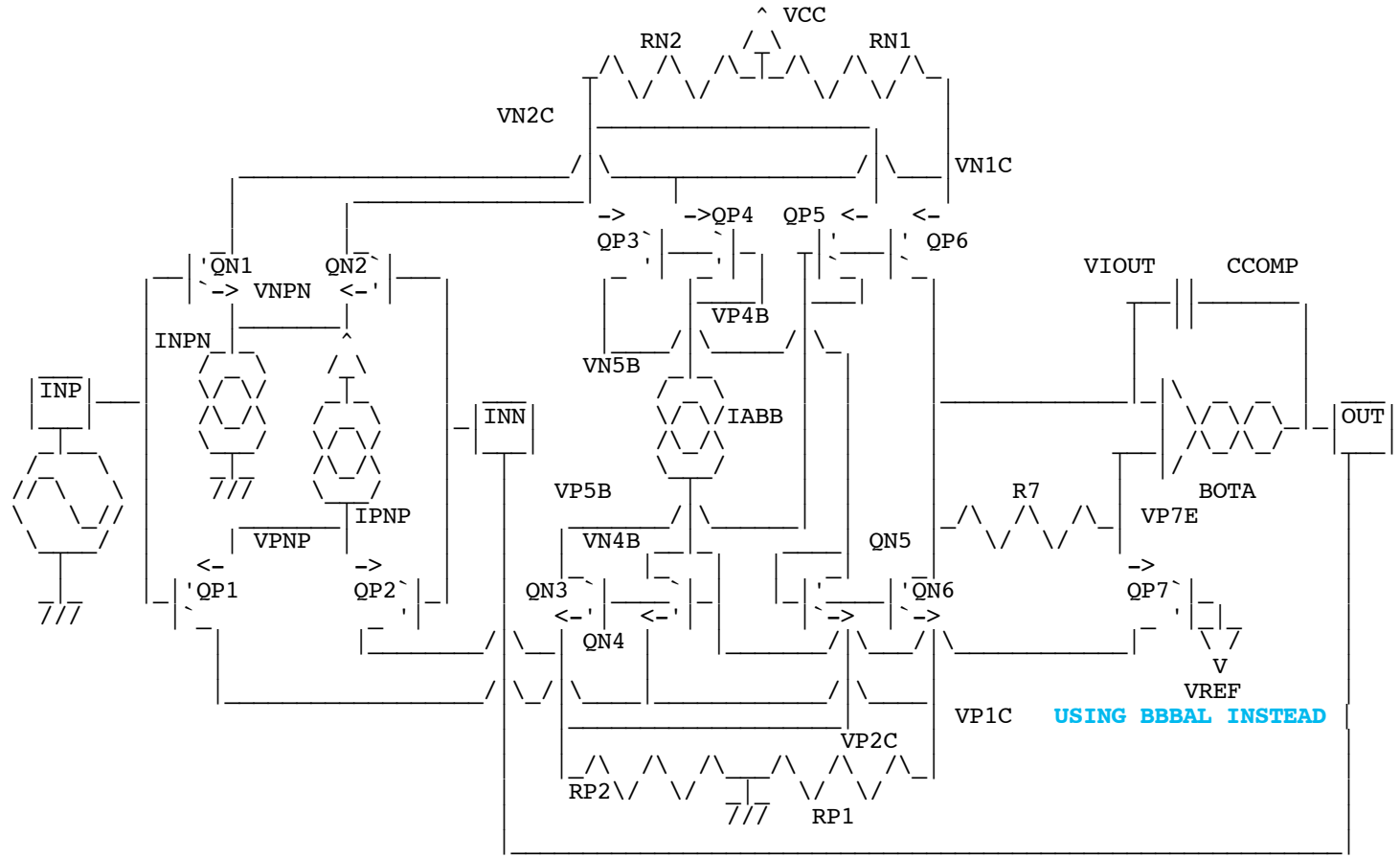
* www.idea2ic.com
* US Patent # 5455535




```
.OPTIONS  method=trap

VIN       INP     0       DC  6  AC 1m
QP1       VP1C    INP     VPNP    PNPV   1
QP2       VP2C    OUT     VPNP    PNPV   1
RP1       VP1C    0       5K
RP2       VP2C    0       5K
QN1       VN1C   INP      VNPN    NPNV   1
QN2       VN2C   OUT      VNPN    NPNV   1
RN1       VCC     VN1C    5K
RN2       VCC     VN2C    5K
```

```
VCC       VCC    0      12
VREF      VREF   0      6
IPNP      VCC    VPNP   20u
INPN      VNPN   0      20n

QP3       VN5B   VP4B   VN2C    PNPV   1
QP4       VP4B   VP4B   VN1C    PNPV   1
QP5       VP5B   VP5B   VN2C    PNPV   1
QP6       VIOUT  VP5B   VN1C    PNPV   1

QN3       VP5B  VN4B    VP2C    NPNV   1
QN4       VN4B  VN4B    VP1C    NPNV   1
QN5       VN5B  VN5B    VP2C    NPNV   1
QN6       VIOUT VN5B    VP1C    NPNV   1

IABB      VP4B   VN4B    5u
BOTA      OUT    0       I = -1*( V(VIOUT) - V(VREF) )*1
CCOMP     OUT    VIOUT   1p
R7        VIOUT  VREF    20K
RL        OUT    VREF    1Meg

VBBAL     VBBAL  0       DC 2.07E14
BBBAL     VN4B   0       I = -1*( V(VIOUT) - V(VREF) )/V(VBBAL)

.model    NPNV   npn      BF=150  CJE=.3p  VAF=200
.model    PNPV   pnp      BF=60   CJE=.3p  VAF=60

.control
run
set        pensize = 2

ac         dec   10    1      100000K
let        gain = v(out)/(  v(out)- v(inp) )
plot       dB(gain ) phase(gain)  title No_Load

alter      RL  resistance = 10k
ac         dec   10    1      100000K
let        gain = v(out)/(  v(out)- v(inp) )
plot       dB(gain ) phase(gain)   title 10K_Load

alter      RL  resistance = 1k
ac         dec   10    1      100000K
let        gain = v(out)/(  v(out)- v(inp) )
plot       dB(gain ) phase(gain)  title 1K_Load

alter      VBBAL  dc = 2.06E4
ac         dec   10    1      100000K
let        gain = v(out)/(  v(out)- v(inp) )
plot       dB(gain ) phase(gain) title 1K_Load_with_Beta_Bal

.endc
.end
```

*** ====================END====================================**

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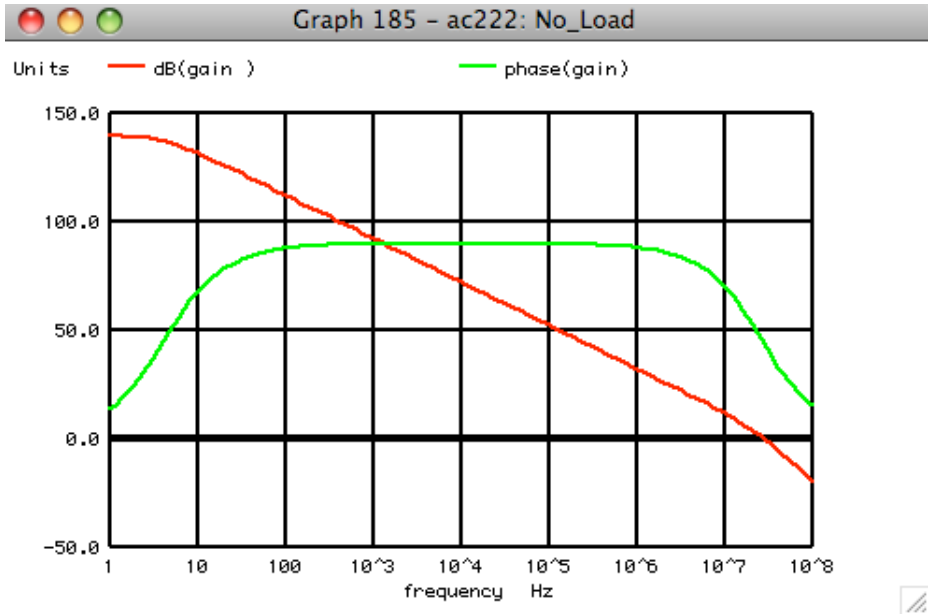
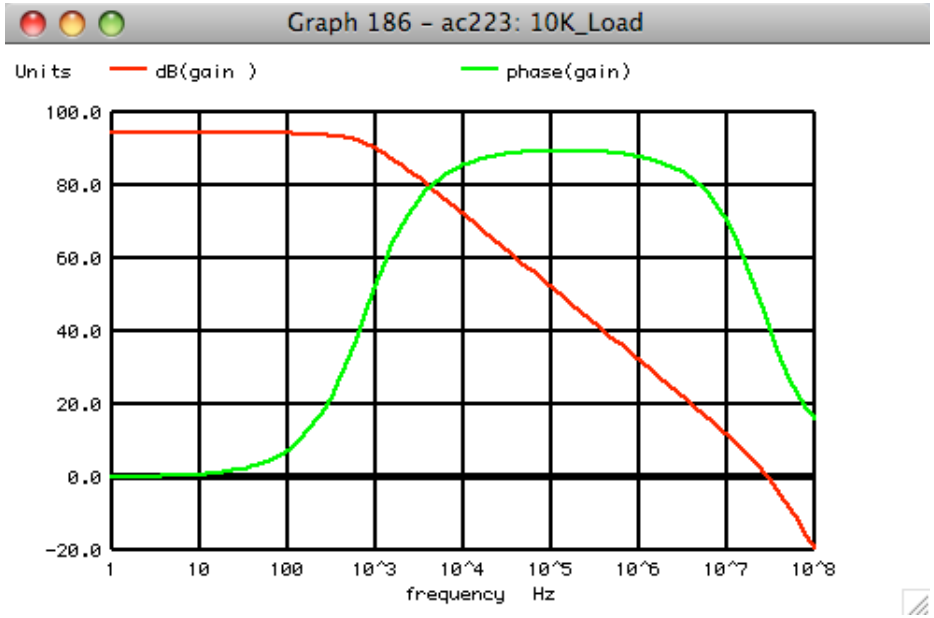
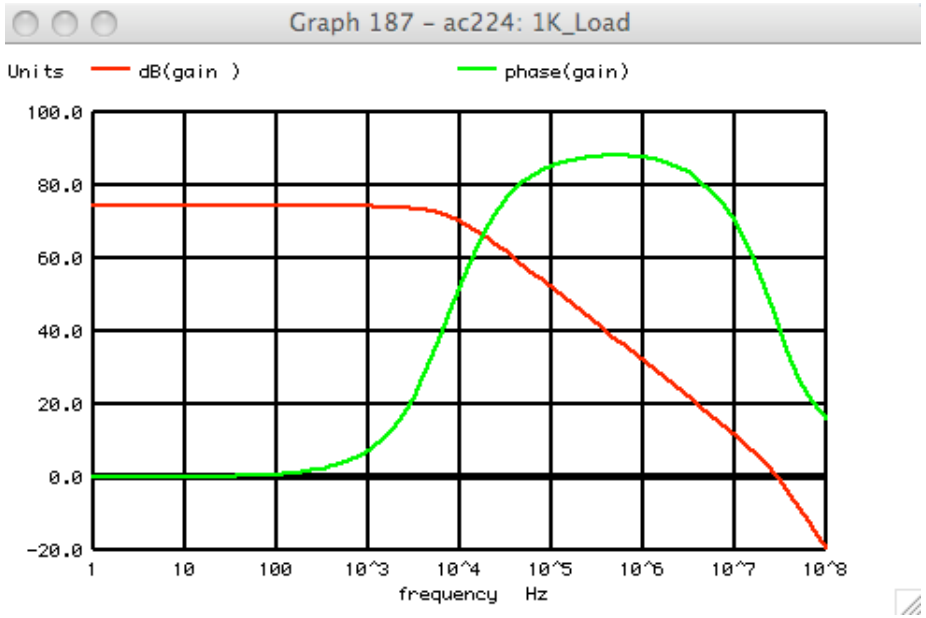
The output stage of a RRIO is effectively a transconductance stage in that it produces output current out of pnp collector off the top rail and a npn collector off the bottom rail.



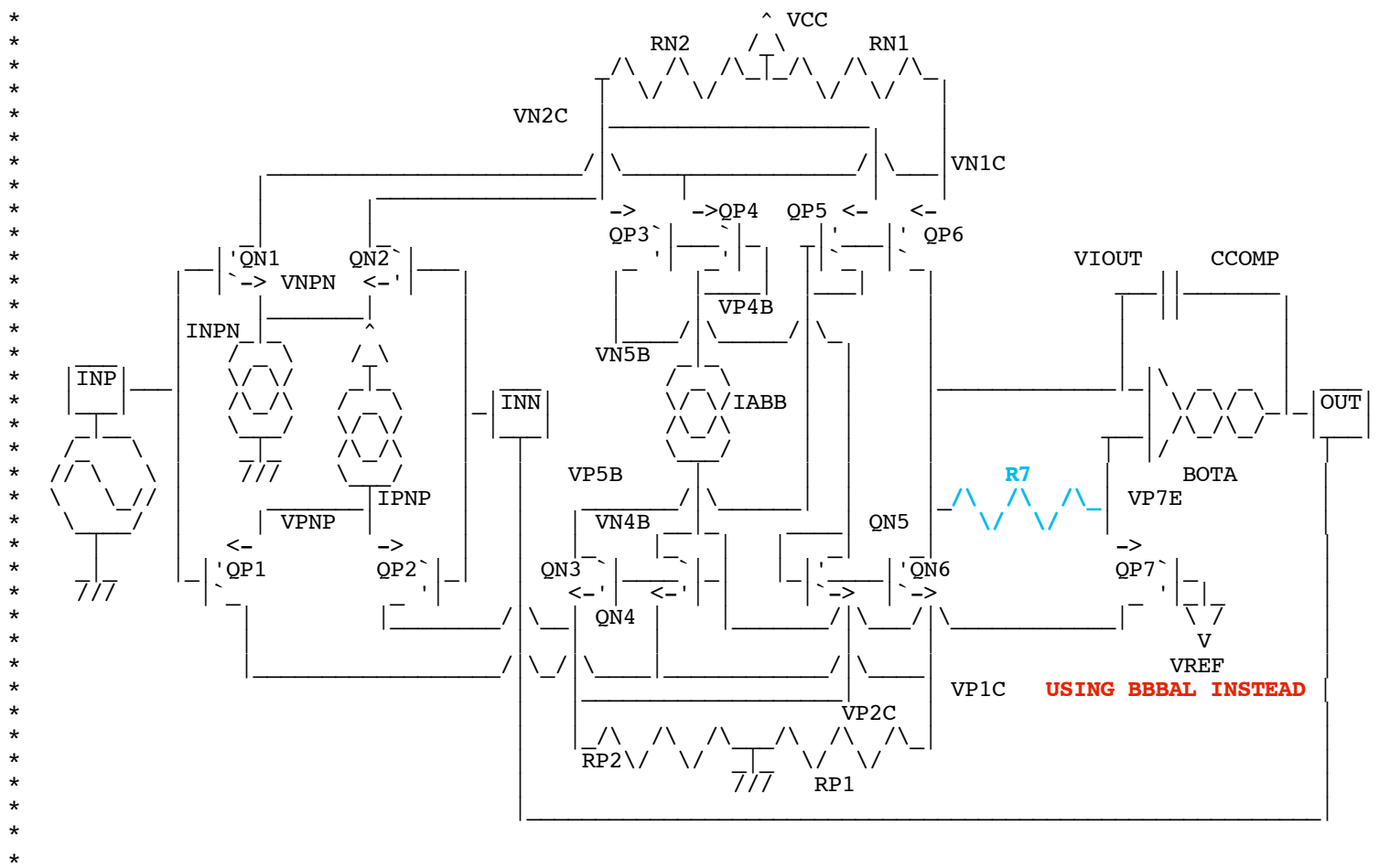
This type of output stage demonstrates a requirement of current gain. When the output stage is not loaded with any resistance or current, the open loop gain of the Op Amp is usually defined by the early voltage of the transistors which is usually high.



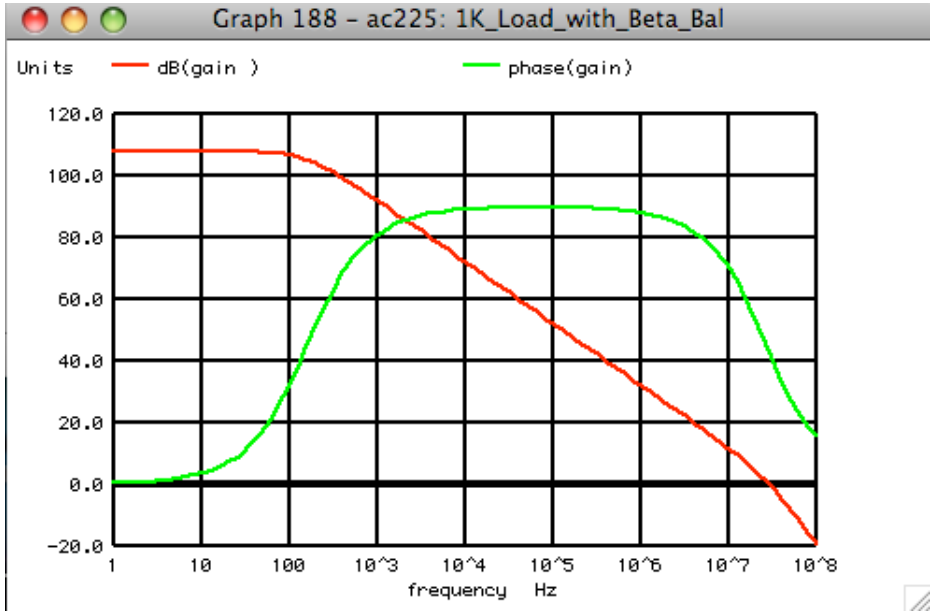
But in bipolar there is always a finite amount of input to output current gain in a transconductance amplifier. This current gain causes an output load to load the open loop gain response.



The spec calls for a 600 ohm load test, and while the LM6142's output stage has the beta gain of two npns in series with a pnp, open loop gain at 600 Ohms is a little lacking.



An extremely simplified version of the LM6142 is shown above. Resistor R7 is not in the circuit but is just being used to model the transconductance amplifier BOTA as having an input bias current generated by its output current. In the LM6142, a buffering transistor like QP7 does have a free collector which is being fed back into the dual input turn around to cancel out the loading of the output stage.



The effect can be thought of as balancing out the errors of beta. While the exact magnitude of a beta error can not be known, any equal and opposite error coming from the same source can be recruited to cancel out both errors.