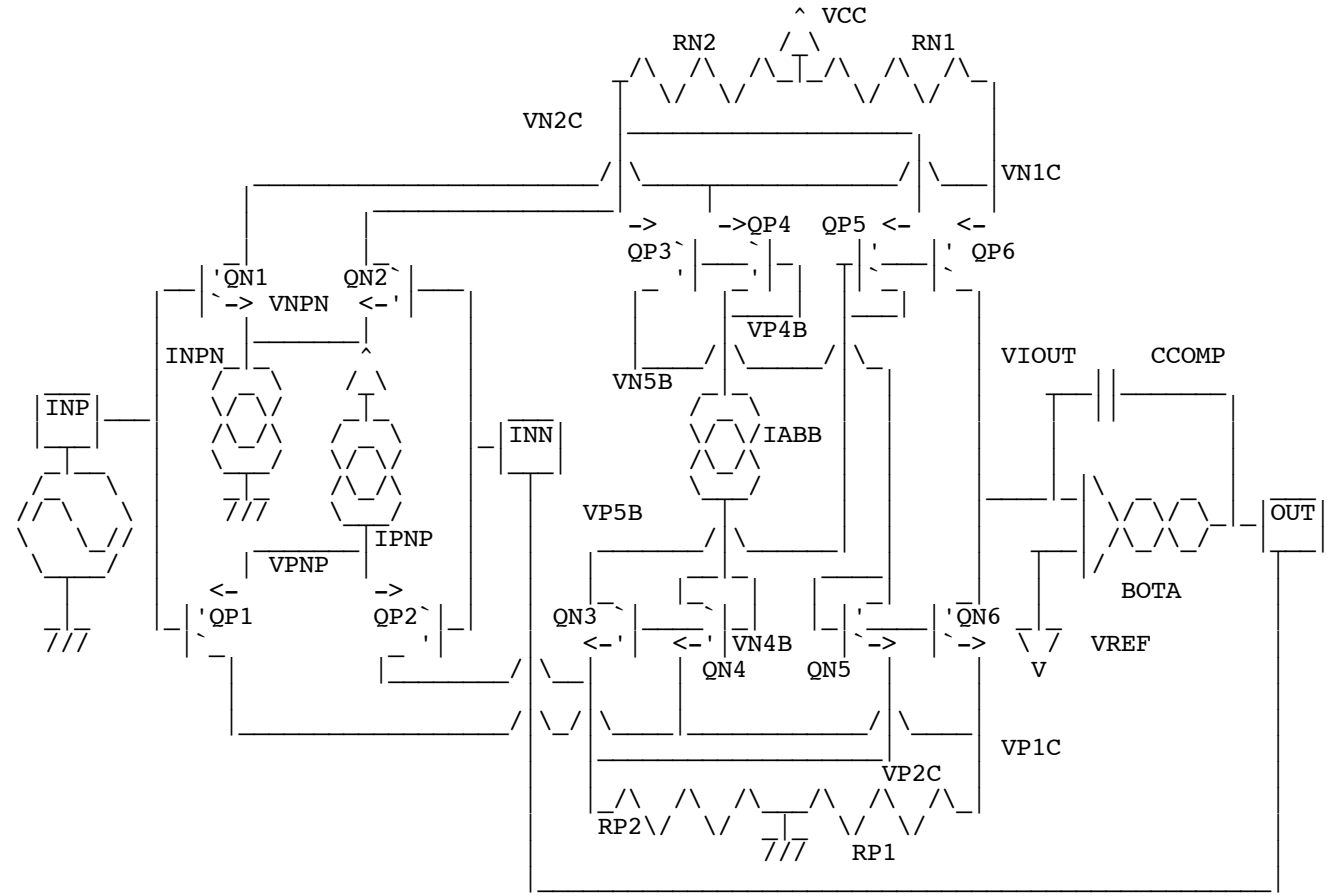
AB_BIAS_TURNAROUND

* dsauersanjose@aol.com 12/17/08
* www.idea2ic.com

* US Patent # 5455535




```
.OPTIONS  method=trap

VIN       INP     0      PULSE( 1 9 1n 1n 1n 10u 20u ) dc 6
QP1       VP1C    INP    VPNP    PNPV   1
QP2       VP2C    OUT    VPNP    PNPV   1
RP1       VP1C    0      5K
RP2       VP2C    0      5K
QN1       VN1C   INP     VNPN    NPNV   1
QN2       VN2C   OUT     VNPN    NPNV   1
RN1       VCC    VN1C    5K
RN2       VCC    VN2C    5K
```

```
VCC       VCC    0      12
VREF      VREF   0      6
IPNP      VCC    VPNP   20u
INPN      VNPN   0      20n

QP3       VN5B   VP4B    VN2C    PNPV   1
QP4       VP4B   VP4B    VN1C    PNPV   1
QP5       VP5B   VP5B    VN2C    PNPV   1
QP6       VIOUT  VP5B    VN1C    PNPV   1

QN3       VP5B  VN4B     VP2C    NPNV   1
QN4       VN4B  VN4B     VP1C    NPNV   1
QN5       VN5B  VN5B     VP2C    NPNV   1
QN6       VIOUT VN5B     VP1C    NPNV   1

IABB      VP4B   VN4B    2u
BOTA      OUT    0     I = -1*( V(VIOUT) - V(VREF) )/50
CCOMP     OUT    VIOUT 20p

.tran     100n   50u     0      100n
.model    NPNV   npn     BF=150
.model    PNPV   pnp     BF=150

.control
run
set        pensize = 2
*plot       v(out) v(inp)
echo       "4% Area Sensistivity vs Transistor  \n"           "
echo       "MissMatch    Device       Input_Offset_mV"
op
let        voffset =  (v(out)- v(inp))*1000
echo       "0%           QP1          $&voffset"
alter      QP1    area =1.04
op
let        voffset =  (v(out)- v(inp))*1000
echo       "4%           QP1          $&voffset"
alter      QP1    area =1
alter      QP2    area =1.04
op
let        voffset =  (v(out)- v(inp))*1000
echo       "4%           QP2          $&voffset"
alter      QP2    area =1
alter      QP3    area =1.04
op
let        voffset =  (v(out)- v(inp))*1000
echo       "4%           QP3          $&voffset"
alter      QP3    area =1
alter      QP4    area =1.04
op
let        voffset =  (v(out)- v(inp))*1000
echo       "4%           QP4          $&voffset"
```

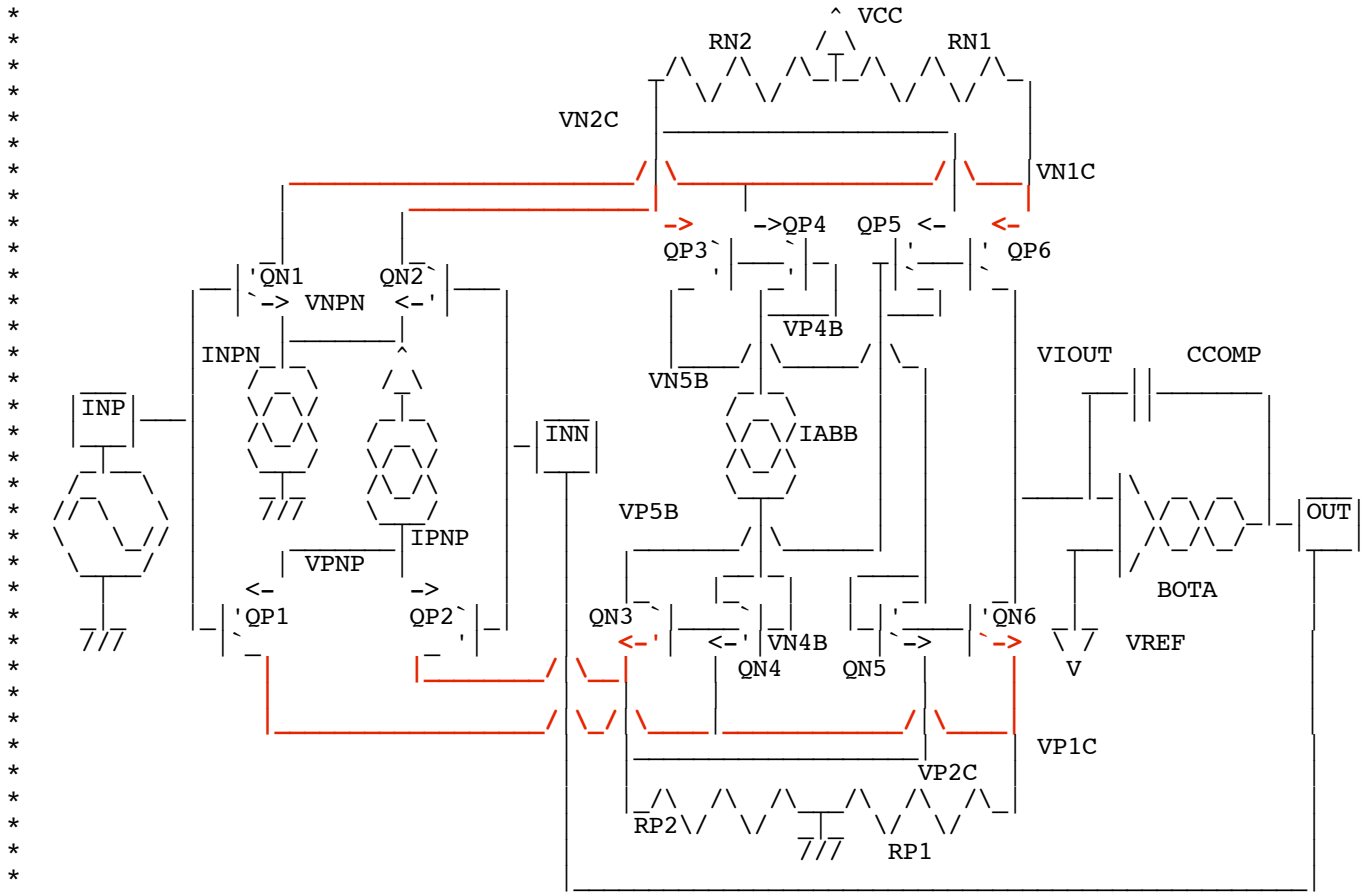
```
alter      QP4    area =1
alter      QN1    area =1.04
op
let        voffset =  (v(out)- v(inp))*1000
echo       "4%           QN1          $&voffset"
alter      QN1    area =1
alter      QN2    area =1.04
op
let        voffset =  (v(out)- v(inp))*1000
echo       "4%           QN2          $&voffset"
alter      QN2    area =1
alter      QN3    area =1.04
op
let        voffset =  (v(out)- v(inp))*1000
echo       "4%           QN3          $&voffset"
alter      QN3    area =1
alter      QN4    area =1.04
op
let        voffset =  (v(out)- v(inp))*1000
echo       "4%           QN4          $&voffset"
alter      QN4    area =1
alter      RN1    resistance =5050
op
let        voffset =  (v(out)- v(inp))*1000
echo       "1%           RN1          $&voffset"
alter      RN1    resistance =5000
alter      RN2    resistance =5050
op
let        voffset =  (v(out)- v(inp))*1000
echo       "1%           RN2          $&voffset"
alter      RN2    resistance =5000
alter      RP1    resistance =5050
op
let        voffset =  (v(out)- v(inp))*1000
echo       "1%           RP1          $&voffset"
alter      RP1    resistance =5000
alter      RP2    resistance =5050
op
let        voffset =  (v(out)- v(inp))*1000
echo       "1%           RP2          $&voffset"


.endc
.end
```

*** ====================END==================================**

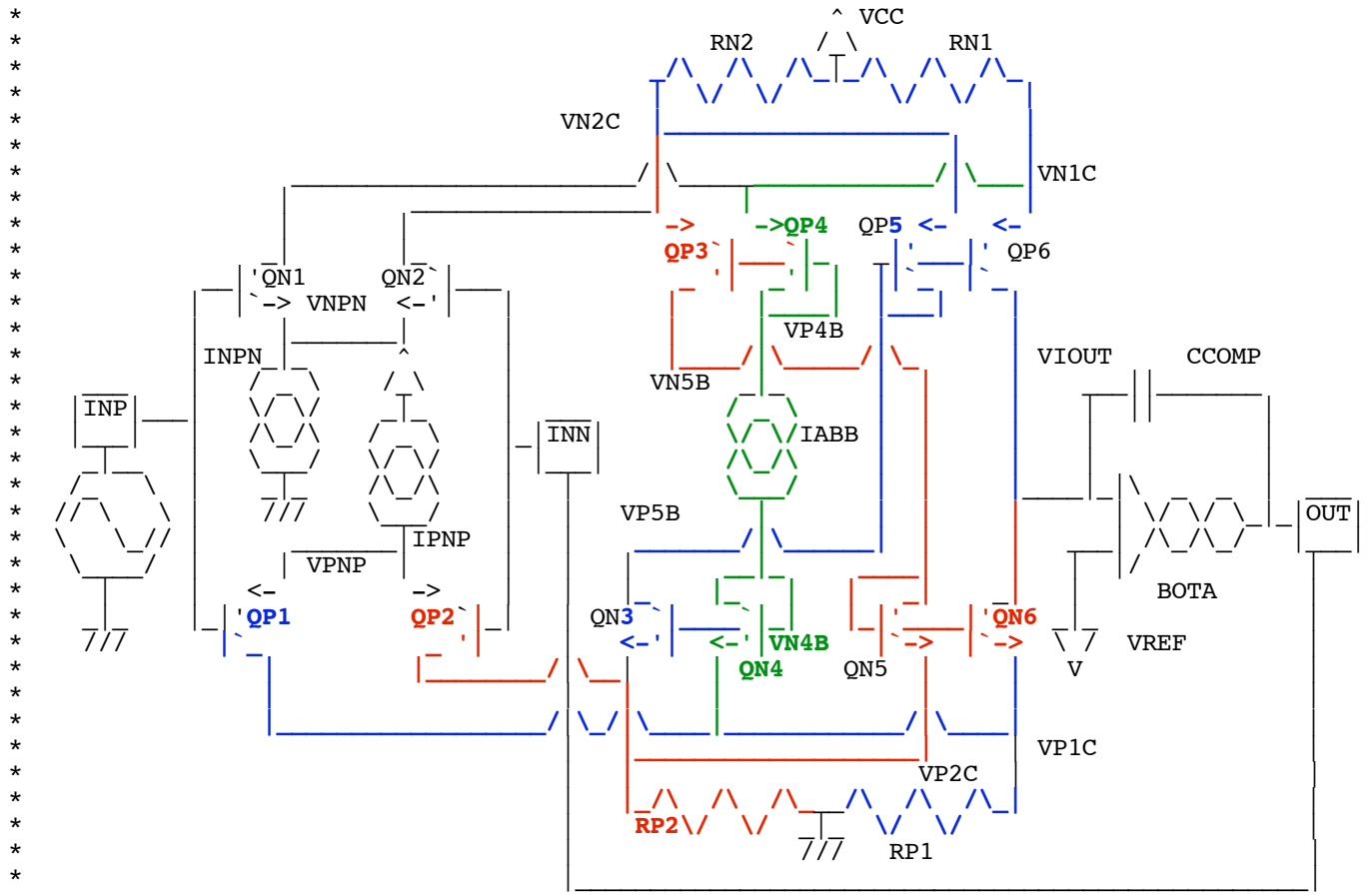
The goal of any Op Amp design is to minimize input offset voltage and input referred to noise. This implies that both offset and noise should be dominated by only the input stage and that all following stage should be insignificant. Both noise a offset add with power such that in input stage which contributes a 1mV standard deviation of input offset which is followed by second stage which contributes 1/5mV of offset will have a combined offset of..

1.02 = sqrt(1^2 +(.2)^2)

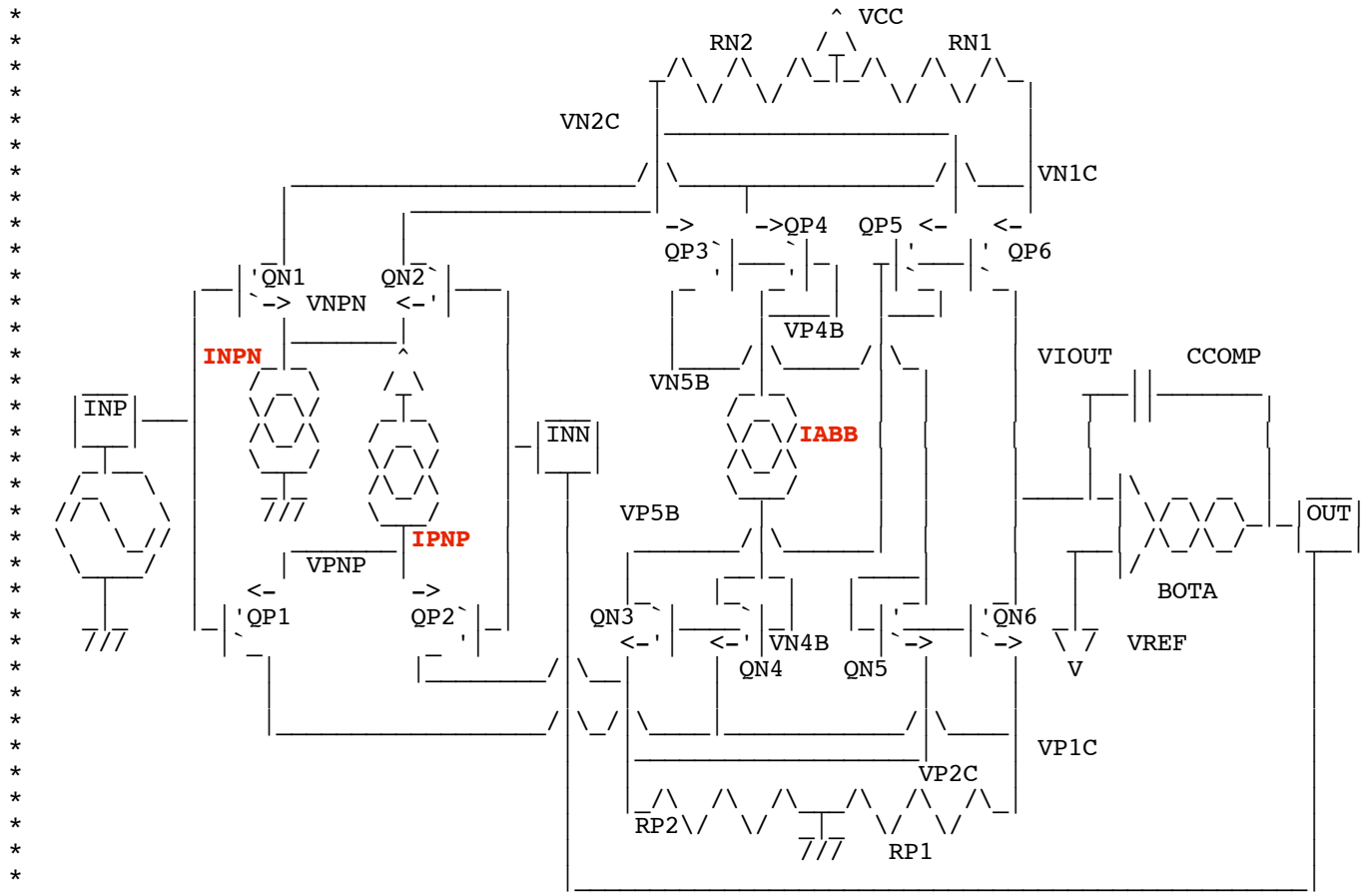
For the LM6142, the two input stages needed to be combined together such that either input stage could work as well. Plus there was the added requirement that the inputs should be able to exceed both rails by 200mV. There was another requirement for the LM6142. The cell phone application at the time was needing an Op Amp with greatly that 10MegHz GainBandWidth Product which of course had to be unity gain stable with a 200pF load capacitor. And add to this the noise and offset should always be dominated by the input.



Several things were discovered using the circuit above. Driving signal into an emitter of a transistors as actually the first way transistors were used. This "common base" drive has the advantage in that it is one of the fastest ways to drive a bipolar transistor. Given that the input stages wanted to have their collectors go to resistor anyway was convenient. Resistors have low offset and noise. Having an input stage take gain in some resistors was a common practice.



This dual input turn around stage is using diode and cross coupling to communicate a differential signal from one end to the other. In the circuit above, assume QP1 is turning off (getting cold) while QP2 is turning on (getting warm). A differential signal is involving all the transistors and resistors. The resistor a driving base voltage through diodes and directly driving emitters.



There is another important feature in that this stage operates in an AB bias mode. Current source IABB is chosen to be much less that what INPN or IPNP. A 1mV offset in the input stage represents a 4% area mismatch. If all the transistors in the turn around stage are running at a much lower current, then their 4% contribution of mismatch is at a smaller current level.

MissMatch	Device	Input_Offset_mV
0%	QP1	-7.71252E-07
4%	QP1	**-1.0134**
4%	QP2	**1.0134**
4%	QP3	0.262465
4%	QP4	-0.26256

4%	QN1	0.00101179
4%	QN2	-0.00101337
4%	QN3	-0.2625
4%	QN4	0.262525
1%	RN1	0.102932
1%	RN2	-0.102494
1%	RP1	-0.359263
1%	RP2	0.35926

The simulation is performing a transistor by transistor mismatch on all transistors and measuring the resulting input offset. A 1mV or 4% mismatch for transistor and a 1% mismatch for resistor may be a little high. But their close enough to be convenient.

From the table that the simulation prints out, the input transistors QP1 and QP2 dominate. The input is configured in the LM324 mode which is just pnp inputs. As desired, the process parameters of the vertical input pnps define most of the performance specs.