Rbase_Remitter_Tracking

```
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* www.idea2ic.com
*
*                    ____                  ___                    __
*          _________/   /|_________________/   /|_________________/  /|______
*                / /   / /    /              /   / /               /   /  / /  /
*               / /   / /    /  N EMITTER   /   / /  N EMITTER   /   /  / /  /
*              / /   / /    /               /   / /               /   /  / /  /
*             / /   / /    /               /   / /               /   /  / /  /
*            / /   / /    /               /   / /               /   /  / /  /
*           / /   / /    /               /   / /               /   /  / /  /
*          / /   / /    /               /   / /               /   /  / /  /
*         / /___/ /    /               /___/ /               /   /  / /  /
*   ______/__|___|/____/_______________|___|/_______________/____|___|/__/_____
*         |                            +                   +                  |
*         | P BASE      | ./\  .../\  ........./\  .../\  .  |  P BASE       |
*         |             \    \/     \/-      - \/     \/ /                   |
*         |              \_____________________________/                     |
*         \               ./\  .../\  ......./\  .../\  .                    /
*          \                \/  +  \/-     - \/+    \/                       /
*           \_____________________________________________________________/
*
 *
 *                    ^            ^            ^            ^
 *                 QN1/_\       QN2/_\       QN3/_\       QN4/_\
 *                   _|_    RB1   _|_    RB2   _|_    RB3   _|_
 *              |'_____/\  __|'_____/\  __|'_____/\  __|'
 *          _|_ |`->    \/   |`->    \/   |`->    \/   |`->
 *         /VEE\        |_/\  __   |_/\  __   |_/\  __   |_/\  __
 *         \___/         \/      |   \/      |   \/      |   \/      |
 *          _|_                  |           |           |           |
 *          ///                  |_/\  _____|_/\  _____|_/\  _____|
 *                                  \/ RS1      \/ RS2      \/ RS3   _|_
 *                                                                    ///
```

```
VCC     VC      0       DC      8
VBE     VB1     0       DC      1.5
QN1     VC      VB1     VE1     NPNP
QN2     VC      VB2     VE2     NPNP
QN3     VC      VB3     VE3     NPNP
QN4     VC      VB4     VE4     NPNP

RB1     VB1     VB2     6000
RE1     VE1     VS1     30
RS1     VS1     VS2     30

RB2     VB2     VB3     6000
RE2     VE2     VS2     30
RS2     VS2     VS3     30

RB3     VB3     VB4     6000
RE3     VE3     VS3     30
RS3     VS3     0       30
RE4     VE4     0       30



.tran    100m   8    0      100m

.control
run
set pensize = 2

plot vb1 - vb2 ve1 - ve2  vb2 - vb3 ve2 - ve3 vb3 - vb4 ve3 - ve4  ylimit .3 0
.endc
```

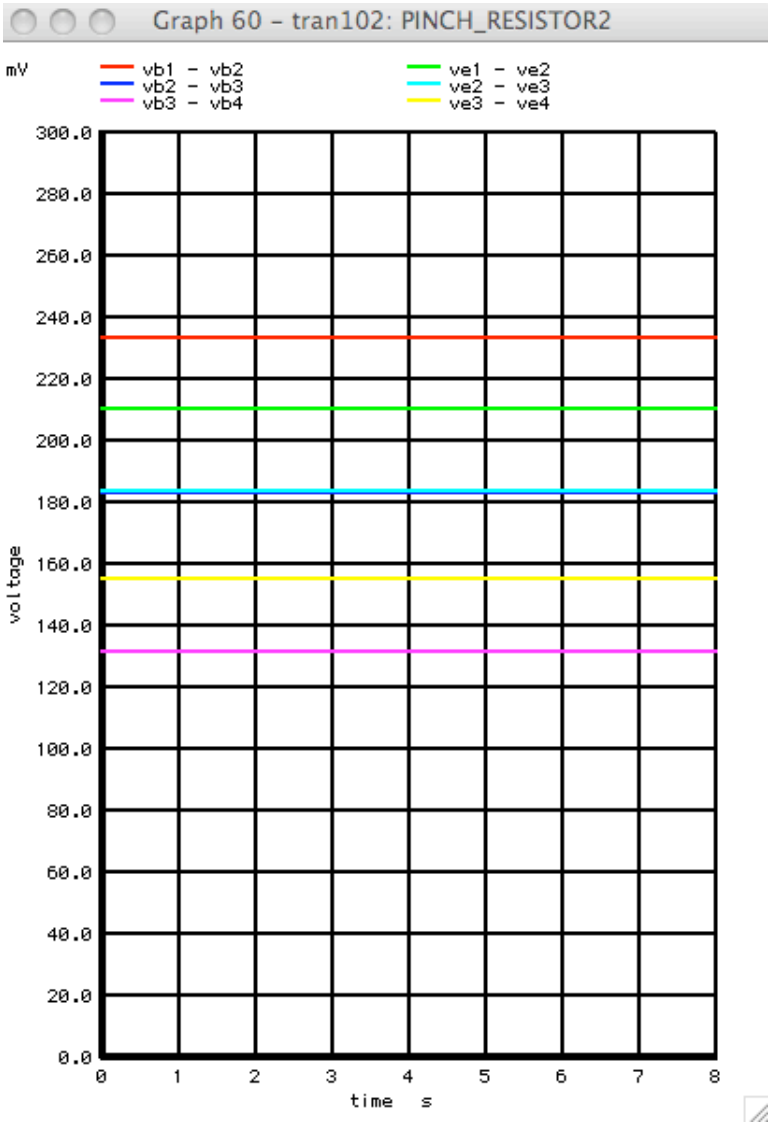
```
.model    NPNP   NPN( BF=210 )
```

.end

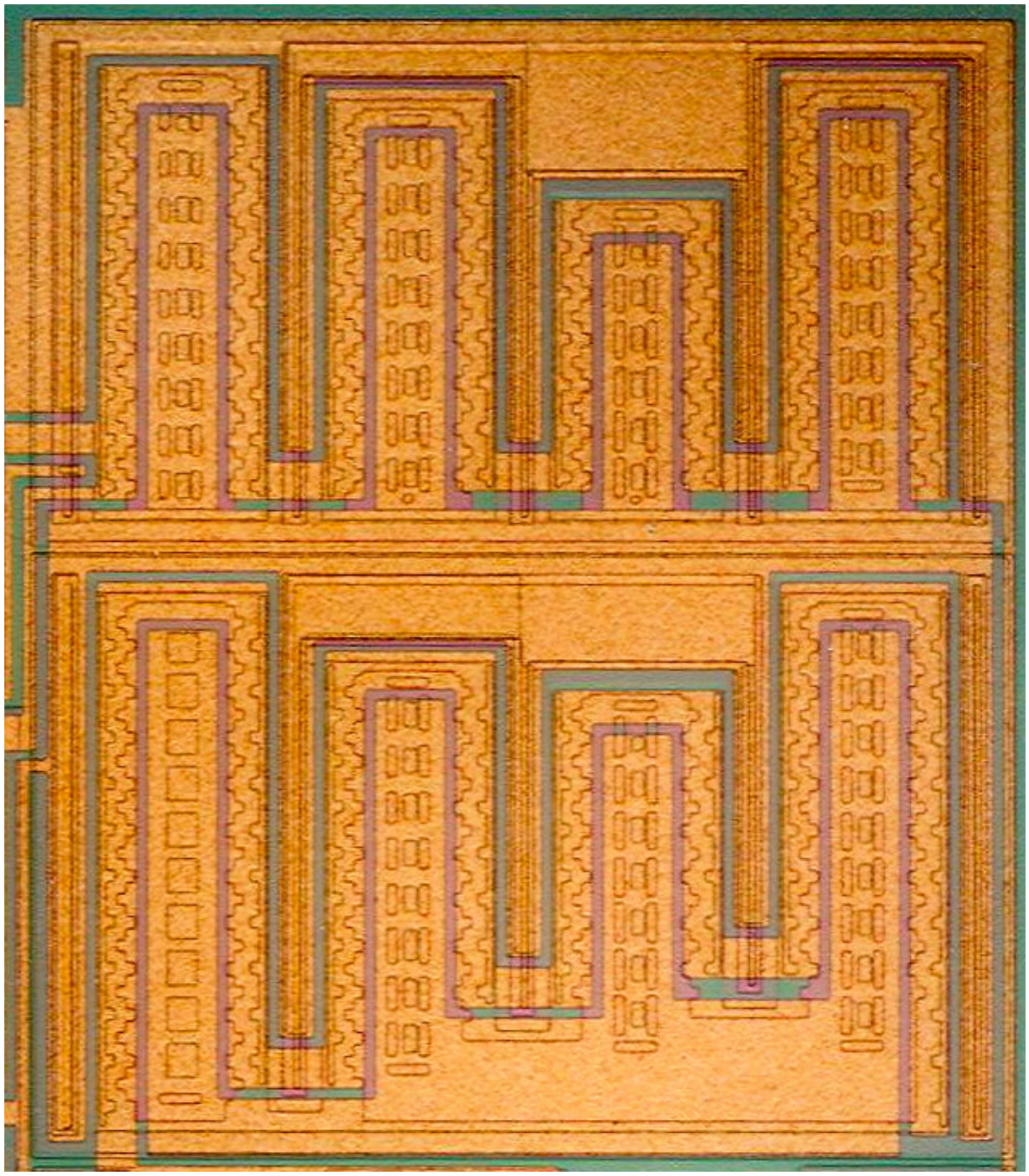
======Rbase_Remitter_Tracking==========

```
*
*                 ____                    ___                    __
*          _________/   /|_________________ /   /|_________________/  /|______
*                / /   / /    /            /   / /                /   /  / /  /
*               / /   / /    /  N EMITTER  /   / /  N EMITTER    /   /  / /  /
*              / /   / /    /            /   / /                /   /  / /  /
*             / /   / /    /            /   / /                /   /  / /  /
*            / /   / /    /            /   / /                /   /  / /  /
*           / /   / /    /            /   / /                /   /  / /  /
*          / /   / /    /            /   / /                /   /  / /  /
*         / /___/ /    /            /___/ /                /   /___/ /  /
*   ______/__|___|/____/____________|___|/________________/____|___|/__/_______
*         |  P BASE     | ./\  .../\  ........./\  .../\  .  |  P BASE      |
*         |             \    \/     \/-       - \/     \/ /                  |
*         |              \_____________________________/                     |
*         \               ./\  .../\  ......./\  .../\  .                    /
*          \                \/  +  \/-     - \/+    \/                       /
*           \_____________________________________________________________/
*
*
*                    ^            ^            ^            ^
*                 QN1/_\       QN2/_\       QN3/_\       QN4/_\
*                   _|_    RB1   _|_    RB2   _|_    RB3   _|_
*              _____|'____/\___|'____/\___|'____/\___|'
*             |_|_   |`->    \/   |`->    \/   |`->    \/   |`->
*            /VEE\  VB1   |  RE1 VB2  |  RE2 VB3   |  RE3  VB4  |    RE4
*            \___/        |_/\___     |_/\___      |_/\___      |_/\___
*             _|_              \/        \/         \/         \/
*             ///                |         |         |         |
*                                |_/\_______|_/\_______|_/\_________|
*                                   \/ RS1      \/ RS2      \/ RS3   _|_
*                                                                    ///
```

The OLD analog process tends to match the IR drop in the base region with the IR drop in the natural emitter resistors. The simulation is modeling transistor regions as squares. A pinch resistance value of 6k Ohms per square is being at the bases and 30 Ohms per square for the emitters. The IR in both base and emitters are going in the same direction and are close to the same value due to beta.



The current in all the transisters is withing +/- of the average. However the layout for the actual output transistor went to even further lengths to encourage all transistors to draw the same current.



In the actual output transistor layout the IR drop in the metal is also of the same magnitude. The output transistors were designed such that at 5 Amps, every transistor region would see both the same current the same environmental 250mV of IR drop. Where the IR drop would take place would differ between the transistors.

```
*
*
*           _____________________________________________________________
*                 / /Cont___/        /                       /      /___ Cont/  /
*                / /Cont/      _____/          ____        /_____     /Cont/  /
*               / /Cont/     /  N EMITTER   /Cont/   N EMITTER  /    /Cont/  /
*              / /Cont/     /             /Cont/        _____    /    /Cont/  /
*             / /Cont/     /    /BASE/    /Cont/   /BASE/     /    /Cont/  /
*            / /Cont/     /    /____/    /Cont/   /____/     /    /Cont/  /
*           / /Cont/     /              /____/              /    /Cont/  /
*          / /Cont/__   /_____                          _____/   __/Cont/  /
*         / /Cont   /        /       N EMITTER       /        /  Cont/  /
*   ______/_/_______/________/_______________________/________/______/__/_____
*         |                 |                       |                       |
*         | P BASE          |       N EMITTER       |      P BASE           |
*         |                  \                     /                        |
*         |                   \___________________/                         |
*         \                                                                 /
*          \                                                               /
*           \_____________________________________________________________/
*
 *
 *                    ^          ^          ^          ^
 *                QN1/_\      QN2/_\      QN3/_\      QN4/_\
 *                   _|_    RB1   _|_    RB2   _|_    RB3   _|_
 *            ______|'____/\  __|'____/\  __|'____/\  __|'
 *          _|_     |`->    \/  |`->    \/  |`->    \/  |`->
 *         /VEE\        |   RE1      |   RE2      |   RE3      |   RE4
 *         \___/        |_/\  __     |_/\  __     |_/\  __     |_/\  __
 *          _|_            \/  |       \/  |       \/  |       \/  |
 *          ///               |_/\  _______|_/\  _______|_/\  _______|
 *                                \/ RS1      \/ RS2      \/ RS3   _|_
 *                                                                  ///
```

The layout was done by assuming all transistors shared equally the same current at 5Amps. All IR drops where calculated everywhere. Then holes where made in the N+ emitter doping regions to see to it that all all transistor regions where seeing the same vbe voltage. This current matching was later verified through the use of liquid crystals on a probe station.

***#1==========WinSpiceVersion==========**

```
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*
*           __________/____/|_________________ /___/|_________________/  __/|______
*                 / /   / /    /                /   / /                /   / /  /
*                / /   / /    /  N EMITTER     /   / /  N EMITTER    /   /   / /  /
*               / /   / /    /                /   / /               /   /   / /  /
*              / /   / /    /                /   / /               /   /   / /  /
*             / /   / /    /                /   / /               /   /   / /  /
*            / /   / /    /                /   / /               /   /   / /  /
*           / /   / /    /                /   / /               /   /   / /  /
*          / /___/ /    /               /___/ /               /   /___/ /  /
*   ______/__|___|/____/_______________|___|/_______________/____|___|/__/_____
*         |             |        +                +         |             |
```

```
*          | P BASE     | ./\  .../\  ........./\  .../\  . |  P BASE    |
*          |            \    \/     \/-       - \/     \/ /               |
*          |             \_____________________________/                  |
*         \              ./\  .../\  ......./\  .../\  .                 /
*          \               \/  +  \/-     - \/+    \/                   /
*           \_____________________________________________________________/
*
 *
 *                     ^           ^           ^           ^
 *                 QN1/_\      QN2/_\      QN3/_\      QN4/_\
 *                   _T    RB1   _T    RB2   _T    RB3   _T
 *            _____|'____/\ __|'____/\ __|'____/\ ___|'
 *          _|_        |`->    \/  |`->    \/  |`->    \/   |`->
 *         /VEE\       |   RE1     |   RE2     |   RE3     |    RE4
 *         \___/       |_/\ __     |_/\ __     |_/\ __     |_/\ __
 *          _|_            \/ |        \/ |        \/ |        \/ |
 *          ///               |          |          |          |
 *                            |_/\ ______|_/\ ______|_/\ ______|
 *                                \/ RS1      \/ RS2      \/ RS3   _|_
 *                                                                  ///
```

```
VCC     VC      0       DC      8
VBE     VB1     0       DC      1.5
QN1     VC      VB1     VE1     NPNP
QN2     VC      VB2     VE2     NPNP
QN3     VC      VB3     VE3     NPNP
QN4     VC      VB4     VE4     NPNP

RB1     VB1     VB2     6000
RE1     VE1     VS1     30
RS1     VS1     VS2     30

RB2     VB2     VB3     6000
RE2     VE2     VS2     30
RS2     VS2     VS3     30

RB3     VB3     VB4     6000
RE3     VE3     VS3     30
RS3     VS3     0       30
RE4     VE4     0       30

.op
.control
run
set pensize = 2
print vb1 - vb2;
print ve1 - ve2
print vb2 - vb3
print ve2 - ve3
print vb3 - vb4
print ve3 - ve4
.endc

.model    NPNP   NPN( BF=210 )

.end
```