LOW_CROSSOVER_DISTORTION

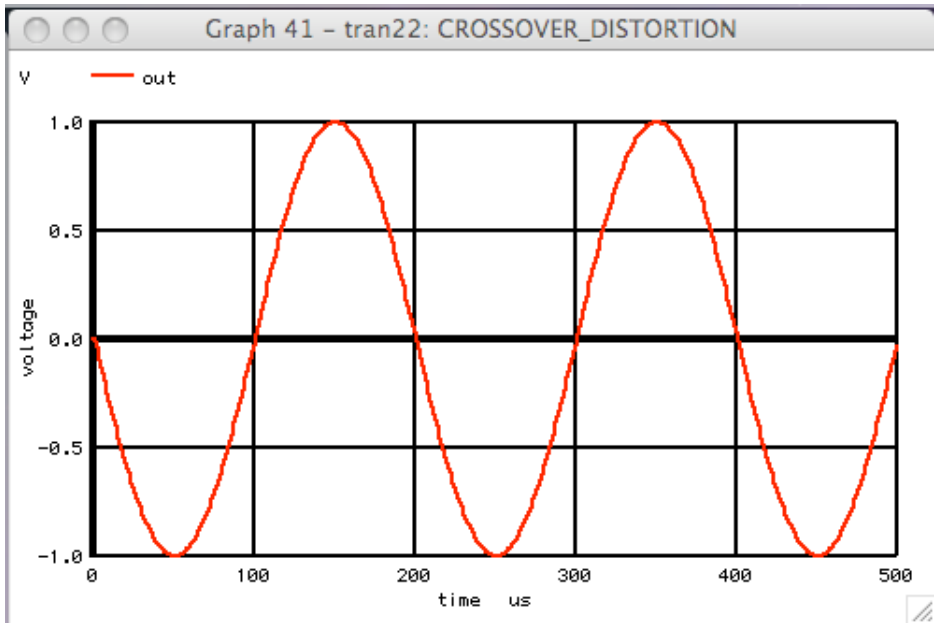
```
* dsauersanjose@aol.com  8/15/08
* www.idea2ic.com
*
*
*                                R2   100k
*                              _/\  /\  /\_____________________
*                             |   \/  \/                       |
*                             |                          VC ^   |
*                             |                            /_\  |
*          R1 1K              |                       _____|    |
*                             |                      |  _|      |
*    ____                     |\                     |_|'QN1 |_|'QN2
*   |IN |_/\  /\  /\_|INN|___|_|-\ OUT1 |            |`->   |`-> 100X
*   |___|   \/  \/   |___|   |  \_____|             |VEM     |_____|_|OUT|_____
*    _|_                     |  /                   <-                |___|     |
*   /VIN\    ^ VC   ^ VE     |+/                 |'QP1     <-                   |
*   \___/   /_\    /_\       |/                  |`_      |'QP2 100X            |
*     |      _|_    _|_      _|_                 |____|__|_|`_          RL  8   |
*     _|_   /VCC\  /VEE\    ///                  VPB1       |       _/\  /\  /\__|
*    ///    \___/  \___/                        _|_         _|_      |  \/  \/
*            |      |                          /_ _\       \ /    _|_
*           _|_    _|_                         \/_\/ I1    VE V    ///
*           ///    ///                         /\_/\
*                                              \___/
*                                               _|_
*                                               \ /
*                                                V
*
VCC     VC      0     DC     6
VEE     VE      0     DC     -6
VIN     IN      0     DC     0    SIN( 0 10m 5k 1n )
R1      IN      INN   1k
R2      INN     OUT   100k
RL      OUT     0     8
X_OPA   INN     0     OUT1    OP_AMP
QN2     VC      OUT1  OUT     NPNP 100
QP2     VE      VPB   OUT     PNPP 100
QN1     OUT1    OUT1  VEM     NPNP
QP1     VPB     VPB   VEM     PNPP
I1      VPB     0     7u
.tran    1u   .5m    0      1u
.control
run
set     pensize = 2
plot    out
plot    out  out1 vpb
alter  R1  resistance = 10000G
run
plot    -vcc#branch  ylimit 0 1m
.endc

.SUBCKT  OP_AMP INN   INP  OUT
EGBUF    VDIFF  0     INN  INP  1
RGM      VDIFF  VGND2 1k
CBW      OUT    VGND2 8p
EGOUT    OUT    0     VGND2 0    -100000000
.ENDS    OP_AMP
*
*                        CBW _|____|          ____          .SUBCKT OP_AMP INN INP OUT
*                  VDIFF      ___|_|_____|OUT|
*                        ___/\   ___|_ /   \                 ____   |\
*      |INN|__      _|_    \/   |_ |EGOUT|                 |INN|__| \
*      |___|  _ /   \ RGM VGND |  \___/                     |___|   \
*             +|EGBUF|        __|_|                                 OPA\_|OUT|
*              __|  \___/      |  GAIN=-1M                  ____    /|___|
*      |INP|__|  \___/        |_|                          |INP|__|  /
*      |___|     |  GAIN=1  ///  ___|_|                    |___|    /
*                |_|              ///                                |/
*                ///                     ODB = 20MHz
*
```

```
.model    NPNP   NPN(   BF=21000 )
.model    PNPP   PNP(   BF=21000 )
```

.end

======Low_CrossOver_Distortion==========

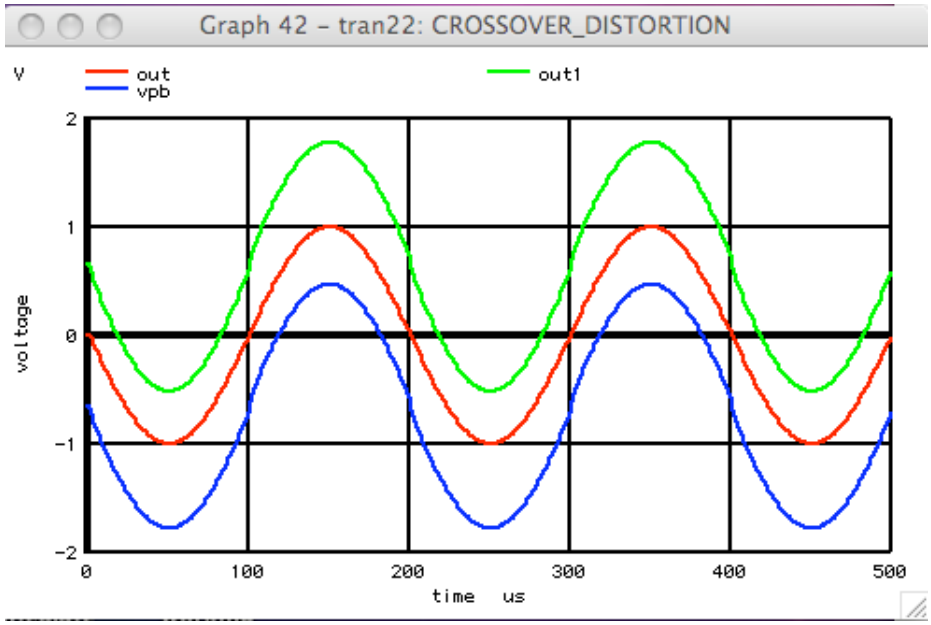
Selecting a level of "AB" bias for the output transistors is a matter of taste. Too much and your wasting supply current. Too little and there is crossover distortion.

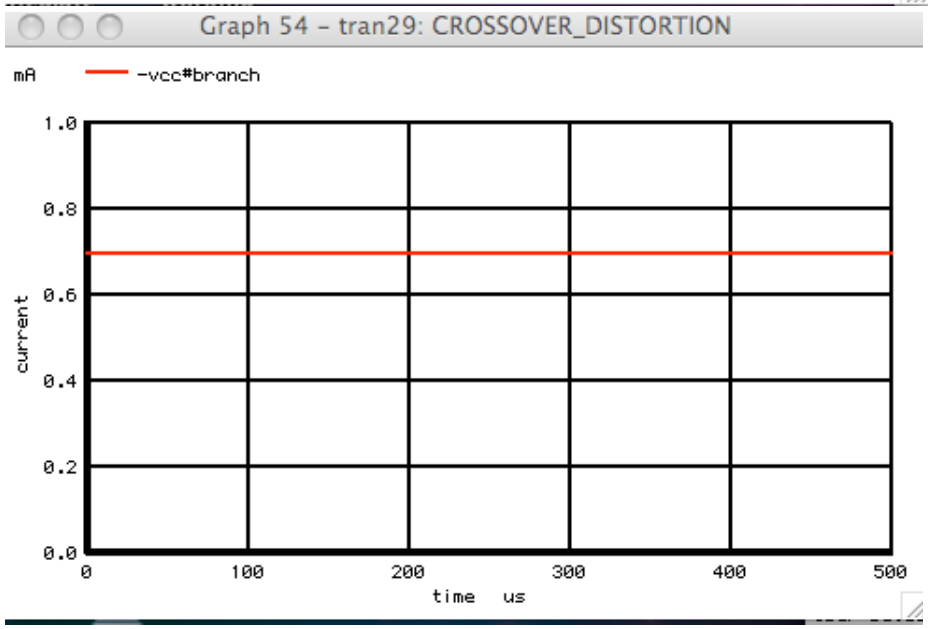



```
*
*                                R2   100k
*                             _/\  /\  /\____________________
*                            |   \/  \/                      |
*                            |                          VC ^  |
*                            |                            /_\ |
*          R1 1K             |                 _______    _T  |
*    ___                     |                |  _T  |  _T   |
*   |IN |_/\  /\  /\_|INN|__|_|\              |_|'QN1 |_|'QN2 |
*   |___|   \/  \/   |___|  |-\ OUT1 |        |`->   |`-> 100X
*    _|_                    |  \_____|        |VEM    |_____|_|OUT|_____
*   /VIN\     ^ VC    ^ VE  |  /               <-      |     |___|
*   \___/    /_\     /_\    |+/            _|'QP1     <-      |
*     |      _T_      _T_    |/            |`_    _|'QP2 100X |
*    _|_    /VCC\   /VEE\   _|_            |____|__|`_        RL  8
*    ///    \___/   \___/   ///             VPB1     |      _/\  /\  /\__|
*            |       |                     _|_\      _|_    |   \/  \/
*           ///     ///                   /_ _\     \ /    _|_
*                                         \/ \/ I1   VE V   ///
*                                         /\_/\
*                                         \___/
*                                          _|_
*                                          \ /
*                                           V
```

One good design method is the use area scaling and always match NPNs with NPNs and PNPs with PNPs. In this simulation, QN1 matches QN2 and QP1 matches QP2.

Given the 100 to 1 area ratios, current source I1 sets the DC AB bias current of the output transistors to be 100 times larger.





***#1==========WinSpiceVersion==========**

```
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*
*
*                                R2   100k
*                             _/\  /\  /\_____________________
*                            |   \/  \/                       |
*                            |                   VC ^           |
*                            |                     / \          |
*          R1 1K             |             _______ _|_         |
*     ___                    |            |  _|  |  _|'QN2     |
*   |IN |_/\  /\  /\_|INN|__|_|\ OUT1 |_|_|'QN1 |_|`-> 100X   |  ___
```

```
*   |___|   \/  \/   |___|     |  \_____|      |VEM     |______|_|OUT|_____
*    _|_                        |  /          <-        |      |___|     |
*   /VIN\    ^ VC   ^ VE      __|+/         _|'QP1     <-                 |
*   \___/   /_\    /_\       |__|/         |_|`_      _|'QP2 100X         |
*     |     _|_    _|_      _|_            |____|__|_|`_          RL  8   |
*    _|_   /VCC\  /VEE\    _///            |  VPB1      |       _/\  /\  /\__|
*    ///   \___/  \___/                     |_|_         _|_      |  \/  \/
*            |      |                      /_ _\        \ /    _|_
*           _|_    _|_                     \/_\/ I1    VE V    ///
*           ///    ///                     /\_/\
*                                          \___/
*                                           _|_
*                                           \ /
*                                            V
```

```
VCC     VC      0     DC     6
VEE     VE      0     DC     -6
VIN     IN      0     DC     0    SIN( 0 10m 5k 1n )
R1      IN      INN   1k
R2      INN     OUT   100k
RL      OUT     0     8
X_OPA   INN     0     OUT1    OP_AMP
QN2     VC      OUT1  OUT     NPNP 100
QP2     VE      VPB   OUT     PNPP 100
QN1     OUT1    OUT1  VEM     NPNP
QP1     VPB     VPB   VEM     PNPP
I1      VPB     0     7u

.tran    1u   .5m    0      1u


.control
run
set     pensize = 2
plot    out
plot    out  out1 vpb


alter  R1  resistance = 10000G
run
plot    -vcc#branch  ylimit 0 1m
.endc


.SUBCKT  OP_AMP INN   INP  OUT
EGBUF    VDIFF  0     INN  INP  1
RGM      VDIFF  VGND2 1k
CBW      OUT    VGND2 8p
EGOUT    OUT    0     VGND2 0    -100000000
.ENDS    OP_AMP
```

```
*                                 ____
*                        CBW _|____|          ____      .SUBCKT OP_AMP INN INP OUT
*                 VDIFF       ____   |_____|OUT|
*                          ___/\  ___|  _|_   |___|      ____     |\
*      ____|INN|__      _|_    \/___|_ /   \             |INN|__|  \
*      |___|_ /   \ RGM VGND |EGOUT|                      |___|      \
*             +|EGBUF|       __|      |                              OPA\_|OUT|
*              __|       |     \___/                                  /  |___|
*      ____|INP|__|  \___/        |   GAIN=-1M            ____|INP|__|  /
*      |___|        |  GAIN=1  ///  _|_                  |___|      /
*                  _|_                ///                            |/
*                  ///                     ODB = 20MHz
*
```

```
.model    NPNP   NPN(   BF=21000 )
.model    PNPP   PNP(   BF=21000 )

.end
```