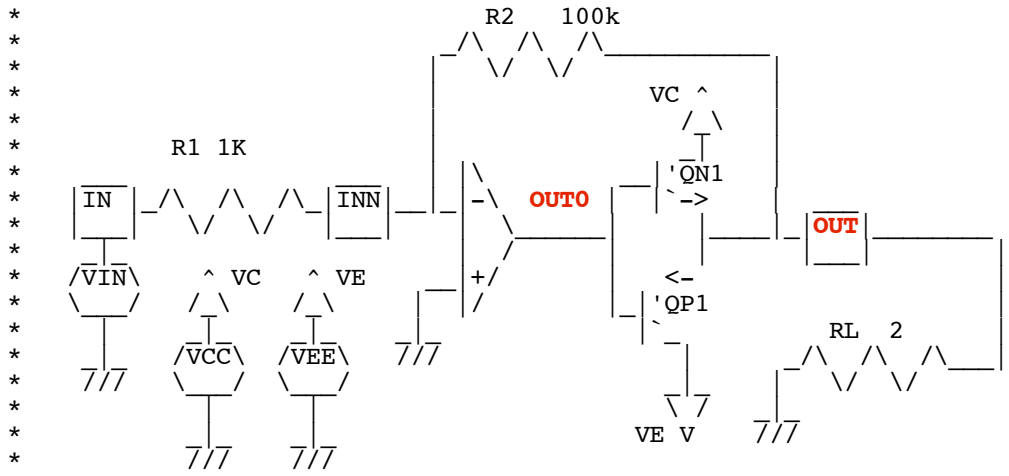
CROSSOVER_DISTORTION

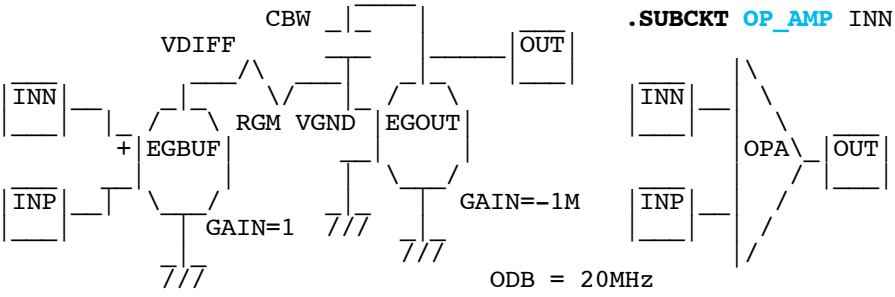
* dsauersanjose@aol.com 8/15/08
* www.idea2ic.com
*
*



*
*

```
VCC     VC      0     DC     6
VEE     VE      0     DC     -6
VIN     IN      0     DC     0    SIN( 0 10m 5k 1n )
R1      IN      INN   1k
R2      INN     OUT   100k
RL      OUT     0     8
X_OPA   INN     0     OUT0    OP_AMP
QN1     VC      OUT0  OUT     NPNP
QP1     VE      OUT0  OUT     PNPP

.tran    1u   .5m    0      1u

.control
run
set     pensize = 2
plot    out
plot    out  out0
.endc


.SUBCKT  OP_AMP INN   INP  OUT
EGBUF    VDIFF  0     INN  INP  1
RGM      VDIFF  VGND2 1k
CBW      OUT    VGND2 8p
EGOUT    OUT    0     VGND2 0    -100000000
.ENDS    OP_AMP
```

*



*

```
.SUBCKT OP_AMP INN INP OUT
```

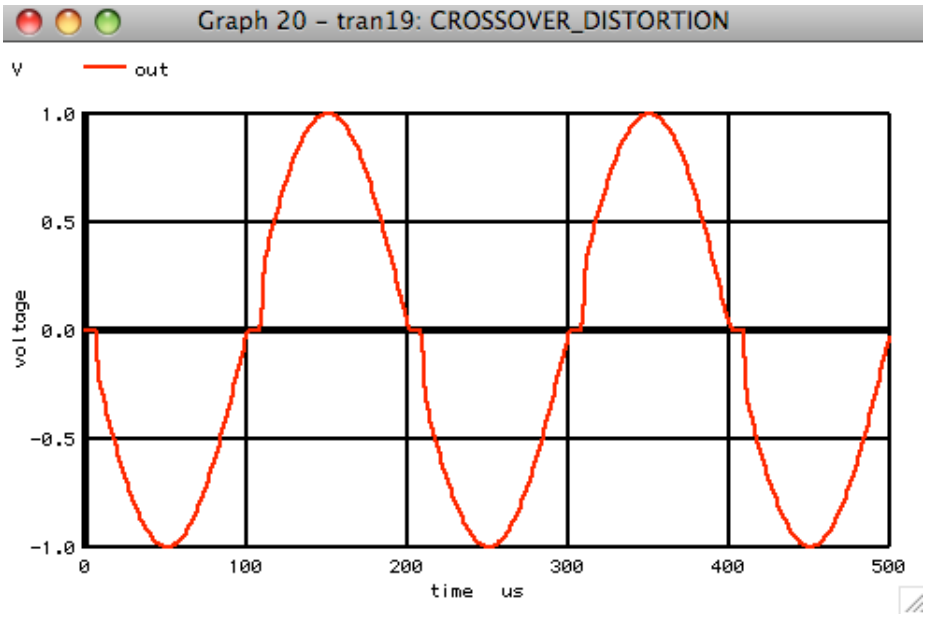


```
.model    NPNP   NPN(   BF=2100  )
.model    PNPP   PNP(   BF=2100  )
```

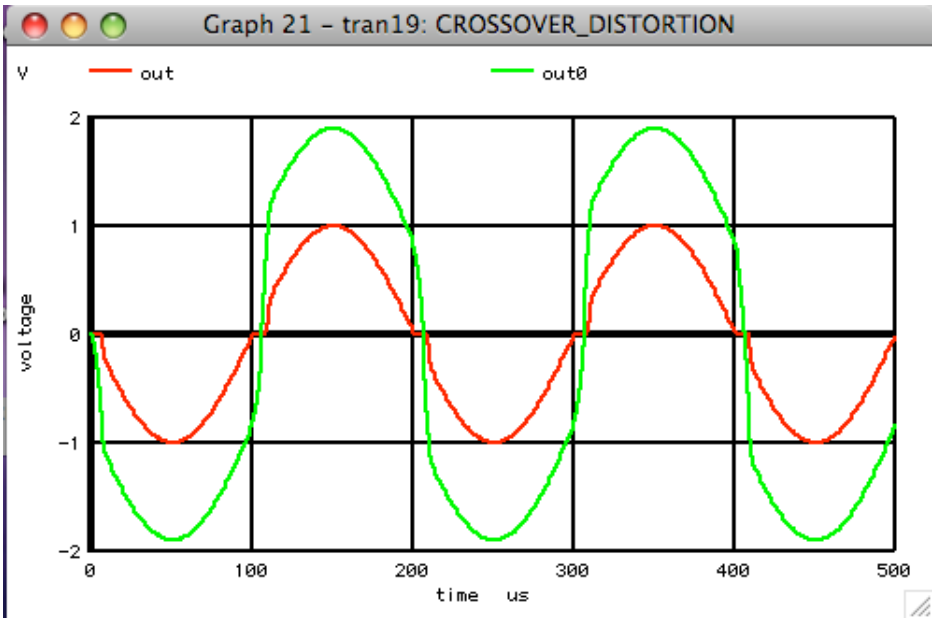
```
.end
```

```
======CrossOver_Distortion============
```

One common job in designing a power amplifier it choosing a level of AB bias for the output transistors.



The output transistors tend to be very large. The goal is to keep them on all the time while not wasting supply current.

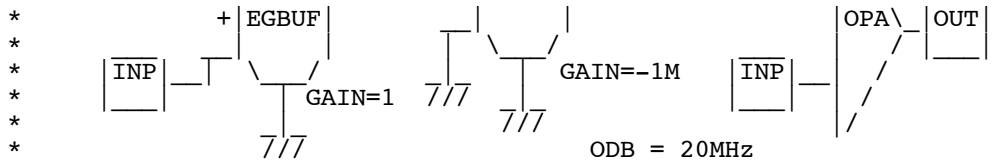


The above simulation is a really a "B" biased output stage. Both output transistors are never

on at the same time. Hence there is a period to time where both transistors are off and the power amplifier goes open loop at this time. The result usually shows up as glich in the output waveform.

***#1=============WinSpiceVersion=================**

```
CROSSOVER_DISTORTION
* dsauersanjose@aol.com  8/15/08
* www.idea2ic.com
*
*
*                               R2   100k
*                             _/\  /\  /\___________
*                            |   \/  \/             |
*                            |               VC ^   |
*                            |                 / \  |
*          R1 1K             |                 _|_  |
*    ___                ___  | |\           __|'QN1 |
*   |IN |_/\  /\  /\_|INN|__|_|-\  OUT0  |  |`->    |     ___
*   |___|   \/  \/   |___|     |  \______|     |____|_|OUT|________
*    _|_                       |  /      |                |___|    |
*   /VIN\    ^ VC   ^ VE     __|+/       |    <-                    |
*   \___/   / \    / \      |  |/        |_|'QP1                    |
*            _|_    _|_    _|_             |`_        RL  2         |
*    _|_   /VCC\  /VEE\   ///              |      _/\  /\  /\___|
*    ///   \___/  \___/                   _|_    |   \/  \/
*                                         \ /   _|_
*            _|_    _|_                VE V    ///
*            ///    ///
*
*

VCC      VC       0      DC      6
VEE      VE       0      DC      -6
VIN      IN       0      DC      0    SIN( 0 10m 5k 1n )
R1       IN       INN    1k
R2       INN      OUT    100k
RL       OUT      0      8
X_OPA    INN      0      OUT0     OP_AMP
QN1      VC       OUT0   OUT      NPNP
QP1      VE       OUT0   OUT      PNPP

.tran    1u   .5m    0      1u

.control
run
set     pensize = 2
plot    out
plot    out  out0
.endc


.SUBCKT  OP_AMP INN   INP  OUT
EGBUF    VDIFF  0     INN  INP  1
RGM      VDIFF  VGND2 1k
CBW      OUT    VGND2 8p
EGOUT    OUT    0     VGND2 0    -100000000
.ENDS    OP_AMP

*
*                       CBW _|_____                .SUBCKT OP_AMP INN INP OUT
*                VDIFF      ___    |_____|OUT|
*                     ___/\ ___|  _|_    |___|          |\
*     |INN|__   _|_    \/    |_ / \                |INN|__| \
*     |___|  |_ /   \ RGM VGND |EGOUT|             |___|  |  \   ___
```




```
.model    NPNP   NPN(   BF=2100 )
.model    PNPP   PNP(   BF=2100 )

.end
```