Bottom_Side_Fuzzy

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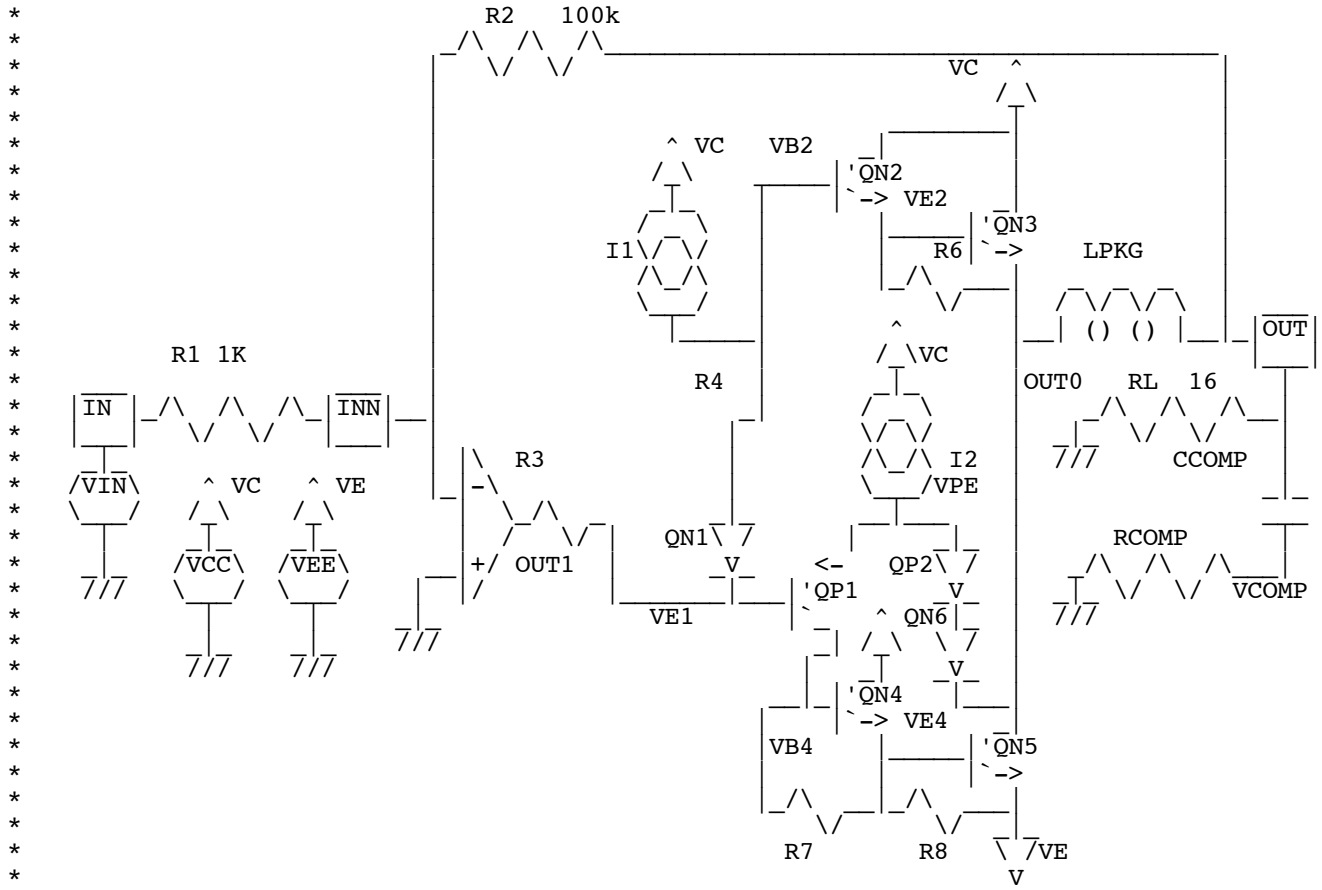
* www.idea2ic.com




```
.OPTIONS  GMIN=1e-15 METHOD=gear ABSTOL=1e-15 temp=27

VCC     VC      0     DC      8
VEE     VE      0     DC      -7
VIN     IN      0     DC      0    SIN( 0 50m 10k 1n )
R1      IN      INN   1k
R2      INN     OUT   100k
X_OPA   INN     0     OUT1    OP_AMP
R3      OUT1    VE1   10
QN1     VB2     VB2   VE1     NPNP 90
I1      VC      VB2   200u
QN2     VC      VB2   VE2     NPNP 5
QN3     VC      VE2   OUT0    NPNP 100
R6      VE2     OUT   20k
I2      VC      VPE   1m
QP1     VB4     VE1   VPE     PNPP 1
QP2     VPB2    VPB2  VPE     PNPP 10
QN6     VPB2    VPB2  OUT0    NPNP 10
QN4     VC      VB4   VE4     NPNP 10
QN5     OUT0    VE4   VE      NPNP 200
R7      VB4     VE4   100k
R8      VE4     VE    20k
LPKG    OUT0    OUT   10n
RL      OUT     0     16
CCOMP   OUT     VCOMP .1u
RCOMP   VCOMP   0     1
.tran    10n   .2m    0      10n

.control
run
set     pensize = 1
plot    out out1 vb4 ve  title With_Comp
```

```
alter   CCOMP  capacitance = 1p
run
set       pensize = 1
plot      out out1 vb4 ve  title WithOut_Comp


.endc


.SUBCKT  OP_AMP INN    INP  OUT
EGBUF    VDIFF  0      INN  INP   1
RGM1     VDIFF  VDIFF2 1k
RGM2     VDIFF2 VGND2  1k
CBW      OUT    VGND2  4p
CSP      VDIFF2 0      4f
EGOUT    OUT    0      VGND2 0    -100000000
.ENDS    OP_AMP

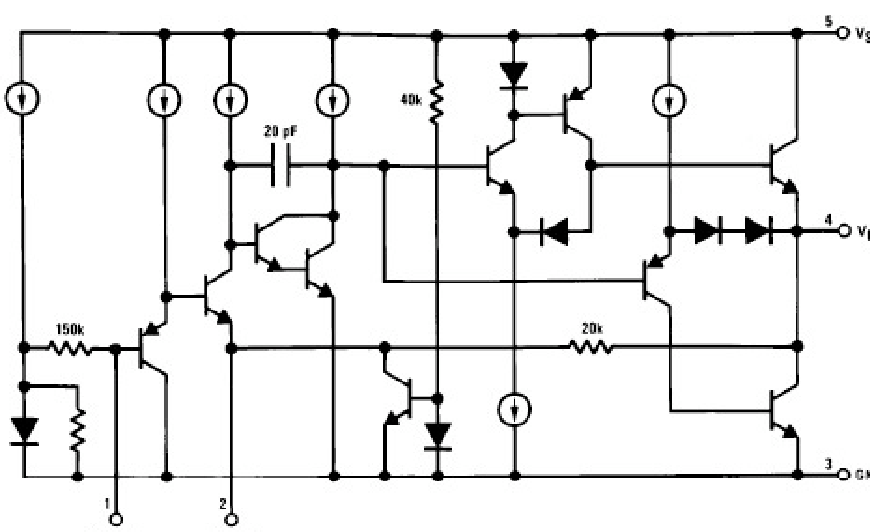
*
*                      CBW _|___  |                .SUBCKT OP_AMP INN INP OUT
*               VDIFF      _  _   |______|OUT|
*                     ___/\  ___|    _|_              |\
*     |INN|__     _|_     \/    |_  /   \        |INN|__|  \
*     |___|  |_  /   \ RGM VGND |EGOUT|         |___|  |   \
*             +|EGBUF|        __|     |              |OPA\_|OUT|
*            __|     |         |   \___/               |    /  |___|
*     |INP|__|   \___/        _|_   _|_  GAIN=-1M  |INP|__|  /
*     |___|          |  GAIN=1 ///  _|_             |___|  | /
*                   _|_              ///                   |/
*                   ///                        ODB = 20MHz
*
.model     NPNP    NPN( BF=210 IS=1e-17    )

.model     PNPP    PNP(   BF=10    IS=1e-17 IKF=7.6e-06  ITF=1.70E-6
+ CJE= 4e-12      CJC=1.826E-12   CJS=1.826E-12
+ TF=.03e-6   PTF=205      )

.end
```

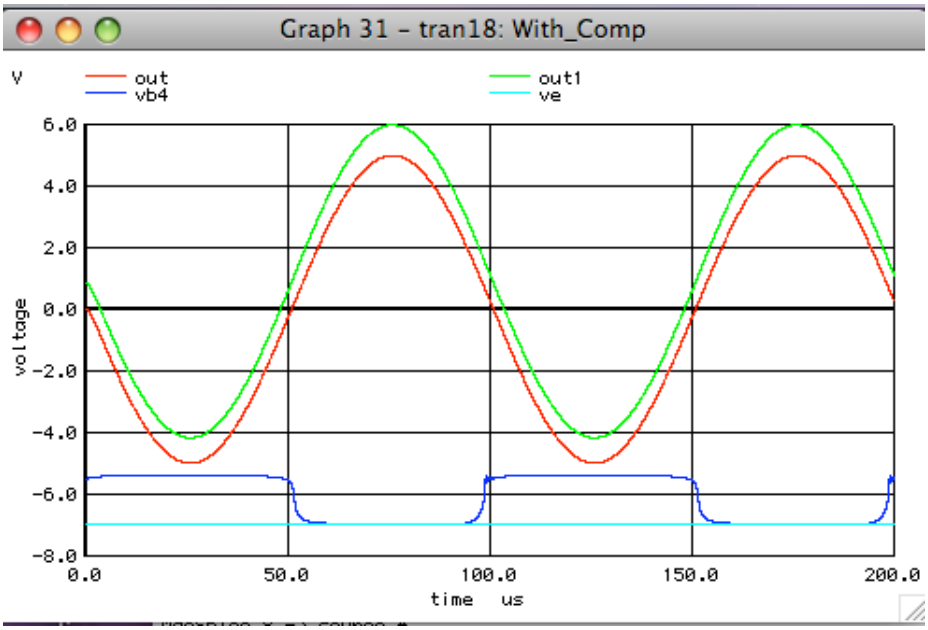
======**Bottom_Side_Fuzzy**=============

Equivalent Schematic

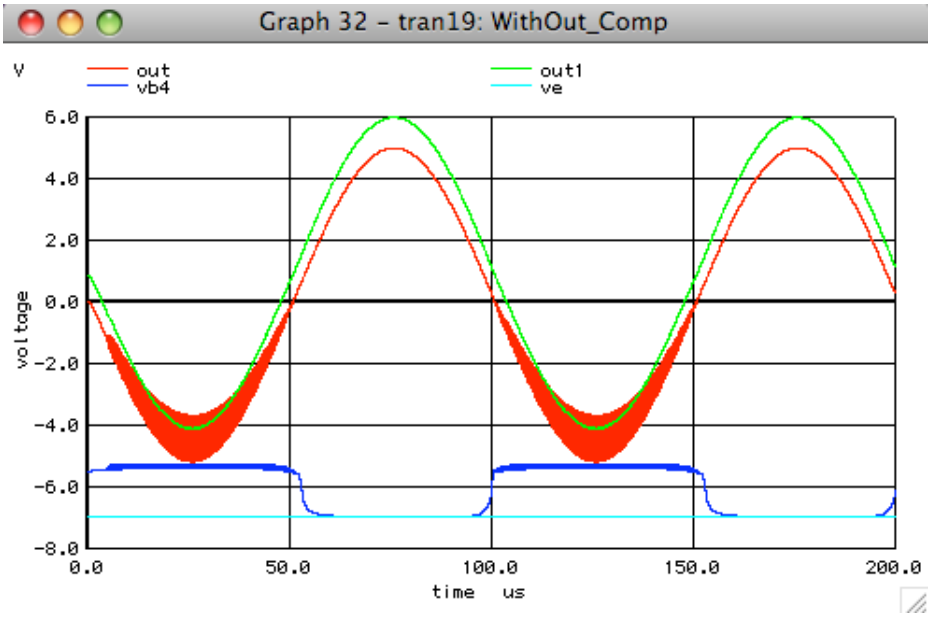


At the time that LM383 was designed, the only available PNPs were lateral and had an ftau

around a few MegHz. They also could put out much less current. In order to have an big enough NPN output transistor be able to pull the output almost to ground at 5 amps, one of these lateral PNPs needs to be put in a loop similiar to what is shown in the LM383's equvalent schematic shown above.



It had been common practice to stablize such an output stage by connecting a capacitor and small resistor to from the output to ground. The plot above shows the output with the stablity compensation network in place.



For comparison sake, the plot above is without

the stablity compensation network. In this simulation, transistors QN2 and QN3 are AB biased with the bottom side pnp composite. The NPN darlington attempts to stabilize the pnp composite but is less and less able to do so as the QN5 is required to produce more output current. The lower the output voltage swings, the more QN5 turns on and QN3 turns off resulting in more instability. This was commonly referred to at that time as "the Bottom Side Fuzzies".

***#1=============WinSpiceVersion=================**

```
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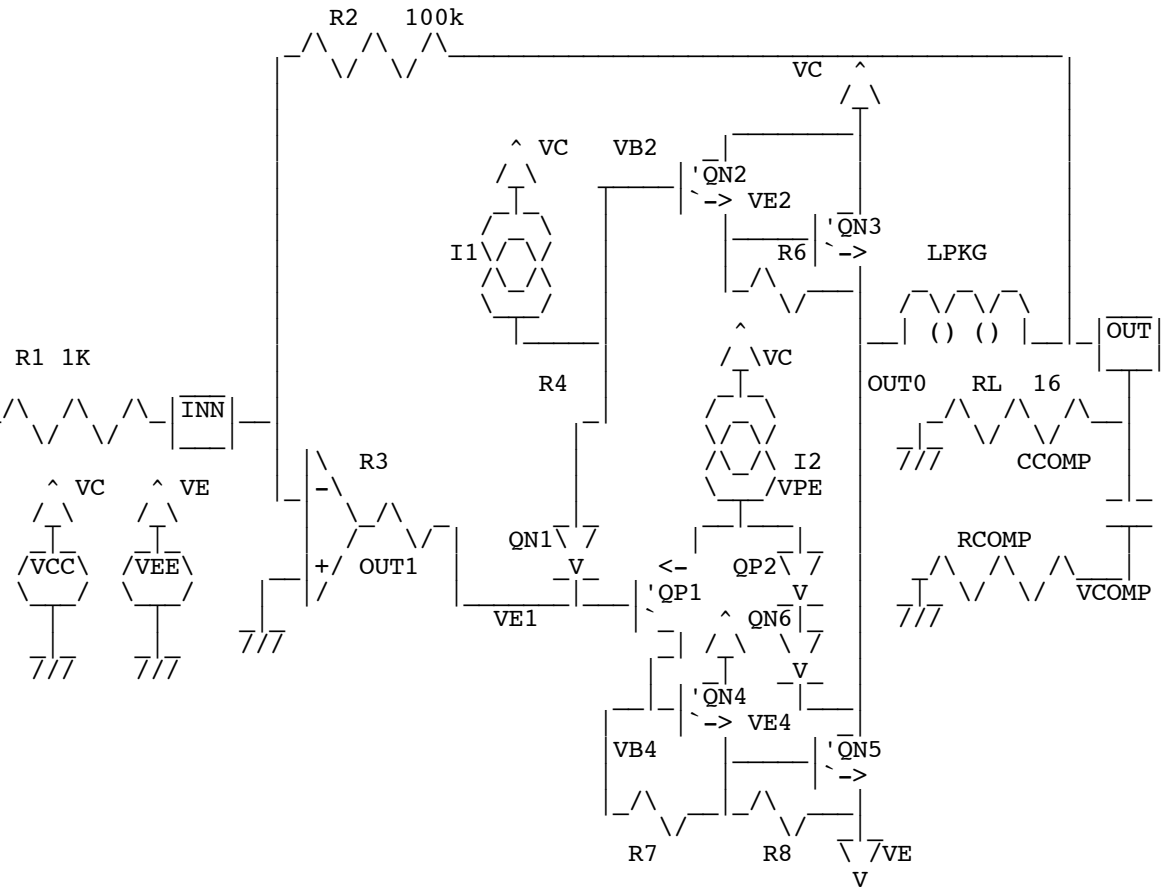
```

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R2      INN     OUT   100k
X_OPA   INN     0     OUT1    OP_AMP
R3      OUT1    VE1   10
QN1     VB2     VB2   VE1     NPNP 90
I1      VC      VB2   200u
QN2     VC      VB2   VE2     NPNP 5
QN3     VC      VE2   OUT0    NPNP 100
R6      VE2     OUT   20k
I2      VC      VPE   1m
```

```
QP1      VB4      VE1   VPE      PNPP 1
QP2      VPB2     VPB2  VPE      PNPP 10
QN6      VPB2     VPB2  OUT0     NPNP 10
QN4      VC       VB4   VE4      NPNP 10
QN5      OUT0     VE4   VE       NPNP 200
R7       VB4      VE4   100k
R8       VE4      VE    20k
LPKG     OUT0     OUT   10n
RL       OUT      0     16
CCOMP    OUT      VCOMP .1u
RCOMP    VCOMP    0     1
.tran     10n   .2m    0      10n

.control
run
set      pensize = 1
plot     out out1 vb4 ve  title With_Comp

alter  CCOMP  capacitance = 1p
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set      pensize = 1
plot     out out1 vb4 ve  title WithOut_Comp


.endc


.SUBCKT  OP_AMP INN    INP  OUT
EGBUF    VDIFF  0     INN  INP  1
RGM1     VDIFF  VDIFF2 1k
RGM2     VDIFF2 VGND2  1k
CBW      OUT    VGND2  4p
CSP      VDIFF2 0      4f
EGOUT    OUT    0     VGND2 0    -100000000
.ENDS    OP_AMP

*
*                       CBW _|_____|              .SUBCKT OP_AMP INN INP OUT
*                VDIFF      ___    |_____|OUT|
*                    ___/\   __|_  _|_  |___|          |\
*     |INN|__     _|_   \/   |_ / \             |INN|__| \
*     |___|  |_  /   \ RGM VGND |EGOUT|          |___|  |  \
*             +|EGBUF|       __|     |                 |OPA\_|OUT|
*           __|      |         | \___/                 |   / |___|
*     |INP|__|  \___/         _|_  |  GAIN=-1M   |INP|__|  /
*     |___|       |GAIN=1   ///  _|_             |___|  | /
*                _|_             ///                    |/
*                ///                    ODB = 20MHz
*
.model    NPNP   NPN( BF=210 IS=1e-17   )

.model    PNPP   PNP(   BF=10   IS=1e-17 IKF=7.6e-06  ITF=1.70E-6
+ CJE= 4e-12     CJC=1.826E-12   CJS=1.826E-12
+ TF=.03e-6  PTF=205     )

.end
```