High-Frequency CMOS Switched-Capacitor Filters for Communications Application

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Abstract — **Bandpass filters for communications applications are realized using an 80 MHz differential single-stage CMOS op amp and a fully differential identical-resonator elliptic bandpass ladder filter configuration. Experimental results are given from a CMOS sixth-order 260 kHz elliptic bandpass filter with a Q of 40 clock frequency of 4 MHz, and a power dissipation of 70 mW.**

I. Introduction

In the past several years, monolithic switched-capacitor filters have been widely applied in the area of commercial communication circuits. These filters can be very accurate since their frequency response depends on capacitor ratios. They are also compatible with current MOS technologies, thus they are useful as interfacing circuits for digital systems [1], [2]. To date, most switched-capacitor filter applications have been limited to the audio range, examples being codec filters for PCM telephony [3]–[6] and filters for speech recognition systems [7]. However, communication systems require filtering above the voiceband. Examples are AM and FM intermediate frequency filtering in radio receivers, TV video processing, channel filters in FDM telephony systems, and filters for data communications. Presently, these filtering functions are realized by passive LC, crystal, or ceramic filters. The extension of switched-capacitor techniques into the several hundred kHz to MHz range would allow the elimination of many of these external components, so that systems, such as communication receivers, could be more fully integrated than is possible now.

This paper describes a design approach for the realization of high-frequency switched-capacitor filters in CMOS technology. While many of the concepts described here could be applied in NMOS technology as well [11], our work focused on CMOS both because of the fundamental advantages in the implementation of high-speed operational amplifiers, and because CMOS is likely to be desirable for other reasons in implementing the highly integrated single-chip subsystems and systems in which these filters would likely be applied.

In Section II, factors limiting the performance of switched-capacitor filters at high frequencies are explored, and design techniques proposed which allow a closer approach to the fundamental limits on achievable performance are examined. In Section III, the design of a fully differential, folded cascode CMOS operational amplifier used in the filters is described. Last, in Section IV, experimental results are given for a 260 kHz high-Q bandpass intended for AM IF filtering applications. In the final section conclusions are reached.

II. Design Techniques for High-Frequency, High-Q Bandpass Filters

A. Introduction

The extension of the range of application of switched-capacitor filters to higher frequencies involves a number of problems, some associated with the high clock rates and resulting severe requirements on operational amplifier settling time, and another set of problems relating to the fact that most of the applications of these filters involve highly selective (high-Q) filter responses. The latter constraint leads to sensitivity problems because of the inherently increased sensitivity of high-Q filters both to the ratios of the capacitors in the filter as well as to the gain and settling behavior of the operational amplifiers. In addition, narrow-band filters require large capacitors ratios, which further aggravate the problems of accuracy and amplifier speed.

Another difficulty arises in the use of elliptic bandpass filters, which are more efficient in realizing the sharp roll-off characteristic often required in high-Q communication filters. The realization of elliptic bandpass filters in active ladder configuration can give rise to unstable dc conditions [2], thus driving the operational amplifier into

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saturation. The successful implementation of high-frequency high-Q filters requires an effective approach which alleviates these problems.

Several authors have explored the use of N-path or pseudo N-path filtering techniques for high-Q filtering [12]–[15]. In the N-path filtering technique, the signal is translated from its initial center frequency to a range centered about zero frequency, low-pass filtered, and then retranslated back up to the original center frequency. In order that all spurious quadrature components introduced by the modulation cancel out, multiple paths are required which are spaced equally in the phase of the modulating signals. The great advantage of this technique is that the center frequency is determined precisely by an externally supplied clock, with no dependence on capacitor ratios, and that the actual filter itself is a low-pass operating at a frequency much lower than the center frequency. The disadvantages are that the modulating signal is at the filter center frequency where carrier feedthrough in the modulators will directly degrade the dynamic range of the filter, that the parallel paths must match to a high degree of accuracy, and that parasitic passbands exist starting at a frequency twice the passband frequency. It appears likely that this type of filter will find wide application in extremely high-Q applications where extreme accuracy of center frequency is paramount, and the more conventional filtering approaches are likely to be used where the required Q is more moderate and dynamic range is paramount. However, because of the wide dynamic range often required in communication filters, we chose a more conventional filtering architecture for this work.

B. Fully Differential Filter Implementation

Since the settling time of the operational amplifier places an upper limit on the allowable clock rate, the operating frequency of a switched-capacitor filter is primarily limited by the transient performance of the operational amplifier. Hence, the selection of an operational amplifier implementation which realizes the required settling time while still achieving sufficient dc gain is perhaps the most important consideration in the implementation of high-frequency filters. Another consideration affecting the choice of operational amplifier configuration is the fact that the effect of charge injection into the signal path from the switch transistors becomes much more important as the clock frequency is increased. This occurs because the switches themselves must be larger so as to minimize the charging time constant, thus increasing the charge injection. This larger clock feedthrough can degrade the effective settling time of the amplifier, degrade the power supply rejection if the clock voltage is dependent on a supply, and give rise to large dc offsets in the filter.

The power supply rejection ratio (PSRR) of the amplifier is particularly important in high-frequency high-Q filters since power supply variations can be coupled to some internal nodes of the operational amplifier and will eventually appear at the output. Because high-Q filters typically take the form of an array of resonators which are weakly coupled to each other, parasitic coupling paths through the power supply can have a strong effect on the response even if they are small in magnitude.

These considerations point strongly to the use of fully differential signal paths and a differential output operational amplifier. The use of differential techniques has been described earlier for voiceband filters [10]. Because it is fully differential, clock noise and power supply variations appear as common mode signals, and therefore will not affect filter response. An additional advantage in the high-frequency case is that the differential-to-single-ended conversion normally required within single-ended operational amplifiers is avoided, thereby improving the bandwidth of the amplifier. The design of such a differential high-speed CMOS amplifier is considered in detail in Section III.

C. Sensitivity in High-Q Bandpass Ladder Filters

As mentioned earlier, most applications in high-frequency communication systems require narrow-band filters ($Q \sim 40$), with a rather tight tolerance in the center frequency accuracy. Compared with voiceband codec filters, these narrow-band filters have pole locations much closer to the $j\omega$ axis. Typical codec filters are 5-pole, 4-zero low-pass filters, with the largest pole Q approximately equal to 3, whereas a sixth-order elliptic bandpass filter with a Q of 40 has individual pole Q's on the order of 100. This means that small variations in the pole locations can cause significant variations in the passband response, and may give rise to a large passband ripple or instability in the worst case. Also, since the filters have narrow bandwidths, a small shift in the center frequency can move the passband outside the frequencies of interest; hence, the filter design must be able to realize a stable center frequency.

To understand more about the sensitivity problem, let us consider a fourth-order all-pole bandpass filter in more detail. A leapfrog realization of the doubly-terminated LC filter in Fig. 1(a) has the signal flowgraph shown in Fig. 1(b). This is typical of leapfrog bandpass structures. The paths denoted by "$1/s\tau_i$" are the integrators, so that a resonator is formed when two such integrators are connected back to back. For this fourth-order filter, there are two resonators coupled together by the coupling paths "a" and "b." Also, "k_1," "k_2" are the termination paths which realize the source and load resistances. Each resonator resonates at a frequency equal to the center frequency of the filter, so that the filter center frequency is only a function of the resonator capacitor ratios and is independent of the coupling capacitor ratios. If we calculate the incremental sensitivity of the transfer function $T(s)$ of this filter, it can be shown that at the passband edge [16]

$$|S_{\tau_i}^{|T|}| \sim Q \qquad \text{where } i = 1,2,3,4 \tag{1}$$

$$|S_x^{|T|}| \sim 1 \qquad \text{where } x = a, b, k_1, k_2. \tag{2}$$

In other words, at the passband edges, the magnitude of the frequency response is about Q times more sensitive to

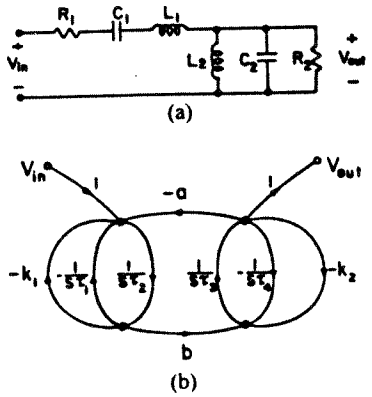


Fig. 1. (a) Fourth-order *LC* bandpass ladder. (b) Signal flowgraph of fourth-order *LC* bandpass ladder.

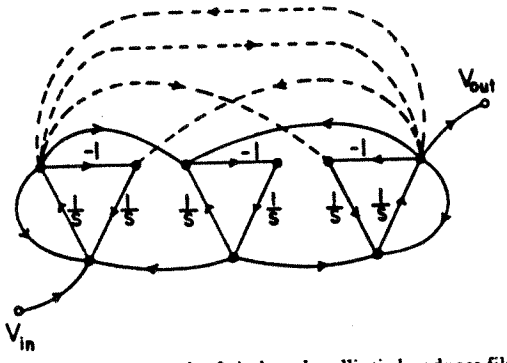


Fig. 2. Signal flowgraph of sixth-order elliptic bandpass filter.

the integrator capacitor ratio than the coupling capacitor ratio.

The significance of this is that the filter should be implemented in such a way that the resonators within the filter have center frequencies which match as closely as possible over all conditions of process variations, temperature variation, supply voltage variation, and so forth. For example, a 0.5 percent variation of all of the resonator center frequencies in the same direction would simply shift the overall response by 0.5 percent without altering its shape. However, a change of frequencies while the others remain constant would grossly distort the passband shape of a filter with an effective Q of, for example, 50.

One approach to achieving a high degree of resonator center frequency matching is to make them identical by making all the individual integrators identical, thus each integrator will have an integrating time constant equal to the reciprocal of the center frequency (in radians). In a switched-capacitor integrator, the integrator time constant τ is defined as

$$\tau = \frac{C_I}{f_s C_S} \tag{3}$$

where C_S is the sampling capacitor, C_I is the integrating capacitor, and f_s is the sample rate. If all the integrators are made identical with a time constant given by the center frequency f_o, then

$$\frac{1}{2\pi f_o} = \frac{C_I}{f_s C_S} \tag{4}$$

or

$$\frac{C_I}{C_S} = \frac{f_s}{2\pi f_o}. \tag{5}$$

Even if the clock rate to center frequency ratio is 20,

$$\frac{C_I}{C_S} \approx 3. \tag{6}$$

With this scheme of identical resonators, all the integrators have the same capacitor ratio, and hence all the integrator time constants track each other. This is important because f_o is now only a function of one particular capacitor ratio. This ratio is small (6); hence the minimum size capacitor can be on the order of 1 pF without jeopardizing the operational amplifier settling time. With this kind of capacitor size, accuracy of better than half a percent can be easily achieved, and this is more than enough for most center frequency accuracy requirements.

Another obvious advantage of using this scheme is that it greatly simplifies the layout since all integrators are identical. Nevertheless, there is a disadvantage with this method. With identical resonators, the operational amplifier voltage swings are not properly scaled to have equal maxima, resulting in a reduction of dynamic range. In a narrow-band filter with Q on the order of 40, there is a loss of about 6 dB in dynamic range.

D. Component Spreads in High-Q Active Ladder Bandpass Filters

In addition to the sensitivity problem, the fact that high-frequency filters have high Q's also give rise to large spreads in the required capacitor ratios. This stems fundamentally from the fact that the energy stored in the resonator is much larger than the energy transferred into or out of it each cycle. Consider a sixth-order elliptic bandpass filter with a signal flowgraph shown in Fig. 2—the couplings between the resonators have capacitor ratios determined by the Q of the filter as well as the nature of the band edges. Typically, a high Q or a sharp roll off would mean a large ratio. A Q of 40 in this sixth-order elliptic bandpass would require capacitor ratios on the order of 100. In order to maintain adequate ratio accuracy, the minimum size capacitor cannot be too small (≥ 0.1 pF), and thus the large ratios would require large capacitors which in turn slow down the amplifier response.

There are two kinds of coupling paths between the resonators. A realization of the signal flowgraph in Fig. 2 using switched capacitor integrators is shown in Fig. 3. Here single-ended operational amplifiers are used, but the following analysis is true for fully differential operational amplifiers as well. It is seen that the coupling paths which feed into the outputs of integrators can be realized by feedforward capacitors, whereas those which feed into the

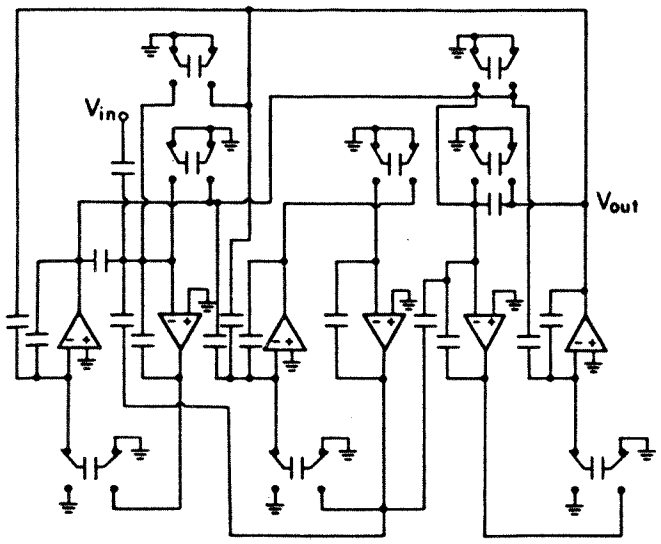


Fig. 3. Six operational amplifier realizations of sixth-order elliptic band-pass filters.

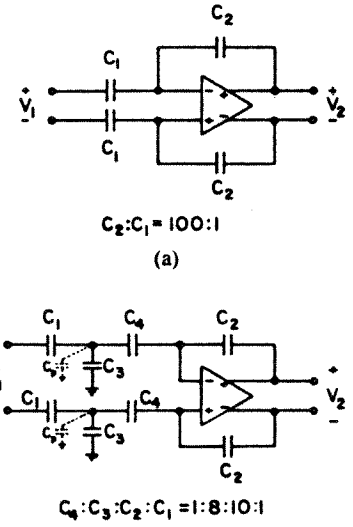


Fig. 4. (a) Direct realization of a gain of 0.01. (b) T-network scheme to realize a gain of 0.01.

inputs of integrators have to be realized via sampling capacitors. For the feedforward capacitors, a T-network scheme can be used to reduce the large coupling ratios required. A straightforward realization of a gain of 0.01 is shown in Fig. 4(a). Here, the gain of the circuit is given by

$$\frac{V_2(s)}{V_1(s)} = -\frac{C_1}{C_2} \tag{7}$$

and the ratio $C_2 : C_1$ is equal to 100:1. A T-network scheme used to realize a similar gain of 0.01 is shown in Fig. 4(b). Here, the transfer function of the circuit is given by

$$\frac{V_2(s)}{V_1(s)} = -\frac{C_1}{C_1 + C_3 + C_4} \cdot \frac{C_4}{C_2}. \tag{8}$$

The ratio $C_2 : C_3 : C_1 : C_4$ is equal to 10:8:1:1 for the same

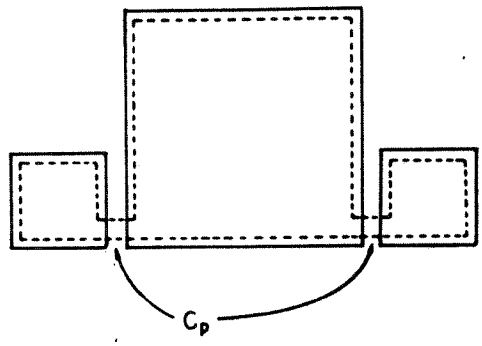


Fig. 5. T-network layout strategy to minimize capacitances.

gain of 0.01. Thus, a maximum capacitor ratio of 100 is reduced to 10 by this method.

The circuit in Fig. 4(b) is sensitive to parasitic capacitors C_p at the center node of the T-network. However, this capacitance can be reduced to a negligible amount by means of proper layout. Fig. 5 shows such a layout of the T-network. Here, the solid lines are the thin-oxide regions, and the dashed lines are the polysilicon of the capacitors (polysilicon to substrate capacitors are assumed). The polysilicon forms the center node of the T-network. Thus, parasitic capacitance C_p consists of only 2 squares of minimum feature size over the field oxide. For the case of Fig. 4(b), if the minimum size capacitors (C_1 and C_4) are equal to 0.1 pF, then C_3 is equal to 0.8 pF. Assuming a 4×4 μm minimum feature over a 0.8 μm field oxide, C_p is approximately equal to 1.4 fF. This C_p adds to C_3, the biggest capacitor of the T-network and 1.4 fF amounts to less than 0.2 percent of 0.8 pF. Hence, the parasitic capacitances are entirely negligible.

This T-network scheme is not applicable towards the coupling paths realized via sampling capacitors because of the additional switching involved and the added clock noise. Thus, it is desirable to convert this type of coupling to feedforward capacitors. This is done by redirecting the signal paths which go into an integrator input to the output of the other integrator of the same resonator. This is shown in Fig. 6(a) and (b). Here, the signal path α which feeds into the input of an integrator in Fig. 6(a) is redirected as shown in Fig. 6(b). However, this integrator output may feed other parts of the circuit as well. Hence, an equal amount of the signal has to be subtracted from those nodes fed by this output. In Fig. 6(b), this is shown by the signal path $\alpha\beta$. Using this method, the signal flowgraph in Fig. 2 can be redrawn in Fig. 7(a). It should be noted that Fig. 7(a) has been simplified by ignoring signal paths which represent a gain factor of 10^{-4} or less of an operational amplifier output. The corresponding switched-capacitor circuit for this flowgraph is shown in Fig. 7(b). Here, fully differential operational amplifiers are used. This circuit has 7 operational amplifiers instead of 6 because the filter output node has been modified and a signal has to be subtracted from it to regain the proper output. An extra operational amplifier is therefore needed to do the subtraction. In this circuit, all the coupling paths are now realized

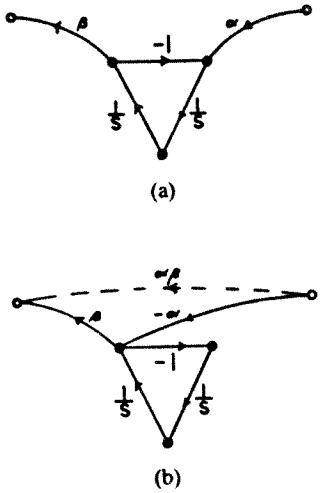


Fig. 6. Conversion of coupling paths via sampling capacitors to coupling paths via feedforward capacitors. (a) Original signal flow diagram. (b) Signal flow diagram after conversion.

by feedforward capacitors, and thus T-networks are applicable for reducing the capacitor ratios.

One drawback of the use of continuous coupling paths, such as those represented by T-networks, is the fact that the settling time behavior of the operational amplifiers within the filter is more complex than before, since continuous time paths exist which link the output voltage of one amplifier to the summing node of another during the settling interval. Fortunately, in the case of high-Q filters, the coupling path between operational amplifiers is sufficiently weak that the loop gain around any continuous-path loop is small compared to unity. Under these conditions, it can be shown that the settling time to a given accuracy is lengthened by a factor on the order of two for operational amplifiers whose inputs and outputs are interconnected by continuous time paths.

E. DC Stability in Elliptic Bandpass Active Ladder Filters

Elliptic bandpass filters are very useful in realizing narrow-band filters because of the higher selectivity at the band edges obtained from the transmission zeros. However, implementation of elliptic bandpass filters in the leapfrog configuration can result in unstable dc conditions in the circuit [2]. This problem arises from the presence of inductor loops in the LC ladder (capacitor loops may have similar problems), and is not unique to switched-capacitor filters. To see this, consider the circuits in Fig. 8, where an RC integrator is used to simulate the $I-V$ characteristics of an inductor. Here, active RC integrators are used for demonstration purposes, the same reasoning applied to switched-capacitor integrators. Assuming the operational amplifier is ideal, the transfer function of the integrator is given by

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = -\frac{1}{sRC}. \tag{9}$$

The $I-V$ characteristic of an inductor is given by

$$\frac{I(s)}{V(s)} = \frac{1}{sL}. \tag{10}$$

If $I(s)$ is resistively scaled to $V'(s)$, then

$$\frac{V'(s)}{V(s)} = \frac{I(s)R'}{V(s)} = \frac{R'}{sL} \tag{11}$$

where R' is the scaling resistance. Equations (9) and (11) show that, with an ideal operational amplifier, an inductor can be exactly simulated by an active RC integrator, where the RC time constant is related to L by

$$RC = \frac{L}{R'}. \tag{12}$$

The minus sign in (9) is not important since the inductor current can be defined with a different orientation.

If there is an offset voltage V_{os} in the operational amplifier [Fig. 8(a)], then

$$\frac{V_{\text{in}}(s) - V_{os}}{R} = sC(V_{os} - V_{\text{out}}(s)) \tag{13}$$

or

$$V_{\text{out}}(s) = -\frac{V_{\text{in}}(s) - V_{os}}{sRC} + V_{os}. \tag{14}$$

This relationship can be represented by the circuit in Fig. 8(b). If the small offset voltage at the output is ignored, then

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s) - V_{os}} \approx -\frac{1}{sRC}. \tag{15}$$

Comparing (15) with (11), this would mean that instead of $V(s)$, $(V(s) - V_{os})$ is being integrated. Hence, in addition to simulating an inductor, there is a small voltage source in series which is equal to the offset voltage of the operational amplifier [Fig. 8(c)]. If such integrators are used to implement an inductor loop as in Fig. 9(a), it will result in the circuit in Fig. 9(b) where there are offset voltage sources in series with the inductors. Since it is very likely that these offsets do not add up to zero, they will cause infinite current in the inductors. In terms of the active equivalent circuit, there will be an operational amplifier driven by a voltage equal to $A(\Sigma_i V_{os})$, where A is the operational amplifier gain. Hence, if the offset voltages do not sum up to zero, then the operational amplifier will be driven into saturation.

The same problem can be analyzed in the context of the active filter. Consider the inductor loop in Fig. 10(a), with inductor voltages and currents defined as shown. This can be part of a doubly-terminated LC ladder. The signal flowgraph representing their $I-V$ characteristic is shown in Fig. 10(b). This is realized by active RC integrators as shown in Fig. 10(c), where V_i's are the integrator inputs, and V_o's are the operational amplifier outputs. Consider the dc condition of the circuit. In order to keep the output

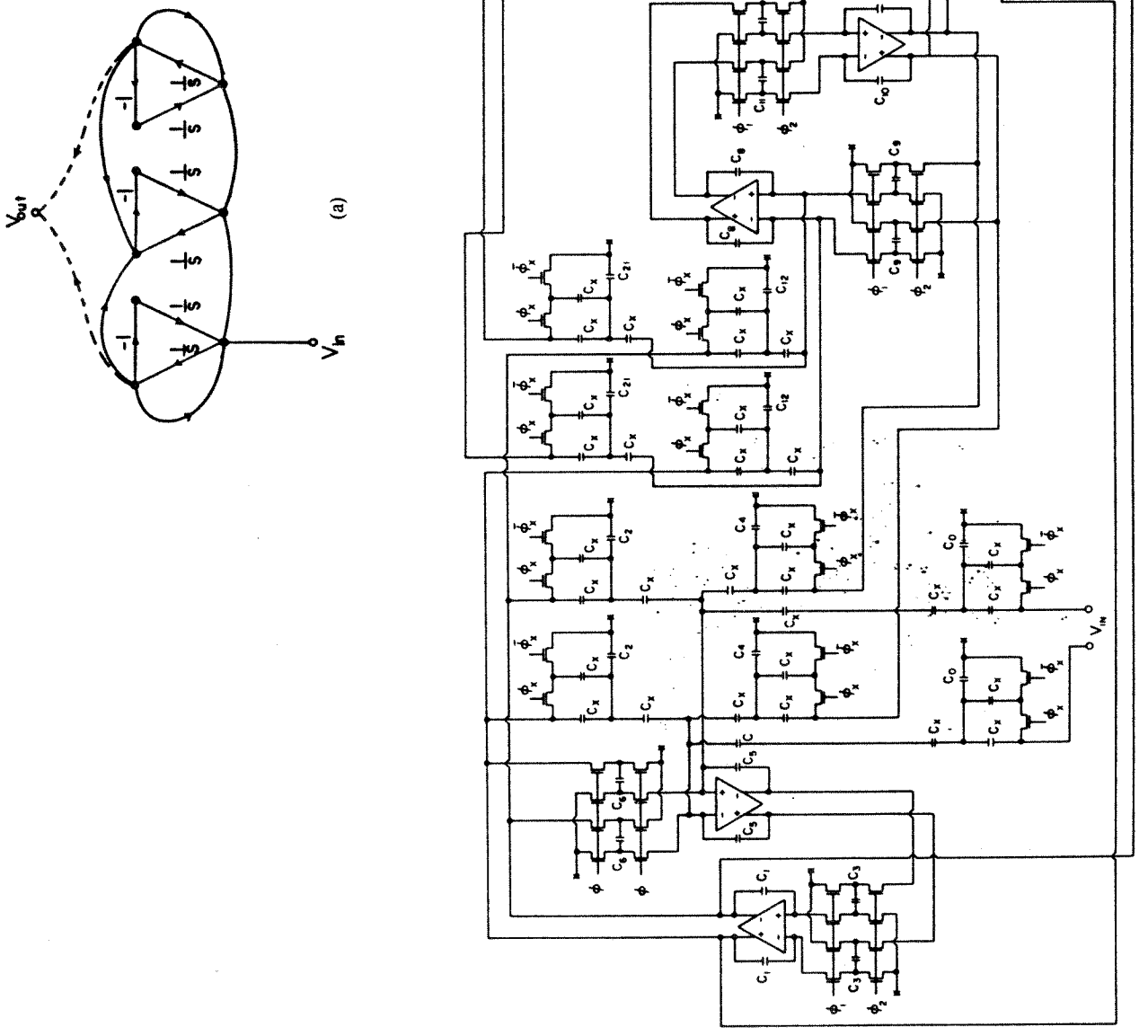


Fig. 7. (a) Signal flowgraph for sixth-order elliptic bandpass filter after converting coupling paths via sampling capacitors to coupling paths via feed-forward capacitors. (b) Seven operational amplifier realizations of sixth-order elliptic bandpass filters.

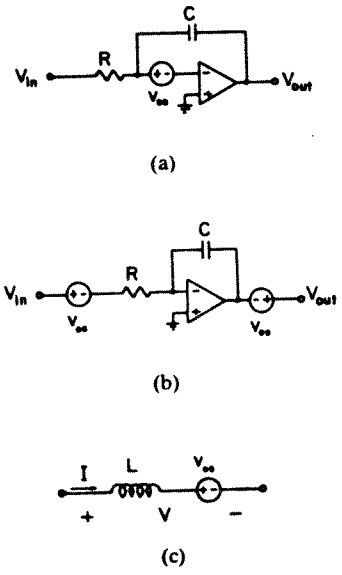


Fig. 8. (a) An active *RC* integrator with offset voltage in the operational amplifier. (b) Equivalent circuit of Fig. 8(a). (c) Effect of operational amplifier offset voltage in the simulated inductor.

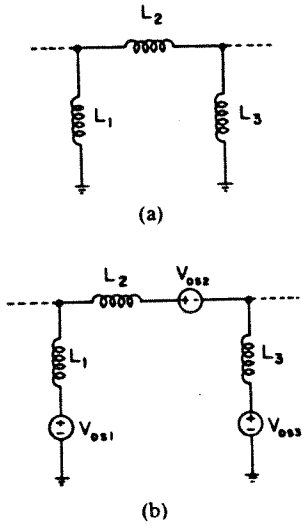


Fig. 9. (a) An inductor loop. (b) An inductor loop simulated by active *RC* integrators with operational amplifier offset voltages.

voltage V_{o1} in active region, its input voltage is given by

$$V_{i1} \approx V_{os1} \tag{16}$$

where V_{os1} is the offset voltage in the first operational amplifier. Likewise,

$$V_{i3} \approx V_{os3}. \tag{17}$$

Then

$$V_{o2} = -A_2(V_{os1} + V_{os2} + V_{os3}) \tag{18}$$

where A_2 is the gain of the second operational amplifier. If the offset voltages of the three operational amplifiers do not add up to zero, then V_{o2} will be driven into saturation.

To solve this problem, the *LC* loops in the passive filter can be broken up by Thevenin equivalent circuits using a technique similar to that by Jacobs *et al.* [8] for low-pass

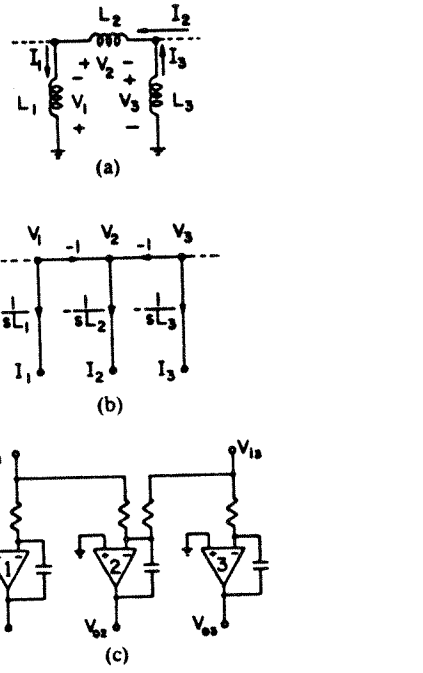


Fig. 10. (a) An inductor loop. (b) Corresponding signal flowgraph. (c) Realization by active *RC* integrators.

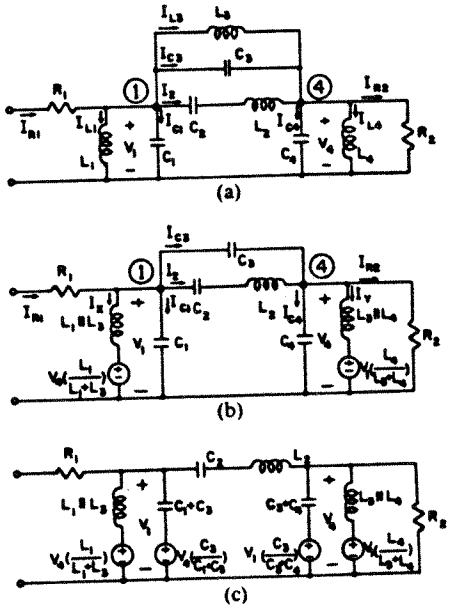


Fig. 11. (a) Doubly-terminated sixth-order elliptic bandpass *LC* ladder. (b) Inductor L_5 represented by voltage-controlled voltage source. (c) Final Thevenin equivalent circuit of Fig. 11(a).

filters. Fig. 11(a) shows a doubly-terminated sixth-order elliptic bandpass filter. By writing the nodal equation at node (1), we have

$$I_{R1} - \frac{V_1}{sL_1} - I_{C1} - I_2 - I_{C3} - \frac{V_1 - V_4}{sL_3} = 0. \tag{19}$$

Rewriting (19), we have

$$V_1 = (I_{R1} - I_{C1} - I_2 - I_{C3})\frac{sL_1L_3}{L_1 + L_3} + V_4\frac{L_1}{L_1 + L_3}. \tag{20}$$

Similarly, writing the nodal equation at node (4) will give

$$V_4 = (I_{C3} + I_2 - I_{C4} - I_{R2})\frac{sL_3L_4}{L_3+L_4} + V_1\frac{L_4}{L_3+L_4}. \quad (21)$$

From (20) and (21), we see that the inductor L_3 can be represented by two voltage-controlled voltage sources, with corresponding change in inductor values, as shown in Fig. 11(b). Likewise, to remove the capacitor C_3, we wrote the nodal equation at node (1) of Fig. 11(b) and have

$$I_{R1} - I_x - I_2 - V_1(sC_1) - (V_1 - V_4)sC_3 = 0 \quad (22)$$

or

$$V_1 = (I_{R1} - I_x - I_2)\frac{1}{s(C_1+C_3)} + V_4\frac{C_3}{C_1+C_3}. \quad (23)$$

Similarly, for node (4)

$$V_4 = (I_2 - I_y - I_{R2})\frac{1}{s(C_3+C_4)} + V_1\frac{C_3}{C_3+C_4}. \quad (24)$$

Equations (23) and (24) result in the final circuit shown in Fig. 11(c). The shunt inductor L_3 and capacitor C_3 are now replaced by voltage-controlled current sources. The corresponding switched-capacitor circuit for Fig. 11(c) requires only 6 operational amplifiers to implement since the voltage-controlled voltage sources can be easily realized by feedforward paths.

III. The Effects of Amplifier Nonidealities on Switched-Capacitor Filters

The integrator is the principal building block for active filters realized by the leapfrog or the active ladder synthesis technique. Any nonideal characteristics of the integrator can cause the frequency response of active filters to deviate from their designed response. In particular the finite dc gain of the integrator can cause the passband of the filter to droop. Even a small amount of excess phase in the vicinity of the unity gain frequency of the integrator can result as peaking at the band edge and Q-enhancement for high selectivity filters.

In order to determine the performance requirements of the amplifier that is intended for high-frequency and high-selectivity filters, the relationship between the open-loop gain a_o, and the unity gain bandwidth ω_u of the amplifier and the two poles p_1 and p_2 of the integrator must be established. Here, p_1 is the low-frequency pole caused by the finite amplifier gain, and p_2 is the high-frequency pole attributed to the finite amplifier bandwidth. For continuous-time integrators, there is a straightforward connection between a_o and p_1, and ω_u and p_2 [17]. Unfortunately, such is not the case for switched-capacitor integrators. In order to obtain the exact relationship between the amplifier parameters and the frequency response of the switched-capacitor integrator, the system is first analyzed in the sample-data domain, and the result is then translated to the frequency domain by an appropriate mapping technique [18]. It can be shown that for a typical LDI switched-capacitor integrator, assuming a single-pole operational amplifier model, the corresponding equivalent integrator poles p_1 and p_2 are given by the following equations:

$$p_1 \approx \frac{1}{T_c}\left[\frac{1}{a_o\dfrac{C_i}{C_s+C_n+C_i}}\right] \quad (25)$$

$$p_2 \approx \frac{1}{T_c}\left[\frac{1}{\exp - mT_c\omega_u}\right] \quad (26)$$

where the terms are defined as follows:

T_c is the period of the clock phases,

a_o is the open-loop dc gain of the amplifier,

C_s, C_i, and C_n are the sampling, integration and the parasitic input capacitance, respectively,

m is the duty cycle of the clocks, and

ω_u is the unity gain frequency of the amplifier.

The bracketed term in (25) is the inverse of the loop gain of the switched-capacitor integrator during the integration phase. The bracketed term in (26) corresponds to the inverse of the settling error that is caused by the finite bandwidth of the amplifier. Thus, the degree of the switched-capacitor integrator nonideality is directly related to the amount of error signal present at the amplifier input. Equations (25) and (26) indicate that the gain and the bandwidth be made as large as possible.

IV. High-Speed Amplifier Design Considerations

It is clear now that the successful implementation of high-frequency and high-selectivity switched-capacitor filters is dependent on the design of a fast settling amplifier that has sufficient gain. Fig. 12 shows two amplifier topologies that may be used to satisfy the gain and bandwidth requirements. In switched-capacitor filters the amplifiers, which are configured as integrators, drive on-chip capacitive loads; therefore, as long as they are not required to interface with the outside world, they can have a high output impedance. This simplification allows the use of simple two-stage or single-stage amplifier design.

Assume for the sake of simplicity that the active devices in Fig. 12 are characterized by two parameters—transconductance g_m and output resistance r_o—and that they drive ideal current source loads as shown. Under these conditions, it can be shown that both amplifiers have identical low-frequency gain of $(g_m r_o)^2$. Their frequency response, however, is different. The dominant and the nondominant pole locations of the two-stage and the single-stage amplifiers are listed in Table I. If both of these amplifiers are utilized in a closed-loop configuration, such as in a switched-capacitor integrator, it can be shown that the settling behavior is determined by the time constant of the nondominant pole. This is because in a closed-loop configuration with increasing loop gain, the dominant and non-

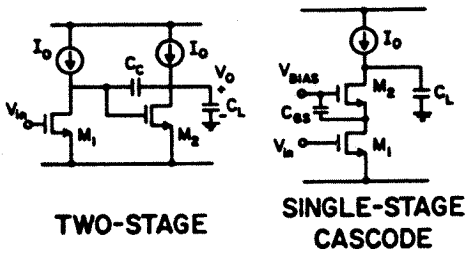


Fig. 12. Two-stage and single-stage amplifiers.

TABLE I
DOMINANT AND NONDOMINANT POLE LOCATIONS FOR THE TWO- AND SINGLE-STAGE AMPLIFIERS

	Dominant pole location	Nondominant pole location
Two-stage amplifier	$\frac{1}{r_o C_c g_m r_o}$	$\frac{g_m}{C_L}$
One-stage amplifier	$\frac{1}{r_o C_L g_m r_o}$	$\frac{g_m}{C_p}$

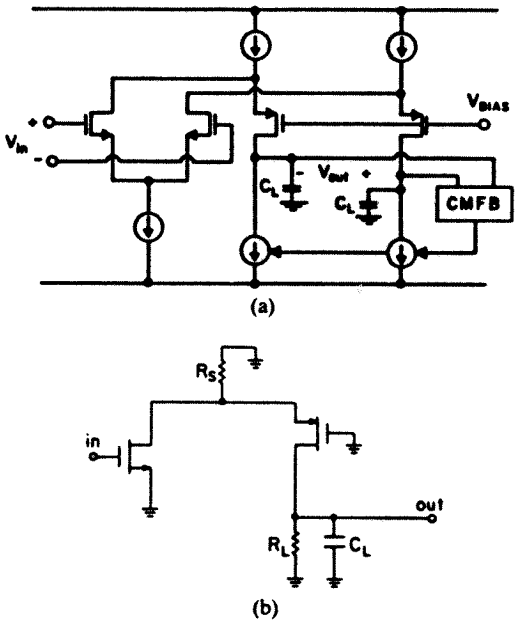


Fig. 13. (a) Simplified schematic of the fully differential folded cascode amplifier. (b) Small-signal equivalent-differential mode half-circuit.

dominant poles converge and form a complex pole pair. The settling behavior is determined by the reciprocal of the real part of the complex pole which is approximately equal to $-\frac{1}{2}s_n$, where $-s_n$ is the nondominant pole location in the s-plane. It should be noted that the presence of spurious high-frequency poles tends to push the complex pole pair toward the imaginary axis resulting in a reduced real part σ_p. Even in such a case, the resulting real part of the complex pole is still strongly influenced by the nondominant pole. In light of this information, to achieve a fast settling response, the amplifier must have a very high-frequency nondominant pole.

The ratio of the nondominant pole of the single-stage cascode to the two-stage configuration is given by

$$\frac{s_n(\text{one-stage})}{s_n(\text{two-stage})} = \frac{C_l}{C_p}. \tag{27}$$

In a switched-capacitor filter environment, C_p, which is equal to the total parasitic capacitance present at the cascode node, is typically one-fifth to one-tenth of the total load capacitance C_l, which the amplifier drives. Thus, the single-stage cascode amplifier exhibits a faster settling behavior than the two-stage amplifier.

To satisfy the gain and speed requirements for the high-frequency and high-selectivity filters, a variant of the single-stage cascode configuration, the folded cascode amplifier is proposed. A simplified schematic is shown in Fig. 13(a). The n-channel devices are the drivers, and the p-channel devices act both as the cascode elements and dc level shifters. The load capacitors C_l function as the compensation capacitor. The small-signal differential-mode half-circuit is depicted in Fig. 13(b). Here, R_s and R_l represent the finite output resistance of the current source loads. In order to maintain a high gain, it is crucial that the output resistance of the current is kept large. The exact differential-mode voltage gain expression is given in (13):

$$A_v = -(g_{mn}r_{on})(g_{mp}r_{op})\left\{\frac{1}{1+\frac{r_{on}}{R_s}+\frac{r_{on}}{R_{on}}}\right\}\left\{\frac{1}{1+\frac{r_{op}}{R_l}}\right\} \tag{28}$$

where g_{mn} and r_{on} and g_{mp} and r_{op} are the transconductance and the output resistance of the NMOS and PMOS devices, respectively, and R_s and R_l are the finite output resistance of the current source loads, and

$$R_n = \frac{1}{g_{mp}}\left(1+\frac{R_l}{r_{op}}\right)$$

is the effective resistance seen looking into the source terminal of the p-channel cascode device.

If the output resistance of the loads is much larger than that of the active devices, the overall gain approaches the theoretical maximum, which is the combined $g_m r_o$ products of the n- and p-channel devices.

The complete schematic diagram of the fully-differential folded cascode amplifier is shown in Fig. 14. Two PMOS transistors, $MP1$ and $MP1A$, provide the bias current to the amplifier. In order to maintain a reasonably high output resistance, the channel length of these two devices is made longer than that of the cascode elements $MP2$ and $MP2A$. The high impedance current source loads at the output of the amplifier are realized by cascoded current source. $MN1$ through $MN2A$. The resulting output resistance is slightly over 1 MΩ.

The common-mode feedback circuit is an essential part of any fully-differential amplifiers. Without it the common-mode output remains undefined, and the amplifier may drift out of its high gain operating regime. $MN3$ and

Fig. 14.

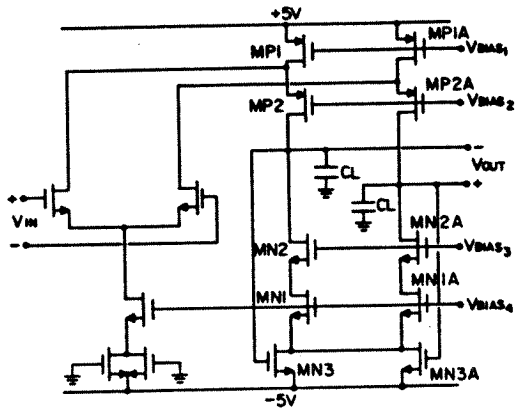
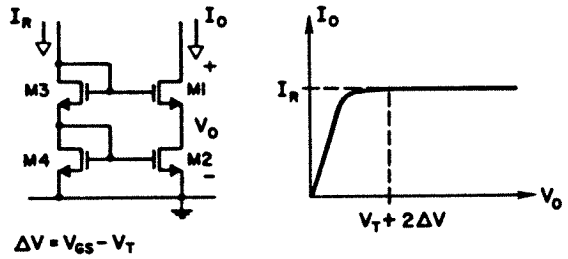


Fig. 14. Complete schematic of the fully differential folded cascode amplifier.



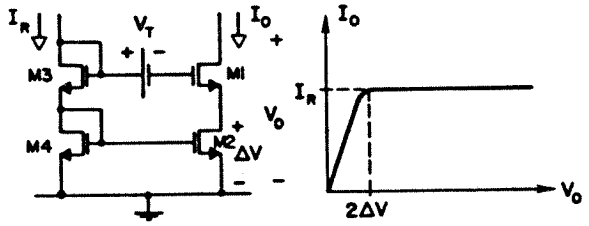


Fig. 15. Concept of the high-swing cascode bias circuitry.

MN3A, which are biased in their triode region, form the common-mode feedback circuit. These two devices sample the common-mode output signal and feed back a correctional common-mode signal into the source terminals of *MN2* and *MN2A*. The cascode devices, *MN1* through *MN2A*, amplify this compensating signal to restore the common mode output voltage to its original level.

One of the major drawbacks of the cascode amplifier is its reduced output swing. As shown in Fig. 15 if the cascode devices *M1* and *M2* are biased from a diode string *M3* and *M4*, the voltage across the cascodes can swing only to within $V_T + 2V_{Dsat}$ from the negative rail before *M1* goes into the triode region. The voltage swing can be improved by inserting a level-shifting dc source whose value is exactly equal to V_T, between the gates of *M1* and *M3*. The level-shifting voltage source forces *M2* to be biased at the edge of saturation with a drain-to-source voltage that is equal to V_{Dsat}. Now the voltage across the cascode can swing to $2V_{Dsat}$ from the negative rail before *M1* is pulled out of its saturation regime of operation. A practical realization of the high swing cascode bias circuit is given in

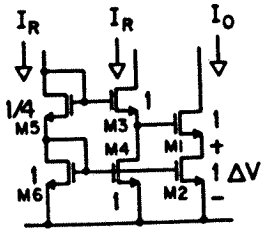


Fig. 16. Practical realization of the high-swing cascode bias.

TABLE II
OPERATIONAL AMPLIFIER PERFORMANCE (± 5 V SUPPLY)

Unity gain frequency (2 pF load)	80 MHz
Setting time to 0.1% of final value (2 pF load 2.5 V steps)	40 ns
Power dissipation	10 mW
Die area	200 mils^2
Open loop gain	1500

Fig. 16. All devices conduct identical biasing current of I_o. They all have the same aspect ratio except for *M5* whose W/L is $\frac{1}{4}$ that of the others. This causes *M2* to be biased at the edge of saturation with V_{DS} equal to V_{Dsat}. The voltage across *M1* and *M2* can now swing to within 2Δ V from the negative supply rail.

V. EXPERIMENTAL FILTER

An experimental 260 kHz bandpass filter having a selectivity of 40 was designed and fabricated. The specifications of this filter correspond to a typical AM IF filter for a car radio. In order to meet the specifications, a sixth-order elliptic bandpass filter is required. The switched-capacitor implementation is clocked at 4 MHz and through the use of T-networks, the maximum capacitor ratio spread has been reduced from 40 to approximately 8. The block diagram of the switched-capacitor sixth-order elliptic bandpass filter is as shown in Fig. 7. As indicated in Fig. 7(a), a seventh operational amplifier is added here as a summer at the filter output.

To meet the high-frequency high-Q requirements of the filter, a high-speed amplifier was designed and fabricated in CMOS technology. This amplifier employed the fully differential, folded-cascode configuration mentioned in Section IV, resulting in a unity gain bandwidth of 80 MHz and occupying a die area of 200 mils^2. The overall operational amplifier performance is summarized in Table II.

The experimental filter was fabricated using a 4 μm double-poly p-well CMOS technology. The microphotograph of the die is shown in Fig. 17. The frequency response obtained from a representative filter chip is shown in Fig. 18. The traces show the overall frequency response while the bottom traces depict the detailed passband response. The inner traces are for a Q of 40 filter, and the outer traces are for a Q of 20 filter. Both traces were obtained from the same filter chip. The Q has been changed

Fig. 17. Die photo of the experimental filter chip.

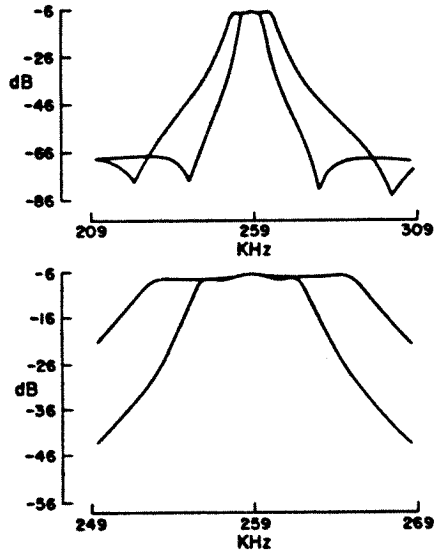


Fig. 18. Frequency response of the filter chip.

by switches which alter the amount of attenuation in the termination and the interresonator coupling paths. For both Q's the center frequency remains stable at 260 kHz. The pertinent statistics for this filter are listed in Table III, where we compare the specifications, the designed response, and the experimental results. All the specifications are met and the small discrepancies between the designed and measured results can be explained by small errors in the capacitor ratios.

Table III also shows the dynamic range, average PSRR, total in-band noise, and power dissipation of the experimental filter. The PSRR of the filter was smaller than expected since we would expect a fully differential filter architecture to be insensitive to power supply variations. A plot of the PSRR as a function of frequency is shown in Fig. 19, where we notice that the minimum PSRR in the passband is about 17 dB. This suggested that the circuit was not well balanced, and a close examination of the chip showed nonsymmetrical layouts in certain areas. To verify that this is the case, we measured the common-mode to differential-mode response of the filter by injecting an ac common-mode signal at the input. Indeed, we notice a large common-mode to differential-mode gain as shown in Fig. 20, where we plot the measured frequency response of both the differential-mode signal and the common-mode

TABLE III
MEASURED RESULTS OF AM IF FILTER AT $V_{DD} = 10$ V

	Specifications	Designed value	Experimental results
Center frequency	260 kHz ± 1%	260 kHz	259 kHz
Ripple content	3 dB max	0.97 dB	1.3 dB
−3 dB-BW	5 kHz min	7.2 kHz	6.5 kHz
Rejection at ±10 kHz	30 dB min	34.7 dB	38 dB
Stopband rejection	55 dB min	60.4 dB	62 dB
Clock frequency	4 MHz	4 MHz	4 MHz
Gain	−6 dB	−6 dB	−6 dB
Dynamic range			70 dB
PSRR			30 dB
Total in band noise			300 μV_{rms}
Power dissipation			70 mV

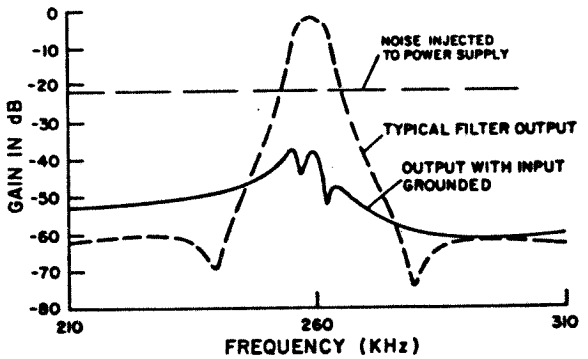


Fig. 19. Experimentally observed PSRR response of filter chip.

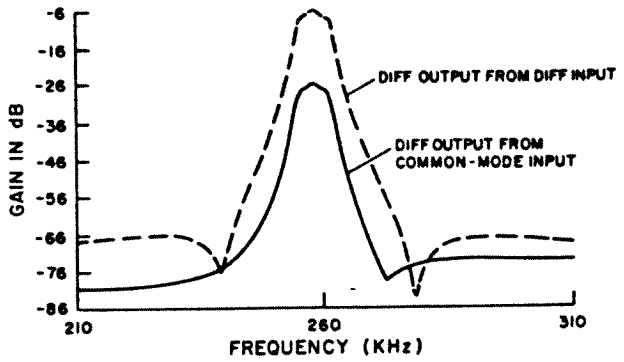
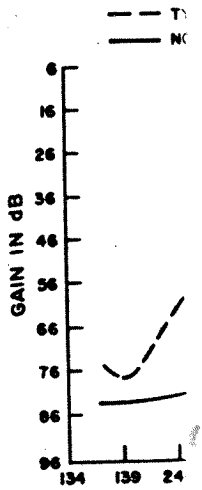


Fig. 20. Experimental common-mode and differential-mode frequency response.

signal. From this figure, the common-mode rejection ratio in the passband is only about 20 dB, thus showing an unbalanced circuit which gives rise to the smaller than expected PSRR.

The in-band noise of 300 μV_{rms} is large compared with voiceband low-pass filters, but this is expected of high-Q



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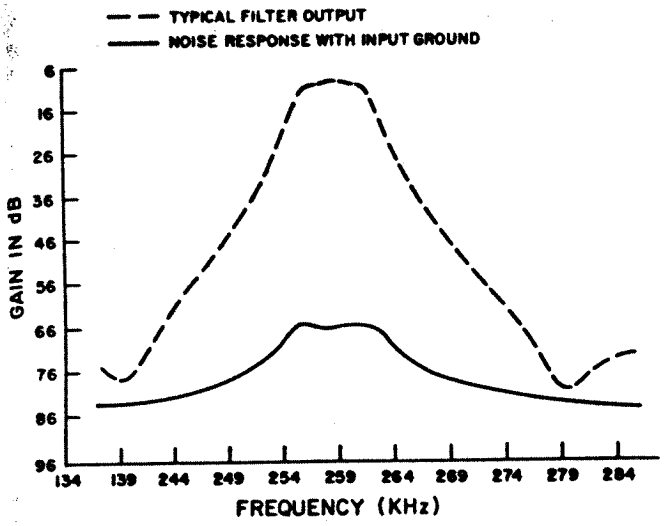

Fig. 21. Measured noise response of filter chip.

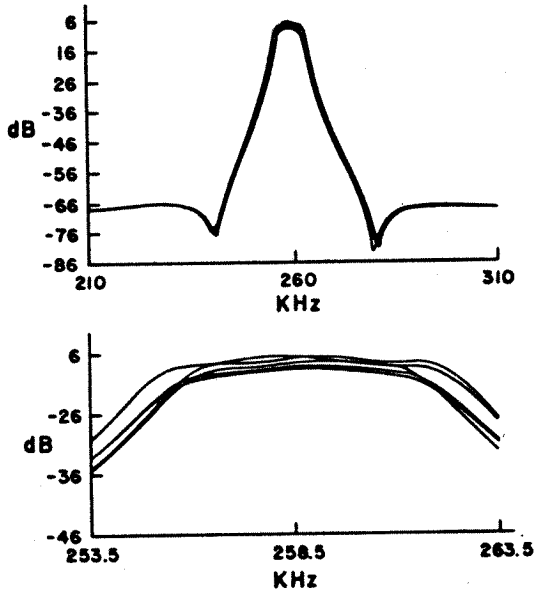

Fig. 22. Ensemble frequency response of five different filter chips.

bandpass ladders. The fact that high-Q filters have greater noise basically stems from the inherent large gains of the resonators, which is only limited by the terminations, so that the noise contributions are enhanced by the large gains. In high-frequency filters, this situation is made worse because the sampling capacitors cannot be too large. In our case C_S is roughly 0.5 pF, which is smaller than the sampling capacitors found in most codec filters. A plot of the measured noise response of the AM IF filter is shown in Fig. 21.

In addition to the above measurements, the frequency response from different chips are measured to check the variations from die to die. This is shown in Fig. 22, which demonstrates very consistent frequency characteristics with no variations in the center frequency at all. Thus, the identical resonator filter architecture indeed helps to reduce sensitivity problems.

VI. Conclusion

A design approach to realize high-frequency and high-selectivity switched-capacitor filters has been presented. An experimental 260 kHz elliptic bandpass filter has been designed and fabricated. From the measured experimental performance of the filter, we can conclude that the switched-capacitor filtering technique is indeed a viable method in implementing high-frequency and high-selectivity monolithic filters.

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Tat C. Choi, photograph and biography not available at the time of publication.

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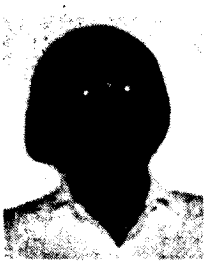
Robert W. Brodersen (M'76–SM'81–F'82), for a photograph and biography, see p. 3 of the February 1983 issue of this JOURNAL.

Paul R. Gray (S'65–M'69–SM'76–F'80), for a photograph and biography, see this issue, p. 643.



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