*=============**Class_D_Dual_Supplies**===========

Class D output stages do some unusual thing when operating off of split supplies. Power should all obey the laws of thermal dynamics. Everything should make sense.

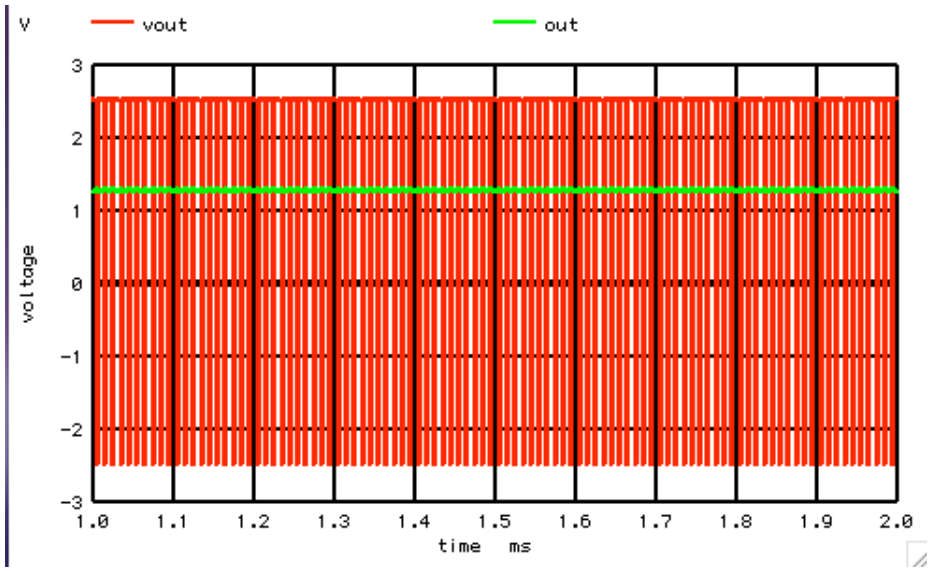
In this case there are two supplies, Vcc and Vee, which are supplying +/-2.5V. There is also an external common mode power source VCM to do experiments.

```
=======================================================================
ClassD_DC_DualSupply
*
*                  VCC _/\  /\  /\_ VP
*                     _|_  \/  \/  _|
*                    /VCC\ RP     <-
*                    \___/       ||___ NMP1
*                     _|_    ____||
*                     ///   |    ||_ VOUT_  _  _
*                           |      |   / \/ \/ \         R1 = 5
* VDUTY    _|_   VG    VG___|     _|___| () () |__|OUT|__/\  /\  /\__
*         / _ \             |__||       L1       |___|    \/  \/   _|_
*   _|_  //  \ \   ___|      ||        100u       |      C1       /VCM\
*  /VDT\ \    \//  _|_      ||-> NMN1             |__||__ 3u      \___/
*  \___/  \___/    ///  RM   |    Freq = 9K           _|_         _|_
*   _|_    _|_  /VEE\ _/\  /\  /\_|   Z=5.8Ohms       ///         ///
*   ///    ///  \___/|  \/  \/  VM
*                 |__|
*
*
*.OPTIONS  GMIN=1f       METHOD=trap  ABSTOL=1u     TEMP=27   srcsteps = 1  gminsteps = 1
*.OPTIONS  RELTOL=.001   ABSTOL=1n    VNTOL=1u      ITL4=500  ITL1=400
*=========Create_Signal=================
VT        VT     0     DC     0      PWL(   0     0    1      1)
Vfreq     Vfreq  0     DC     100k
VD        VD     0     DC     .75
VPI       VPI    0     DC     3.141592653589793
B_TRI     TRI    0     V =    acos( cos(6.283185*V(VFreq)*V(VT)) )/v(VPI)
BVG       VG     0     V =    5*u( v(TRI) -v(VD)) -2.5
VCC       VCC    0     DC     2.5
VEE       VEE    0     DC     -2.5
RPP       VCC    VP    1u
RN        VN     VEE   1u
MN1       VOUT   VG    VN     VEE    NMOSC    W=90000u    L=1u
MP1       VOUT   VG    VP     VCC    PMOSC    W=90000u    L=1u
L1        VOUT   OUT   100u
C1        OUT    0     3u
Rout      OUT    VCM   5
Vrout     Vrout  0     DC     5
VCM       VCM    0     2.5
*=========The_CMOS_Model_Files================================
.model    NMOSC               NMOS(Level=  1  Cbs=2f Cbd=2f)
.model    PMOSC               PMOS(Level=  1  Cbs=2f Cbd=2f)
.control
*TRAN     TSTEP  TSTOP  TSTART TMAX   ?UIC?
tran      .01u    2m     1m      .01u
linearize
set       pensize = 2
plot      vout out

=======================================================================
```

To start off, the output duty cycle has been set to 75%, and VCM has been set to +2.5V. One would expect there to be +1.25V at the output, and 250mA should flow across RL.

===



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But when one looks at the polarity of current at VP and VN, one sees that VP is above 2.5V and VN is below VEE.

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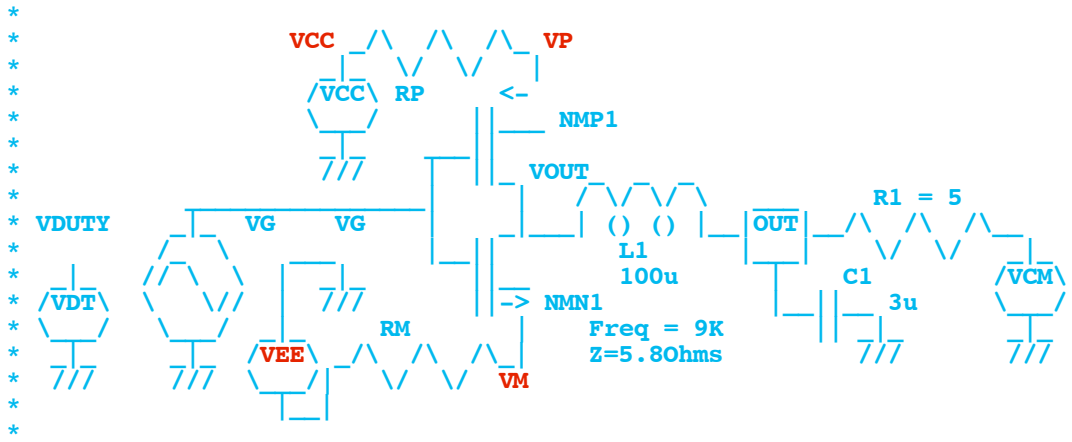
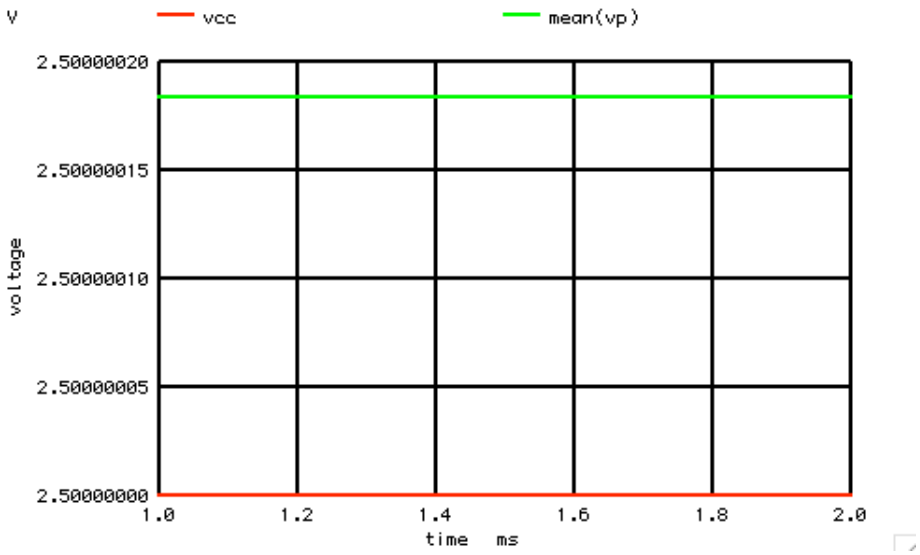
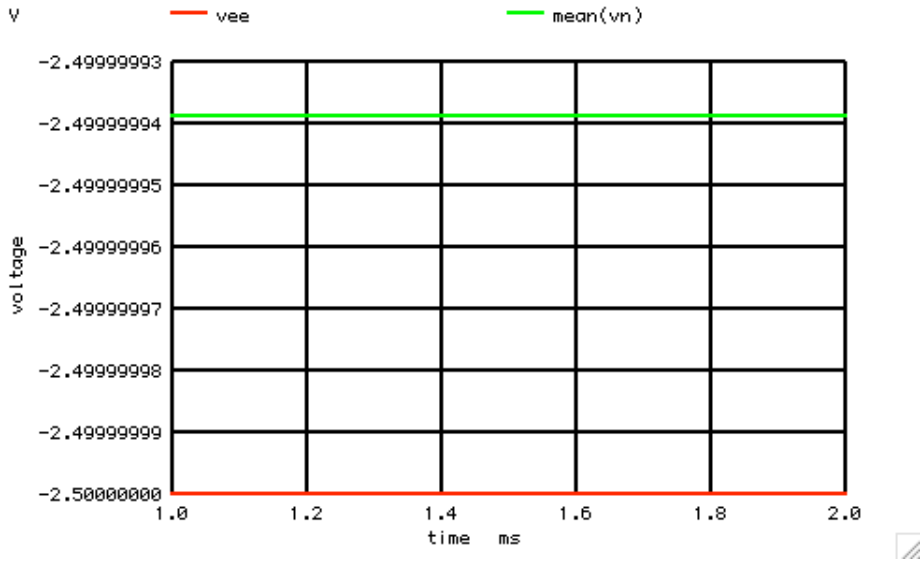



```
plot      vcc mean(vp)
plot      vee mean(vn)
```





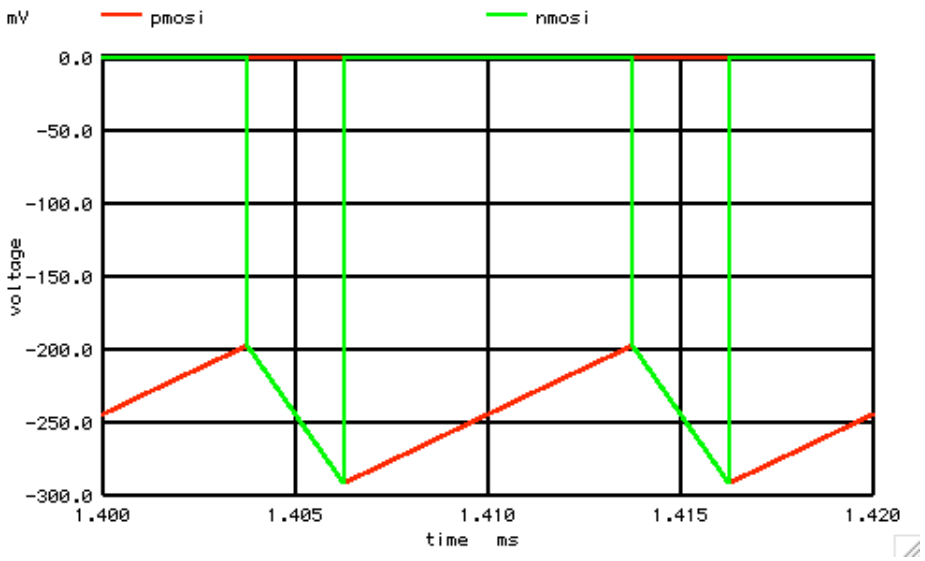
==========

The currents flowing in VCC and VEE can be found and plotted to show that there is a 75% multiplexing of the 250mA of current flowing in RL. And for VCC, the current coming out is negative polarity. In other words the current is actually going in. In the case of VCC being a battery, VCC is getting charged up.

The current is also flowing into VEE. But since this is the negative node of VEE, VEE is being discharged.

==========

```
let       pmosi = (vcc-vp)*1000k
let       nmosi = (vee-vn)*1000k
let       rout_i = (out-vcm)/vrout[0]
plot      pmosi  nmosi   xlimit 1.4m 1.42m
```



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A little math processing comes in handy to show what all is going on.

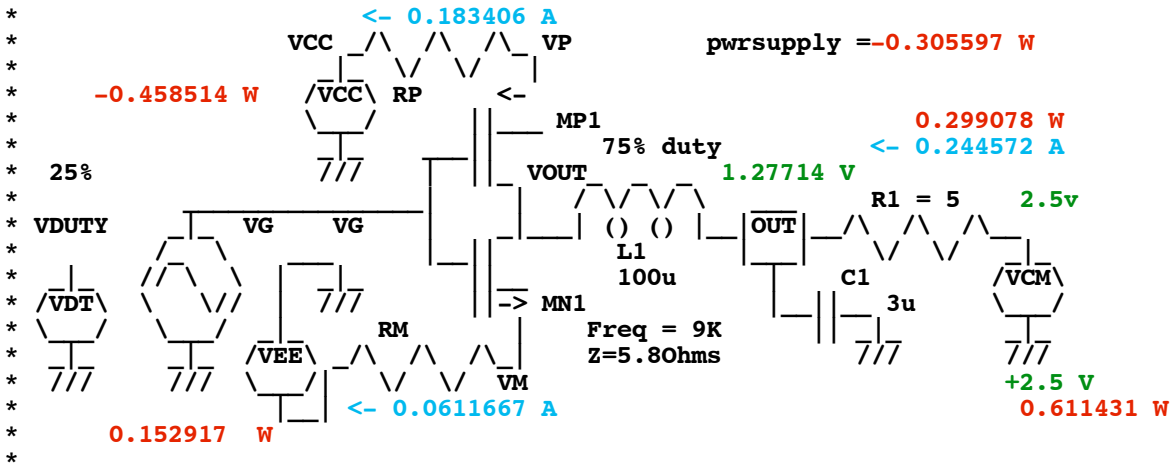
==========

```
let       pmospwr= pmosi*(vcc-vout)
let       nmospwr= nmosi*(vout-vee)
let       pmospwrdc=mean(pmospwr)
let       nmospwrdc=mean(nmospwr)
echo      "pmospwrdc =$&pmospwrdc  nmospwrdc =$&nmospwrdc"

let       outdc=mean(out)
let       vcmdc = vcm[0]
let       routdc =mean(vrout[0])
let       routidc = mean(rout_i)

let       pmosidc = mean(pmosi)
let       nmosidc = mean(nmosi)
let       vccpwr=    mean((pmosi)*vcc[0])
let       veepwr=    mean((nmosi)*vee[0])
let       vcmpwr=    -1*routidc*vcm[0]
let       routpwr    =  routidc*routidc*routdc

let       pwrsupply = vccpwr +veepwr
let       pwrEff     = routpwr/pwrsupply
echo      "pwrsupply =$&pwrsupply"

echo      "outdc  =$&outdc  rload  =$&routdc routidc =$&routidc pmosidc =$&pmosidc nmosidc
=$&nmosidc   "
echo      "vccpwr =$&vccpwr vcmpwr =$&vcmpwr veepwr  =$&veepwr  routpwr =$&routpwr vcmdc
=$&vcmdc  "

.endc
.end
```

==========

For the case of VCM = +2.5V and 75% duty cycle.

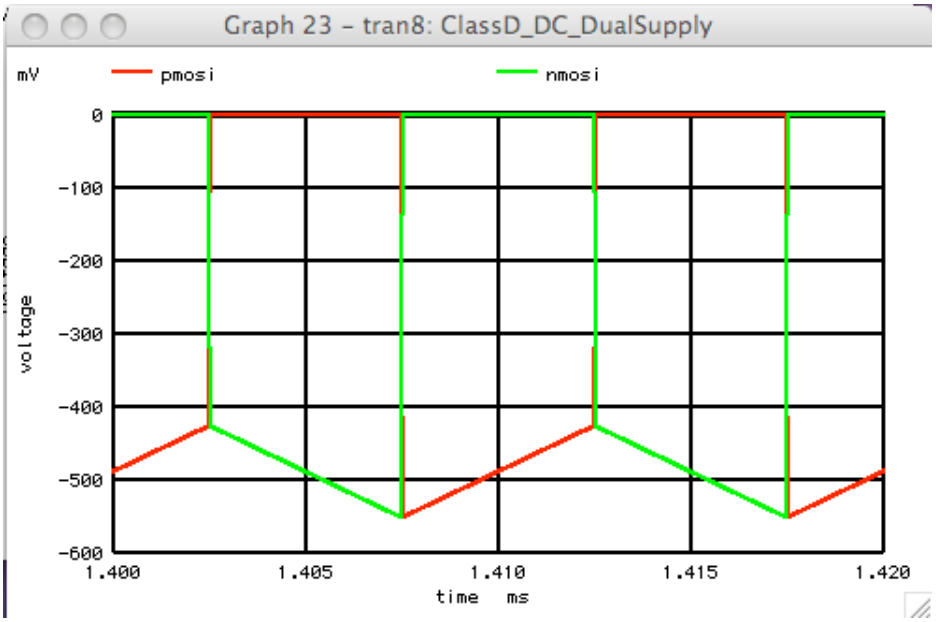
```
Circuit: ClassD_DC_DualSupply
pmospwrdc =0.00441995  nmospwrdc =-0.00229973
pwrsupply =-0.305597
outdc =1.27714    rload  =5 routidc =-0.244572  pmosidc =-0.183406 nmosidc =-0.0611667
vccpwr =-0.458514 vcmpwr =0.611431 veepwr =0.152917  routpwr =0.299078  vcmdc =2.5
```



It looks like node OUT is around 1.25V and for a current in of around 250mA. In other words the V to I relationship at the OUT node is that of a 5 Ohm resistor.

Power supply VEE is supplying around 625mW of power, half of which is dissipated by RL. So node OUt is receiving the other half of that power. It looks like VEE is getting charge up and Vee is getting discharge. But it look likes there is a net charging for the two supplies which equal the power that node OUT is absorbing.

==========

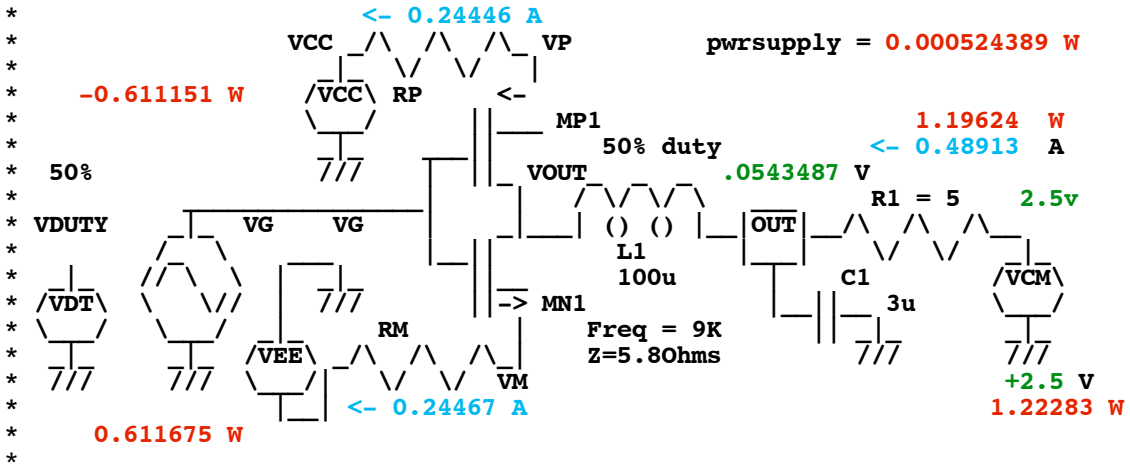


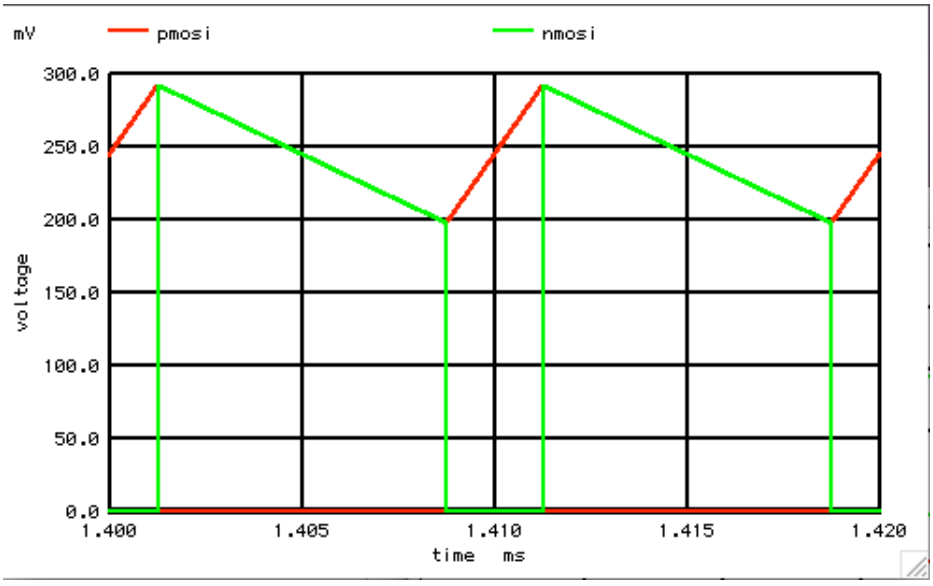
For the case of VCM = +2.5V and 50% duty cycle. Now VCM is supplying about 1.25W of power and RL is receiving it all.

Now about 500mA is flowing into output node OUT. But since it is at zero volts, it is absorbing little power.

Now Vee is still getting discharged and Vcc charges, but both at a equal and opposite value. So there is no net charge to the two supplies, but there is a high efficiency transfer of power between the two supplies.

```
pmospwrdc =0.0120588  nmospwrdc =-0.0146741
pwrsupply =0.000524389
outdc =0.0543487  rload =5 routidc =-0.48913  pmosidc =-0.24446 nmosidc =-0.24467
vccpwr =-0.611151 vcmpwr =1.22283 veepwr =0.611675  routpwr =1.19624  vcmdc =2.5
```





For the case of VCM = -2.5V and 25% duty cycle. Now VCM is supplying about 625W of power and RL is receiving half. Now about 250mA is flowing out of output node OUT. The output Node OUT is again acting like a resistor in terms of voltage, current and power, and the net power is being transferred to the supplies. But in this case Vcc is getting discharged.

```
pmospwrdc =0.00229985  nmospwrdc =-0.00442002
pwrsupply =-0.30559
```

```
outdc =-1.27712  rload =5 routidc =0.244576  pmosidc =0.0611701 nmosidc =0.183406
vccpwr =0.152925 vcmpwr =0.61144 veepwr =-0.458515  routpwr =0.299087  vcmdc =-2.5
```

```
*                       -> 0.0611701 A
*                  VCC _/\  /\  /\_ VP         pwrsupply = -0.30559 W
*                     _|_   \/  \/   |
*     0.152925 W     /VCC\ RP       <-
*                    \___/         ||___ MP1                      0.299087 W
*                      _|_        _||      25% duty            -> 0.244576 A
*  75%                 ///       |  ||_ VOUT_  _  _  -1.27712 V
*                                |     |    / \/ \/ \           R1 = 5    -2.5v
* VDUTY      _|_  VG    VG       |    _|___| () () |__|OUT|__/\  /\  /\__
*           / _ \                |__||         L1        |___|  \/  \/    _|_
*   _|_    // \  \    ____|_       ||          100u        |     C1       /VCM\
*  /VDT\   \     \//   |  ///      ||-> MN1                |__||__ 3u     \___/
*  \___/    \___/     _|_      RM        |     Freq = 9K        ||  _|_      _|_
*   _|_      _|_    /VEE\ _/\  /\  /\_|     Z=5.8Ohms              ///      ///
*   ///      ///    \___/|   \/  \/  VM                                  -2.5 V
*                      |__|  -> 0.183406 A                               0.61144 W
*     -0.458515 W
```

So it looks like it is possible to build a 5 ohm Energy Harvesting Resistor.

```
===========Full_Netlist_For_Copy_Paste=======================
ClassD_DC_DualSupply
*
*                  VCC _/\  /\  /\_ VP
*                     _|_   \/  \/   |
*                    /VCC\ RP       <-
*                    \___/         ||___ MP1
*                      _|_        _||
*                      ///       |  ||_ VOUT_  _  _
*                                |     |    / \/ \/ \           R1 = 5K
* VDUTY      _|_  VG    VG       |    _|___| () () |__|OUT|__/\  /\  /\__
*           / _ \                |__||         L1        |___|  \/  \/    _|_
*   _|_    // \  \    ____|_       ||          100u        |     C1       /VCM\
*  /VDT\   \     \//   |  ///      ||-> MN1                |__||__ 3u     \___/
*  \___/    \___/     _|_      RM        |     Freq = 9K        ||  _|_      _|_
*   _|_      _|_    /VEE\ _/\  /\  /\_|     Z=5.8Ohms              ///      ///
*   ///      ///    \___/|   \/  \/  VM
*                      |__|
*
*
*.OPTIONS  GMIN=1f       METHOD=trap   ABSTOL=1u     TEMP=27    srcsteps = 1  gminsteps = 1
*.OPTIONS  RELTOL=.001   ABSTOL=1n     VNTOL=1u      ITL4=500   ITL1=400
*=========Create_Signal==================
VT        VT     0     DC     0     PWL(   0     0    1     1)
Vfreq     Vfreq  0     DC     100k
VD        VD     0     DC     .75
VPI       VPI    0     DC     3.141592653589793
B_TRI     TRI    0     V =    acos( cos(6.283185*V(VFreq)*V(VT)) )/v(VPI)
BVG       VG     0     V =    5*u( v(TRI) -v(VD)) -2.5
VCC       VCC    0     DC     2.5
VEE       VEE    0     DC     -2.5
RPP       VCC    VP    1u
RN        VN     VEE   1u
MN1       VOUT   VG    VN     VEE   NMOSC   W=90000u    L=1u
MP1       VOUT   VG    VP     VCC   PMOSC   W=90000u    L=1u
L1        VOUT   OUT   100u
C1        OUT    0     3u
Rout      OUT    VCM   5
Vrout     Vrout  0     DC     5
VCM       VCM    0     2.5
*=========The_CMOS_Model_Files==================================
.model    NMOSC              NMOS(Level=  1  Cbs=2f Cbd=2f)
.model    PMOSC              PMOS(Level=  1  Cbs=2f Cbd=2f)

.control
```

```
*TRAN     TSTEP  TSTOP  TSTART TMAX   ?UIC?
tran      .01u    2m     1m      .01u
linearize
set       pensize = 2
plot      vout out

plot      vcc mean(vp)
plot      vee mean(vn)

let       pmosi = (vcc-vp)*1000k
let       nmosi = (vee-vn)*1000k
let       rout_i = (out-vcm)/vrout[0]
plot      pmosi  nmosi   xlimit 1.4m 1.42m
let       pmospwr= pmosi*(vcc-vout)
let       nmospwr= nmosi*(vout-vee)
let       pmospwrdc=mean(pmospwr)
let       nmospwrdc=mean(nmospwr)
echo      "pmospwrdc =$&pmospwrdc  nmospwrdc =$&nmospwrdc"

let       outdc = mean(out)
let       vcmdc = vcm[0]
let       routdc =mean(vrout[0])
let       routidc = mean(rout_i)
let       pmosidc = mean(pmosi)
let       nmosidc = mean(nmosi)
let       vccpwr=    mean((pmosi)*vcc[0])
let       veepwr=    mean((nmosi)*vee[0])
let       vcmpwr=    -1*routidc*vcm[0]
let       routpwr    =  routidc*routidc*routdc

let       pwrsupply = vccpwr +veepwr
let       pwrEff     = routpwr/pwrsupply
echo      "pwrsupply =$&pwrsupply  "

echo      "outdc =$&outdc  rload =$&routdc routidc =$&routidc  pmosidc =$&pmosidc nmosidc =
$&nmosidc   "
echo      "vccpwr =$&vccpwr vcmpwr =$&vcmpwr veepwr =$&veepwr  routpwr =$&routpwr  vcmdc =
$&vcmdc  "

*plot      pmosi nmosi pmosidc nmosidc  xlimit 1m 1.004m
*plot      vout  out    xlimit 1m 1.004m
*plot      pmospwr nmospwr  pmospwrdc nmospwrdc xlimit 1m 1.004m ylimit -20m 20m

.endc

.end
```

9.16.10_1.59PM

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