*=============**CLASS_D_OPAmp**===========

Suppose one wants to take the concept of a Class D amplifier to make an Op Amp. There are some important Gain bandwidth considerations if one wants to make this Op Amp unity gain stable.

```
=======================================================================
CLASS_D_OpAmP_AC
*
*
*    |INN|_|\  BOTA          RB
*    |___| |+\        VD
*          |  \/\/\_______/\  /\  /\____
*          |  /\_/\_/_|_    \/  \/   _|_
*    |INP|_|-/       ___   |  CCOMP   /VB \
*    |___| |/        ___   |          \___/
*                     |    |           _|_
*         _____|     ///   |  |\       ///
*            _|_       |   |  |+\
*           /   \          |__|  \
*          /B_TRI\            |   \___|VG |  PWM output
*          \     /            |   /   |___|
*           \___/  |__________|-/ BVG
*            _|_              |/
*            ///
=======================================================================
```

In this simulation, the Op Amp is being modeled as an input transconductance stage which has its open loop gain defined by the input transconductance and RB, and its bandwidth is defined by the input transconductance and CComp.

The output stage is being modeled as feeding the Op Amp's signal into one side of a voltage comparator which is seeing a triangle wave. The duty cycle output is fed into a Class D output stage.

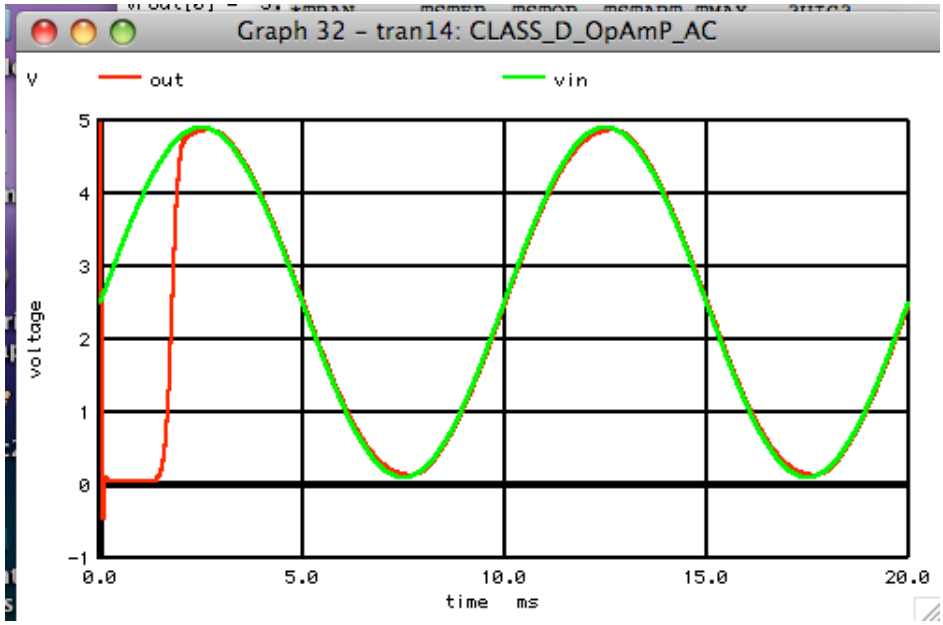
```
=======================================================================
*
*                     VCC _/\  /\  /\_ VP
*                        _|_ \/  \/   |
*                       /VCC\ RP     <-               1000p
*                       \___/       ||___ MP1
*                        _|_        ||              |______||______
*    VIN                 ///    ____||_             |      ||      |
*         _______|INP|_|\          |   |_           |  _/\/\/\_    |  OUT  R1 = 5
*      _|_       |___| |+\         |     |_|VOUT|_|__| () ()  |_|_____/\  /\  /\___ Vhalf
*     /   \            |  \________|__|      |____|      L1        |    \/  \/   _|_
*    //\   \     |INN|_|-/  VG        ||                 100u      |              /Vhf\
*    \   \//     |___| |/   PWM       ||_-> MN1                    |  C1          \___/
*     \___/        |                     |          Freq = 9 K   __||__ 3u         _|_
*      _|_         |         RN      _/\  /\  /\_|    Z=5.8Ohms   ||  _|_          ///
*      ///         |            _|_    \/  \/   VN                   ///
*                  |            ///                   RFB
*                  |                                               |
*                  |____________________/\  /\  /\________________|
*                                          \/  \/
*
.OPTIONS  GMIN=1p       METHOD=trap   ABSTOL=1u     TEMP=27   srcsteps = 1  gminsteps = 1
.OPTIONS  RELTOL=.001   ABSTOL=1n     VNTOL=1u      ITL4=500  ITL1=400
*=========Create_Signal==================
VT        VT      0      DC      0      PWL(   0      0     1      1)
Vfreq     Vfreq   0      DC      100k
B_TRI     TRI     0      V =     acos( cos(6.283185*V(VFreq)*V(VT)) )/3.141592
B_OTA     VD      0      I       = -.3u*tanh((tanh(V(INP)-V(INN))*5)*1)
RB        VD      0      50meg
CCOMP     VD      0      50p
B_VD2     VD2     0      V       = .5*tanh(v(VD) )+.5
```

```
BVG         VG      0       V =     5*u( v(TRI) -v(VD2))
VCC         VCC     0       DC      5
RPP         VCC     VP      1u
RN          VN      0       1u
MN1         VOUT    VG      VN      0       NMOSC   W=90000u    L=1u
MP1         VOUT    VG      VP      VCC     PMOSC   W=90000u    L=1u
L1          VOUT    OUT     100u
C1          OUT     0       3u
Rout        OUT     Vhalf   5
Vhalf       Vhalf   0       2.5
RFB         OUT     INN     1K
RIN         VIN     INP     1K
ccc         out     vout    1000p
VIN         VIN     0       DC      0       SIN(    2.5     2.4     100       )

*=========The_CMOS_Model_Files=====================================
.model      NMOSC               NMOS(Level=  1  Cbs=2f Cbd=2f)
.model      PMOSC               PMOS(Level=  1  Cbs=2f Cbd=2f)
.model      DD                  D(      IS=3.15e-18 )

.control
*TRAN       TSTEP   TSTOP   TSTART TMAX    ?UIC?
tran        .1u     20m      0     .1u
plot        out     vin
.endc

.end
```

==========

This simulation is showing a unity gain Op Amp configuration connected as a buffer to a 100Hz sine wave. But the Open loop gain of this "Op Amp" is only 150. This is for stability purposes.

==========

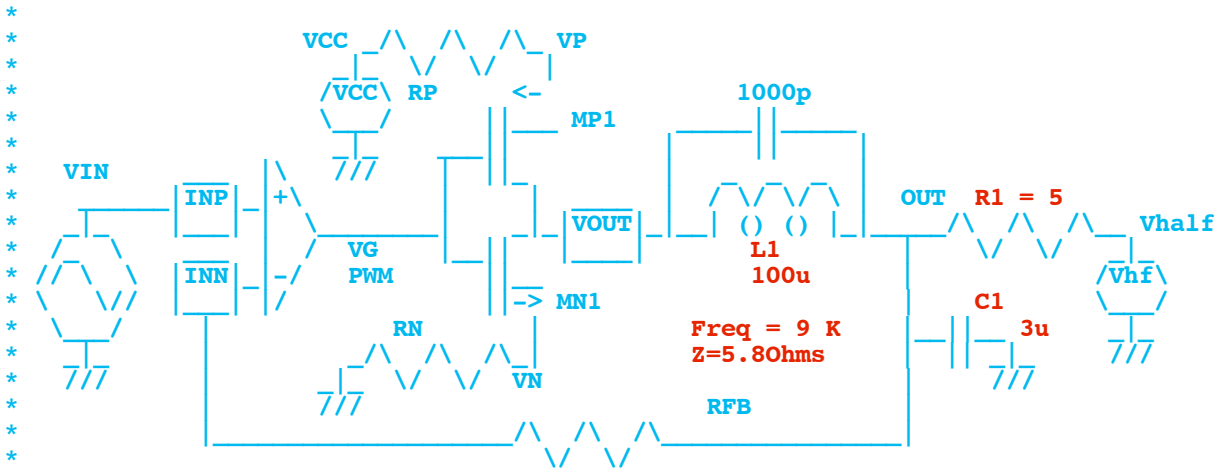


==========

What is making stability challenging is the fact that L1 at 100uH and C1 at 3uF are in the loop, and they provide two poles at 9kHz. The 5 Ohm value of RL is making those pole more real. But anyone who has designed Op Amps knows how adding open loop gain can make poles go complex

and migrate toward the right half plane.

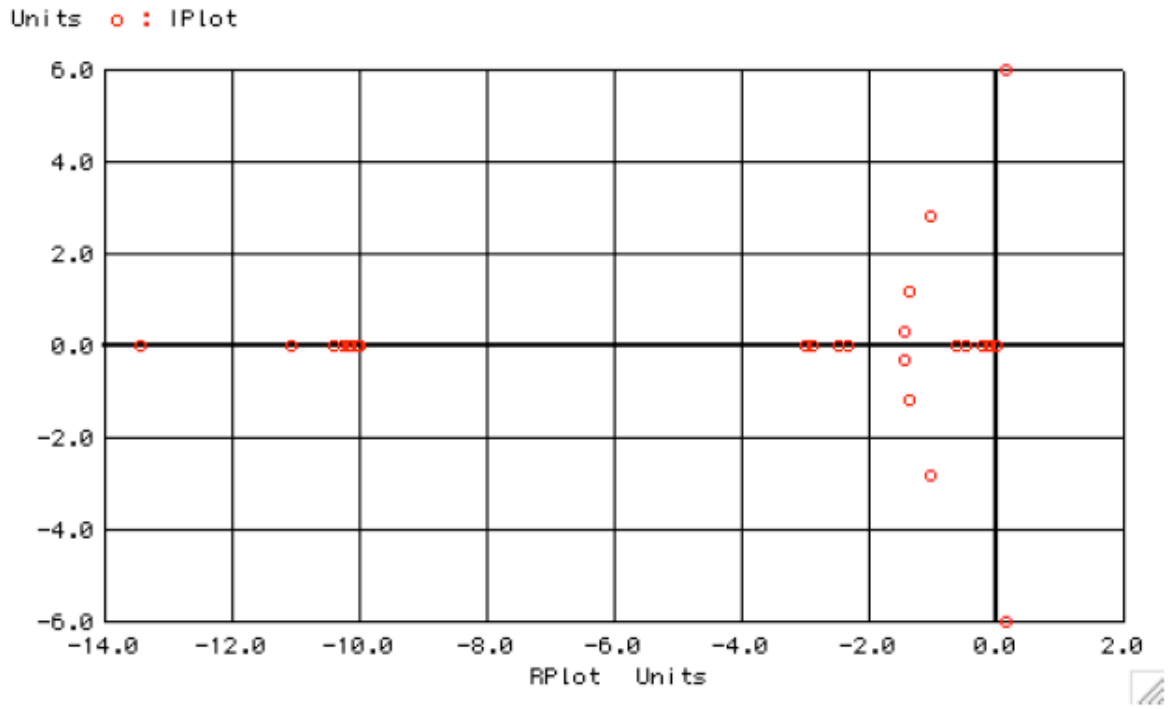
==========



==========

The root locus of a more common Op Amp is shown below. Adding open loop gain causes the two left most poles to come together, split into complex poles, and then migrate to the right side.

==========



A Root locus simulation has been done in MacSpice. It is online at the following site.

http://www.idea2ic.com/PlayWithSpice/pdf/RootLocusPlot.pdf

```
===========Full_Netlist_For_Copy_Paste=========================
CLASS_D_OpAmP_AC
*
*     ___
*    |INN|_|\  BOTA          RB
*    |___| |+\  _  _      VD
*          |  \/ \/ \_______/\  /\  /\____
*          |  /\_/\_/_|_  |   \/  \/    _|_
*     ___  |-/       ___  |  CCOMP      /VB \
*    |INP|_|/         |   |             \___/
*    |___| |          |   |               |
*          |_____    _|_  |  |\          _|_
*         _|_    |   ///  |  |+\         ///
*        /   \   |        |_ |  \    ___
*       /B_TRI\  |           |   \__|VG |  PWM output
*       \     /  |           |   /  |___|
*        \___/   |___________|-/ BVG
*         _|_                |/
*         ///
*............................................................
*
*                   VCC _/\  /\  /\_ VP
*                      _|_ \/  \/   |
*                     /VCC\ RP     <-          1000p
*                     \___/       ||___ MP1     _____||_____
*                      _|_     ___||_          |     ||     |
*   VIN               |\  ///     |  ||        |            |
*       _____ |INP|_|+\          |  |_   _    |   _  _  _  |  OUT  R1 = 5
*      _|_    |___| |  \_________|    |_|VOUT|_|__| / \/ \/ \ |_|_____/\  /\  /\__ Vhalf
*     /   \         |  /  VG     |___||  |____|     () ()   |     \/  \/      _|_
*    // \  \  |INN|_|-/   PWM        ||__          L1                |           /Vhf\
*    \   \//  |___| |/               ||-> MN1      100u              |   C1     \___/
*     \___/     |           RN            |                          |___||___ 3u  _|_
*      _|_      |        _/\  /\  /\_|        Freq = 9 K             |   ||  _|_   ///
*      ///      |       _|_ \/  \/   VN       Z=5.8Ohms              |       ///
*               |       ///                       RFB                |
*               |___________________/\  /\  /\______________________|
*                                     \/  \/
*
.OPTIONS  GMIN=1p      METHOD=trap   ABSTOL=1u     TEMP=27   srcsteps = 1  gminsteps = 1
.OPTIONS  RELTOL=.001  ABSTOL=1n     VNTOL=1u      ITL4=500  ITL1=400
*=========Create_Signal=================
VT        VT     0      DC     0      PWL(   0      0    1      1)
Vfreq     Vfreq  0      DC     100k
B_TRI     TRI    0      V =    acos( cos(6.283185*V(VFreq)*V(VT)) )/3.141592
B_OTA     VD     0      I      = -.3u*tanh((tanh(V(INP)-V(INN))*5)*1)
RB        VD     0      50meg
CCOMP     VD     0      50p
B_VD2     VD2    0      V      = .5*tanh(v(VD) )+.5
BVG       VG     0      V =    5*u( v(TRI) -v(VD2))
VCC       VCC    0      DC     5
RPP       VCC    VP     1u
RN        VN     0      1u
MN1       VOUT   VG     VN     0      NMOSC   W=90000u    L=1u
MP1       VOUT   VG     VP     VCC    PMOSC   W=90000u    L=1u
L1        VOUT   OUT    100u
C1        OUT    0      3u
Rout      OUT    Vhalf  5
Vhalf     Vhalf  0      2.5
RFB       OUT    INN    1K
RIN       VIN    INP    1K
ccc       out    vout   1000p
VIN       VIN    0      DC     0      SIN(   2.5    2.4   100      )

*=========The_CMOS_Model_Files==================================
.model    NMOSC              NMOS(Level=  1  Cbs=2f Cbd=2f)
.model    PMOSC              PMOS(Level=  1  Cbs=2f Cbd=2f)
.model    DD                 D(     IS=3.15e-18 )

.control
*TRAN     TSTEP  TSTOP  TSTART TMAX   ?UIC?
```

```
tran      .1u    20m     0     .1u
plot      out    vin
.endc

.end
```

9.16.10_1.23PM

dsauersanjose@aol.com
Don Sauer