*==========DUTY_CYCLE_RAMP_UP==========

Varying the duty cycle of a CMOS output stage and feeding it into an LRC network should produce a high power efficiency output power sources with a pretty linear duty cycle to output voltage relationship.

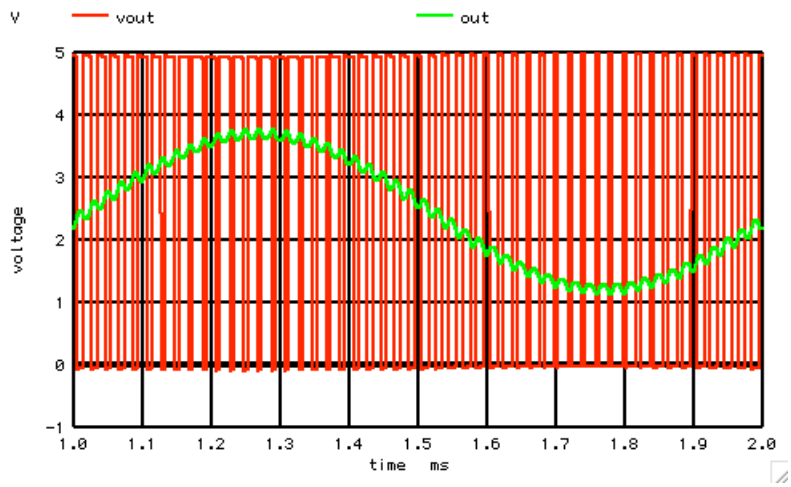
```
=====================================================================
CLASS_D_AC
*
*
*       VD                                          VCC  VP
*                                                     RP     <-
*                                                   VCC
*          T          TRI                                   MP1
*                                                   VOUT
*                                  Gate                          R1 = 5
*                                                   VG   OUT
*                                                         L1
*                                                         100u   C1
*                                                         MN1    3u
*                                                   RN   Freq = 9 K
*                                                        Z=5.8Ohms
*  PWL(0 0 1 1)  acos(cos(F*T))  5*u(v(TRI)-v(VD))   VN
*
*
.OPTIONS  GMIN=1f       METHOD=trap   ABSTOL=1u     TEMP=27   srcsteps = 1  gminsteps = 1
.OPTIONS  RELTOL=.001   ABSTOL=1n     VNTOL=1u      ITL4=500  ITL1=400
*=========Create_Signal==================
VT        VT     0      DC     0      PWL(   0      0    1      1)
Vfreq     Vfreq  0      DC     50k
*VD       VD     0      DC     .75
VD        VD     0      DC     0      SIN(   .5     .25    1k      )
VPI       VPI    0      DC     3.141592653589793
B_TRI     TRI    0      V =    acos( cos(6.283185*V(VFreq)*V(VT)) )/v(VPI)
BVG       VG     0      V =    5*u( v(TRI) -v(VD))
VCC       VCC    0      DC     5
RPP       VCC    VP     1u
RN        VN     0      1u
MN1       VOUT   VG     VN     0      NMOSC   W=90000u    L=1u
MP1       VOUT   VG     VP     VCC    PMOSC   W=90000u    L=1u
L1        VOUT   OUT    100u
C1        OUT    0      3u
Rout      OUT    0      5
Vrout     Vrout  0      5

*=========The_CMOS_Model_Files=================================
.model    NMOSC              NMOS(Level=  1  Cbs=2f Cbd=2f)
.model    PMOSC              PMOS(Level=  1  Cbs=2f Cbd=2f)

.control
*TRAN     TSTEP  TSTOP  TSTART TMAX   ?UIC?
tran      .1u    2m     1m      .1u


.endc
.end
=====================================================================
```

Such an output stage in audio is called a class D output stage. Linear audio power amplifiers all require heats sinks since they are usually wasteful in power. But Class D output stages use output transistors as switches such that they draw little power when they are either on or off.

```
=====================================================================
CLASS_D_AC
*
*
*        VD                                          VCC  VP
*                                                      RP
*                                                      MP1
*          T          TRI                              VOUT
*                                Gate                   R1 = 5
*                                 VG                    OUT
*                                                       L1
*                                                       100u
*                                                       C1
*                                                       3u
*                                                       MN1
*                                                       Freq = 9 K
*                                                       Z=5.8Ohms
*                                                       RN
*                                                       VN
*  PWL(0 0 1 1)  acos(cos(F*T))  5*u(v(TRI)-v(VD))
*
```

This example shows one end of RL going to ground. It is more common in audio to connect RL up to another class D output stage in a bridge configuration. So when one side of RL swings high, the other side swings equally low. An a rather large amount of audio power can be outputted without wasting a lot of heat.

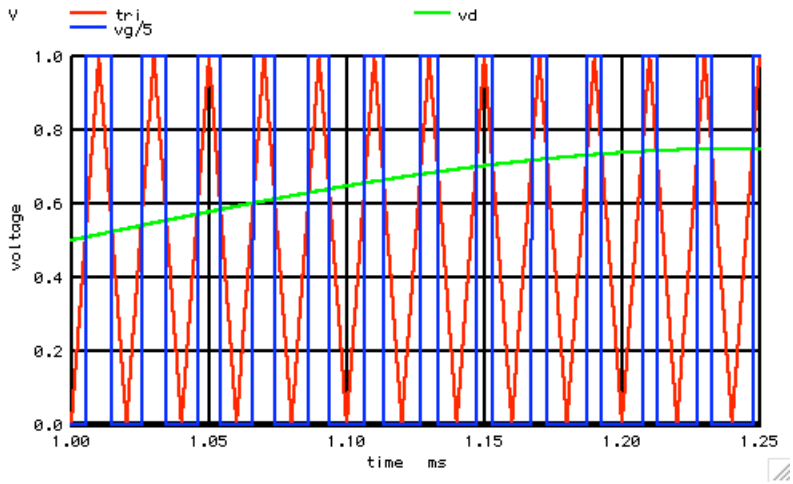
```
=====================================================================
plot      vout out
```




```
=====================================================================
CLASS_D_AC
*
*
*        VD                                          VCC  VP
*                                                      RP
*                                                      MP1
*          T          TRI                              VOUT
*                                Gate                   R1 = 5
*                                 VG                    OUT
*                                                       L1
*                                                       100u
*                                                       C1
*                                                       3u
*                                                       MN1
*                                                       Freq = 9 K
*                                                       Z=5.8Ohms
*                                                       RN
*                                                       VN
*  PWL(0 0 1 1)  acos(cos(F*T))  5*u(v(TRI)-v(VD))
```

This simulation is supplying a triangle wave to a comparator and a sine wave to the other side to produce the duty cycle modulation.

```
=====================================================================
plot      tri vd  vg/5 xlimit 1m 1.25m
```




```
============Full_Netlist_For_Copy_Paste=======================
CLASS_D_AC
*
*
*        VD                                          VCC  /\   /\   /\  VP
*                                                        \/   \/   \/
*                                                     /VCC\ RP      <-
*          /       \  /\  /        __  ____  _       \___/        MP1
*         /         \/  \/                                        ///
*           T          TRI          |_|    |_|                    VOUT
*                                                  Gate                    /\/\/\/\          R1 = 5
*                                                                   VG     ()  ()   OUT   /\   /\   /\
*       B_TRI                                                                L1                \/   \/
*                                                                            100u              C1        ///
*                                                                                   -> MN1        3u
*                                                  -/ BVG                RN        Freq = 9 K
*                                                                                   Z=5.8Ohms        ///
*                                                                                   VN
*  PWL(0 0 1 1)  acos(cos(F*T))  5*u(v(TRI)-v(VD))   ///
*
*
.OPTIONS  GMIN=1f       METHOD=trap   ABSTOL=1u     TEMP=27   srcsteps = 1  gminsteps = 1
.OPTIONS  RELTOL=.001   ABSTOL=1n     VNTOL=1u      ITL4=500  ITL1=400
*=========Create_Signal==================
VT        VT     0      DC     0      PWL(   0      0    1      1)
Vfreq     Vfreq  0      DC     50k
*VD       VD     0      DC     .75
VD        VD     0      DC     0      SIN(   .5     .25    1k      )
VPI       VPI    0      DC     3.141592653589793
B_TRI     TRI    0      V =    acos( cos(6.283185*V(VFreq)*V(VT)) )/v(VPI)
BVG       VG     0      V =    5*u( v(TRI) -v(VD))
VCC       VCC    0      DC     5
RPP       VCC    VP     1u
RN        VN     0      1u
MN1       VOUT   VG     VN     0      NMOSC   W=90000u    L=1u
MP1       VOUT   VG     VP     VCC    PMOSC   W=90000u    L=1u
L1        VOUT   OUT    100u
C1        OUT    0      3u
Rout      OUT    0      5
Vrout     Vrout  0      5
*=========The_CMOS_Model_Files=================================
.model    NMOSC                NMOS(Level=  1  Cbs=2f Cbd=2f)
.model    PMOSC                PMOS(Level=  1  Cbs=2f Cbd=2f)

.control
*TRAN     TSTEP  TSTOP  TSTART TMAX   ?UIC?
tran      .1u    2m     1m      .1u
plot      vout out
plot      tri vd  vg/5 xlimit 1m 1.25m

.endc

.end
```

9.16.10_1.10PM
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