Cables, Connectors and Performance Testing

Chapter 5

5.0.0 CABLES, CONNECTORS AND PERFORMANCE TESTING

5.1.0 GENERAL COMMENTS

When choosing cables and connectors for LVDS it is important to remember:

1. Use controlled impedance media. The cables and connectors you use should have a differential impedance of about 100Ω. They should not introduce major impedance discontinuities that cause signal reflections.

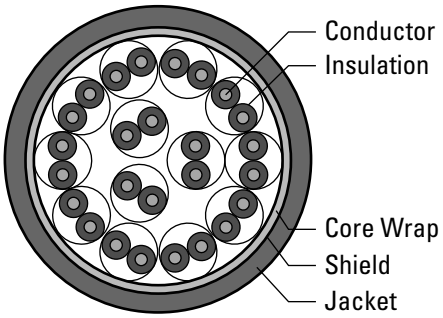
2. Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable, multi-conductor) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential-mode) noise, which is rejected by the receiver.

3. For cable distances < 0.5m, most cables can be made to work effectively. For distances 0.5m < d < 10m, CAT 3 (Category 3) twisted pair cable works well and is readily available and relatively inexpensive. Other types of cables may also be used as required by a specific application. This includes twin-ax cables built from separate pairs and ribbon style constructions, which are then coiled.

5.2.0 CABLING SUGGESTIONS

As described above, try to use balanced cables (twisted pair, twin-ax, or flex circuit with closely coupled differential traces). LVDS was intended to be used on a wide variety of media. The exact media is not specified in the LVDS Standard, as it is intended to be specified in the referencing standard that specifies the complete interface. This includes the media, data rate, length, connector, function, and pin assignments. In some applications that are very short (< 0.3m), ribbon cable or flex circuit may be acceptable. In box-to-box applications, a twisted pair or twin-ax cable would be a better option due to robustness, shielding and balance. Whatever cable you do choose, following the suggestions below will help you achieve optimal results.

5.2.1 Twisted Pair



Drawing of Twisted Pair Cable, Cross-Section

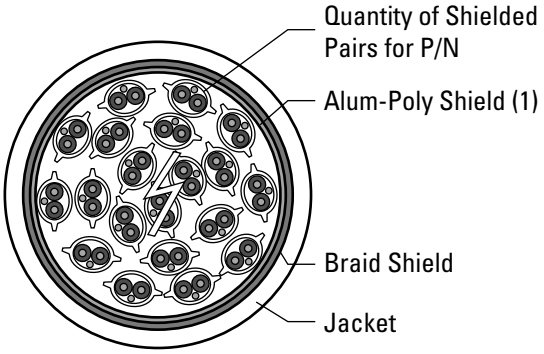
Twisted pair cables provide a good, low cost solution with good balance, are flexible, and capable of medium to long runs depending upon the application skew budget. It is offered with an overall shield or with shields around each pair as well as an overall shield. Installing connectors is more difficult due to its construction.

a) Twisted pair is a good choice for LVDS. Category 3 (CAT3) cable is good for runs up to about 10m, while CAT5 has been used for longer runs.

b) For the lowest skew, group skew-dependent pairs together (in the same ring to minimize skew between pairs).

c) Ground and/or terminate unused conductors (do not float).

5.2.2 Twin-ax Cables



Drawing of Individually Shielded Parallel Pair Twin-ax Cable - Cross Section

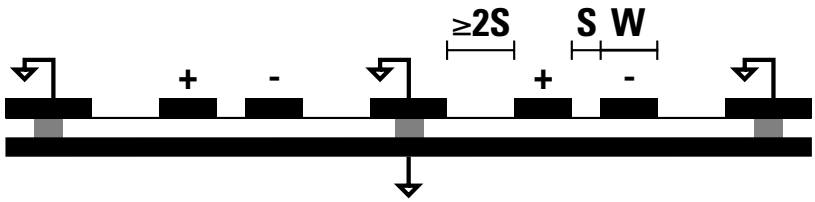
Twin-ax cables are flexible, have low skew and shields around each pair for isolation. Since they are not twisted, they tend to have very low skew within a pair and between pairs. These cables are for long runs and have been commonly deployed in Channel Link and FPD-Link applications.

a) Drain wires per pair may be connected together in the connector header to reduce pin count.

b) Ground and/or terminate unused conductors.

5.2.3 Flex Circuit

Flex circuit is a good choice for very short runs, but it is difficult to shield. It can be used as an interconnect between boards within a system.



Flex Circuit - Cross-Section

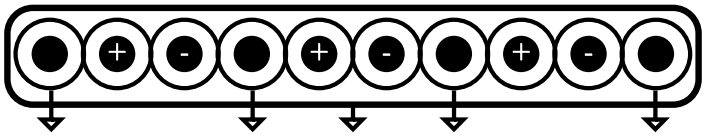
a) Closely couple the members of differential pairs (S < W). Do not run signal pairs near the edges of the cable, as these are not balanced.

b) Use a ground plane to establish the impedance.

c) Use ground shield traces between the pairs if there is room. Connect these ground traces to the ground plane through vias at frequent intervals.

5.2.4 Ribbon Cable

Ribbon cable is cheap and is easy to use and shield. Ribbon cable is not well suited for high-speed differential signaling (good coupling is difficult to achieve), but it is OK for very short runs.



Flat Cable - Cross-Section

a) If ribbon cable must be used, separate the pairs with ground wires. Do not run signal pairs at the edges of the ribbon cable.

b) Use shielded cable if possible, shielded flat cable is available.

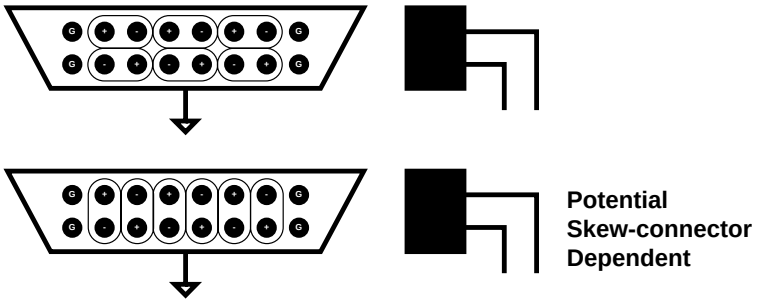
5.2.5 Additional Cable Information

Additional information on cable construction may be found in National Application Note AN-916. Also, many cable, connector and interconnect system companies provide detailed information on their respective websites about different cable options. A non-inclusive list of a few different options is provided below:

3M	**www.3M.com/interconnects/**
Spectra-Strip Cable Products	**www.spectra-strip.amphenol.com/default.CFM**
AMP	**http://connect.amp.com/**

5.2.6 Connectors

Connectors are also application dependent and depend upon the cable system being used, the number of pins, the need for shielding and other mechanical footprint concerns. Standard connectors have been used at low to medium data rates, and optimized low skew connectors have been developed for medium to high-speed applications.



Typical Connector Pinouts

a) Choose low skew, impedance matching connectors if possible.

b) Group members of each pair together. Pins of a pair should be close together (adjacent) not separated from each other. This is done to maintain balance, and to help ensure that external noise, if picked up, will be common-mode and not differential in nature.

c) Some connectors have different length leads for different pins. Group pairs on same length leads. Consult the connector manufacturer for the orientation of pins that yield the lowest skew and crosstalk for your particular connector. Shorter pin lengths tend to be better than long ones, minimize this distance if possible.

d) Place ground pins between pairs where possible and convenient. Especially use ground pins to separate TTL/CMOS signals for LVDS signals.

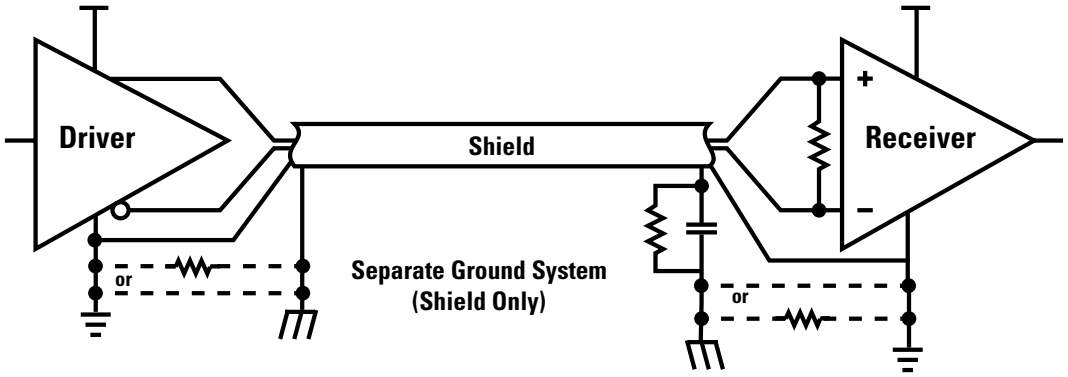
e) Ground end pins. Do not use end pins for high-speed signals, if possible, as they offer less balance.

f) Ground and/or terminate unused pins.

Many different connector options exist. One such cable-connector system that has been used for LVDS with great results is the 3M "High-speed MDR Digital Data Transmission System." This cable system is featured on the National Channel-Link (48-bit) and LDI Evaluation Kits. The connector is offered in a surface mount option that has very small skew between all the pins. Different cable types are also supported.

5.3.0 CABLE GROUND AND SHIELD CONNECTIONS

In many systems, cable shielding is required for EMC compliance. Although LVDS provides benefits of low EMI when used properly, shielding is still usually a good idea especially for box-to-box applications. Together, cable shielding and ground return wires help reduce EMI. The shielding contains the EMI and the ground return wire (the pair shield or drain wire in some cables) and provides a small loop area return path for common-mode currents. Typically one or more pairs are assigned to ground (circuit common). Using one or more pair reduces the DCR (DC Resistance) of the path by the parallel connection of the conductors. This provides a known, very low impedance return path for common-mode currents.



Typical Grounding Scheme

In most applications the grounding system will be common to both the receiver and the driver. The cable shield is connected at one end with a DC connection to the common ground (frame ground). Avoid "pig-tail" (high inductance) ground wiring from the cable. The other end of the shield is typically connected with a capacitor or network of a capacitor and a resistor as shown in the above example. This prevents DC current flow in the shield. In the case where connectors are involved that penetrate the system's enclosure, the cable shield must have a circumferential contact to the connector's conductive backshell to provide an effective shield and must make good contact.

Note: It is beyond the scope of this book to effectively deal with cabling and grounding systems in detail. Please consult other texts on this subject and be sure to follow applicable safety and legal requirements for cabling, shielding and grounding.

5.4.0 LVDS SIGNAL QUALITY

Signal quality may be measured by a variety of means. Common methods are:

- Measuring rise time at the load
- Measuring Jitter in an Eye Pattern
- Bit Error Rate Testing
- Other means

Eye Patterns and Bit Error Rate Testing (BERT) are commonly used to determine signal quality. These two methods are described next.

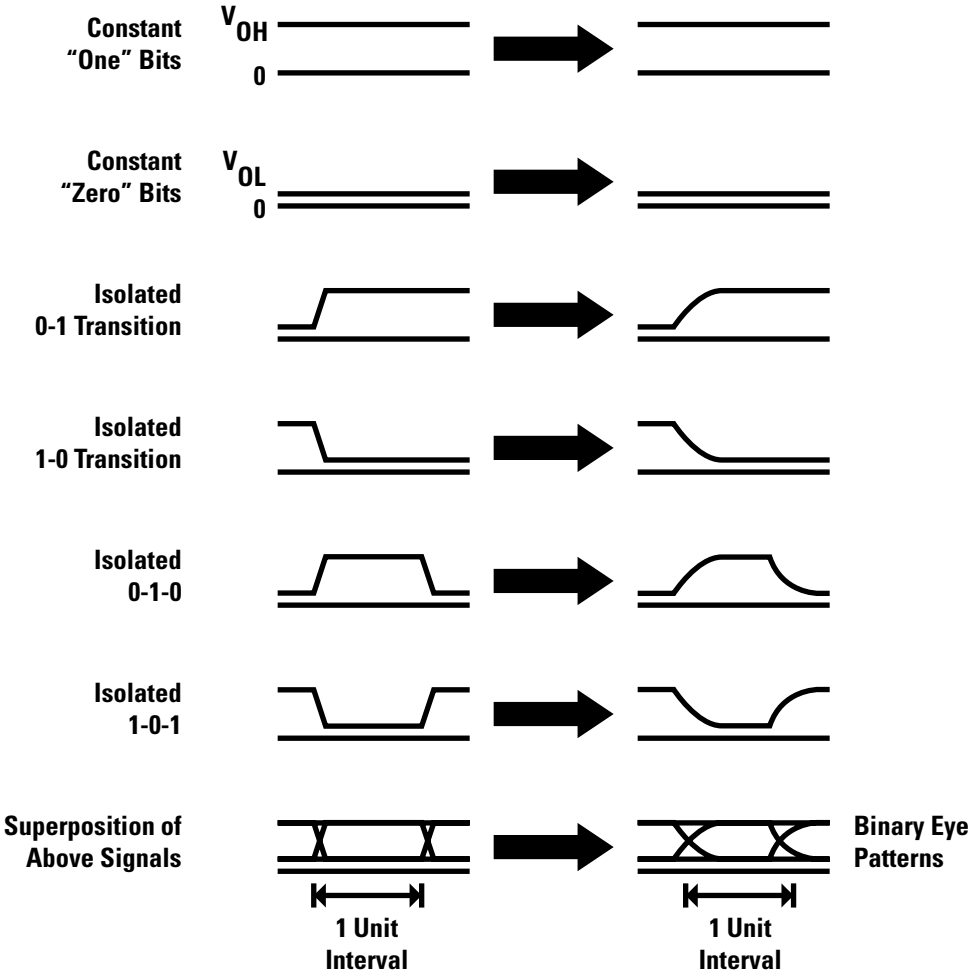
5.4.1 LVDS Signal Quality: Jitter Measurements Using Eye Patterns

This report provides an example of a data rate versus cable length curve for LVDS drivers and receivers in a typical application for a particular twisted pair cable. The questions of: "How Far?" and "How Fast?" seem simple to answer at first, but after detailed study, their answers become quite complex. This is not a simple device parameter specification. But rather, a system level question where a number of other parameters besides the switching characteristics of the drivers and receivers must be known. This includes the measurement criteria for signal quality that has been selected, and also the pulse coding that will be used (NRZ for example). Additionally, other system level components should be known too. This includes details about cables, connectors, and the printed circuit boards (PCB). Since the purpose is to measure signal quality, it should be done in a test fixture that closely matches the end environment — or even better — in the actual application. Eye pattern measurements are useful in measuring the amount of jitter versus the unit internal to establish the data rate versus cable length curves and therefore are a very accurate way to measure the expected signal quality in the end application.

5.4.2 Why Eye Patterns?

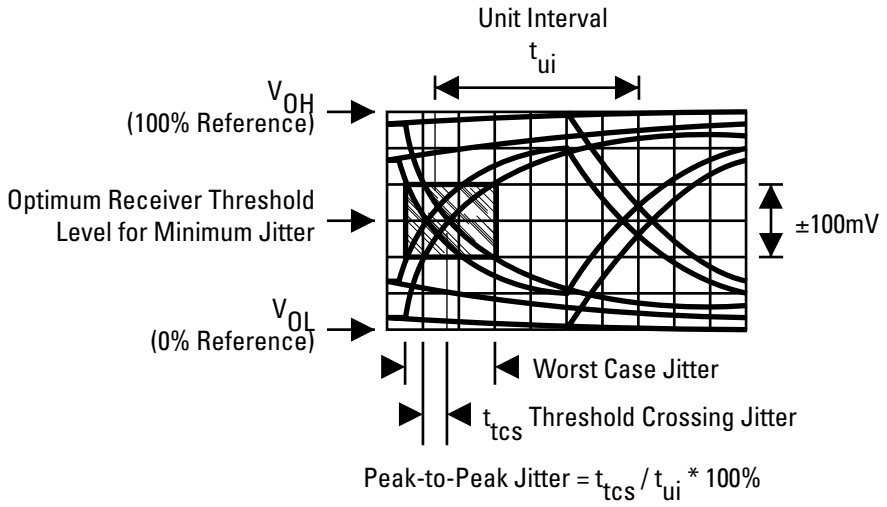
The eye pattern is used to measure the effects of inter-symbol interference on random data being transmitted through a particular medium. The prior data bits effect the transition time of the signal. This is especially true for NRZ data that does not guarantee transitions on the line. For example in NRZ coding, a transition high after a long series of lows has a slower rise time than the rise time of a periodic (010101) waveform. This is due to the low pass filter effects of the cable. The next figure illustrates the superposition of six different data patterns. Overlaid, they form the eye pattern that is the input to the cable. The right hand side of this figure illustrates the same pattern at the end of the cable. Note the rounding of the formerly sharp transitions. The width of the crossing point is now wider and the opening of the eye is also now smaller (see application note AN-808 for an extensive discussion on eye patterns).

When line drivers (generators) are supplying symmetrical signals to clock leads, the period of the clock, rather than the unit interval of the clock waveform, should be used to determine the maximum cable lengths (e.g., though the clock rate is twice the data rate, the same maximum cable length limits apply). This is due to the fact that a periodic waveform is not prone to distortion from inter-symbol distortion as is a data line.



Formation of an Eye Pattern by Superposition.

The figure below describes the measurement locations for minimum jitter. Peak-to-Peak Jitter is the width of the signal crossing the optimal receiver thresholds. For a differential receiver, that would correspond to 0V (differential). However, the receiver is specified to switch between –100mV and +100mV. Therefore for a worse case jitter measurement, a box should be drawn between ±100mV and the jitter measured between the first and last crossing at ±100mV. If the vertical axis units in the figure were 100mV/division, the worse case jitter is at ±100mV levels.



NRZ Data Eye Pattern.

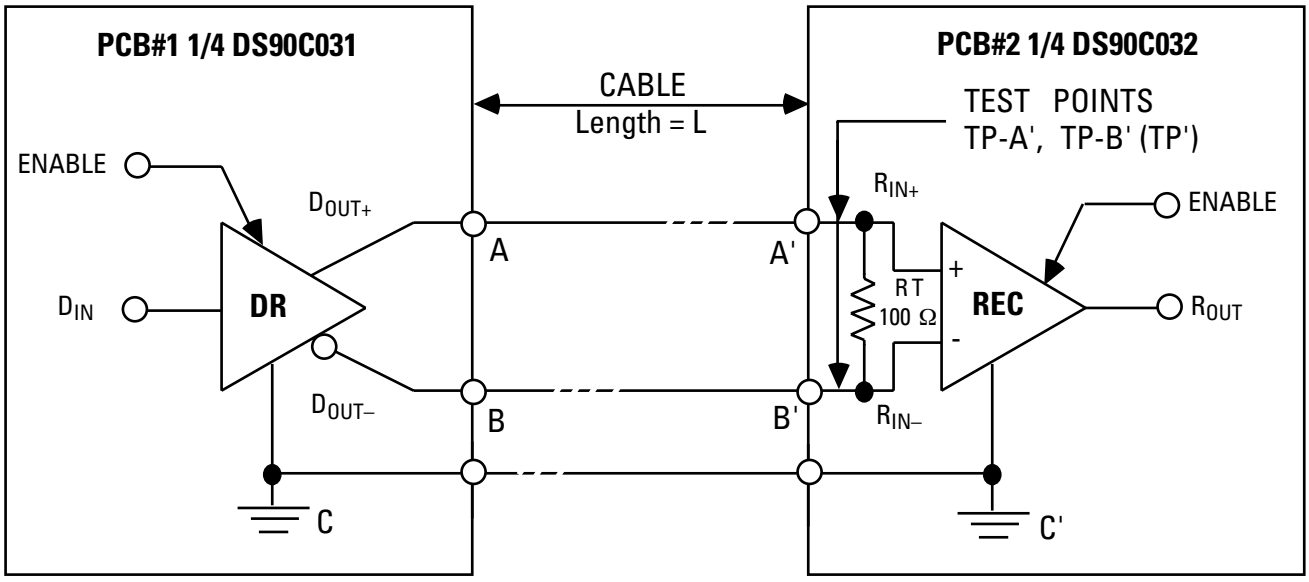
5.4.3 Eye Pattern Test Circuit

LVDS drivers and receivers are typically used in an uncomplicated point-to-point configuration as shown in the figure below. This figure details the test circuit that was used to acquire the Eye pattern measurements. It includes the following components:

PCB#1: DS90C031 LVDS Quad Driver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector.

Cable: The cable used for this testing was Berk-Tek part number 271211. This is a 105Ω (Differential-mode) 28 AWG stranded twisted pair cable (25 Pair with overall shield) commonly used on SCSI applications. This cable represents a common data interface cable. For this test report, the following cable lengths were tested: 1, 2, 3, 5, and 10 meter(s). Cables longer that 10 meters were not tested, but may be employed at lower data rates.

PCB#2: DS90C032 LVDS Quad Receiver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector. A 100Ω surface mount resistor was used to terminate the cable at the receiver input pins.



LVDS Signal Quality Test Circuit

5.4.4 Test Procedure

A pseudo-random (PRBS) generator was connected to the driver input, and the resulting eye pattern (measured differentially at TP') was observed on the oscilloscope. Different cable lengths (L) were tested, and the frequency of the input signal was increased until the measured jitter equaled 20% with respect to the unit interval for the particular cable length. The coding scheme used was NRZ. Jitter was measured twice at two different voltage points. Jitter was first measured at the 0V differential voltage (optimal receiver threshold point) for minimum jitter, and second at the maximum receiver threshold points (±100mV) to obtain the worst case or maximum jitter at the receiver thresholds. Occasionally jitter is measured at the crossing point alone and although this will result in a much lower jitter point, it ignores the fact that the receivers may not switch at that very point. For this reason, this signal quality test report measured jitter at both points.

5.4.5 Results and Data Points

20% Jitter Table @ 0V Differential (Minimum Jitter)

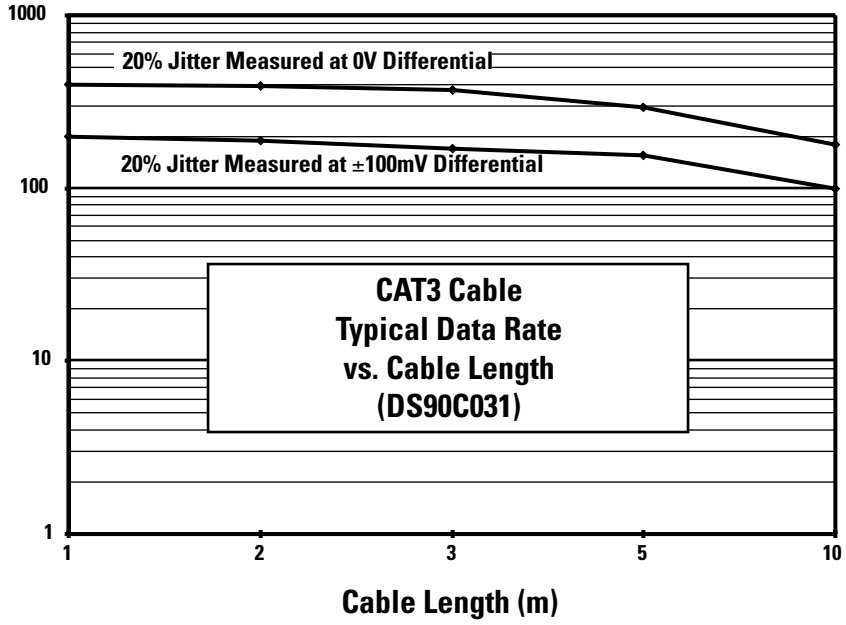
Cable Length (m)	Data Rate (Mbps)	Unit Interval (ns)	Jitter (ns)
1	400	2.500	0.490
2	391	2.555	0.520
3	370	2.703	0.524
5	295	3.390	0.680
10	180	5.550	1.160

As described above, Jitter was measured at the 0V differential point. For the case with the 1 meter cable, 490ps of jitter at 400Mbps was measured, and with the 10 meter cable, 1.160ns of jitter at 180Mbps was measured.

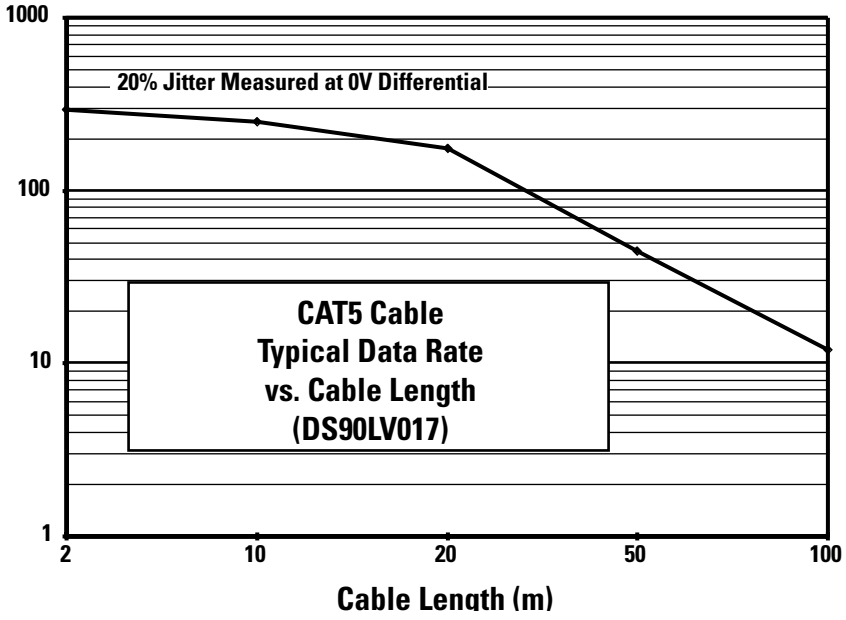
20% Jitter Table @ ±100 mV (Maximum Jitter)

Cable Length (m)	Data Rate (Mbps)	Unit Interval (ns)	Jitter (ns)
1	200	5.000	1.000
2	190	5.263	1.053
3	170	5.882	1.176
5	155.5	6.431	1.286
10	100	10.000	2.000

The second case measured jitter between ±100mV levels. For the 1 meter cable, 1ns of jitter was measured at 200Mbps, and for the 10 meter cable, 2ns of jitter occurred at 100Mbps.



Typical Data Rate vs Cable Length for 0-10m CAT3 Cable



Typical Data Rate vs Cable Length for 2-100m CAT5 Cable (See AN-1088)

Care should be taken in long cable applications using LVDS. When directly coupled, LVDS provides up to ±1V common-mode rejection. Long cable applications may require larger common-mode support. If this is the case, transformer coupling or alternate technologies (such as RS-485) should be considered.

The figures above are a graphical representation of the relationship between data rate and cable length for the application under test. Both curves assume a maximum allotment of 20% jitter with respect to the unit interval. Basically, data rates between 200-400 Mbps are possible at shorter lengths, and rates of 100-200Mbps are possible at 10 meters. Note that employing a different coding scheme, cable, wire gauge (AWG), etc. will create a different relationship between maximum data rate versus cable length. Designers are greatly encouraged to experiment on their own.

5.4.6 Additional Data on Jitter & Eye Patterns

For additional information on LVDS "Data Rate vs Cable Length" please consult the list of LVDS application notes on the LVDS web site at: **www.national.com/appinfo/lvds/**

At this time of this printing the following application notes were available:

AN#	Devices Tested
AN-977	DS90C031/032
AN-1088	DS90LV017/027, DS92LV010A

5.4.7 Conclusions – Eye Pattern Testing

Eye patterns provide a useful tool to analyze jitter and the resulting signal quality as it captures the effects of a random data pattern. They provide a method to determine the maximum cable length for a given data rate or vice versa. Different systems, however, can tolerate different levels of jitter. Commonly 5%, 10%, or 20% is acceptable with 20% jitter usually being an upper practical limit. More than 20% jitter tends to close down the eye opening, making error-free recovery of NRZ data more difficult. This report illustrates data rate versus distance for a common, inexpensive type of cable.

5.5.0 BIT ERROR RATE (BER) TESTING

Bit error rate testing is another approach to determine signal quality. This test method is described next.

5.5.1 LVDS Cable Driving Performance using BERT

The questions of: "How Far?" and "How Fast?" seem simple to answer at first, but after detailed study, their answers become quite complex. This is not a simple device parameter specification. But rather, a system level question, and to be answered correctly a number of other parameters besides the switching characteristics of the drivers and receivers must be known. This includes the measurement criteria for signal quality that has been selected, and the pulse coding that will be used (Non-Return to Zero (NRZ) for example — see application note AN-808 for more information about coding). Additionally, other system level components should be known too. This includes details about the cable, connector and information about the printed circuit boards (PCB). Since the purpose is to measure signal quality/performance, it should be done in a test fixture that matches the end environment precisely if possible. The actual application would be best if possible. There are numerous methods to measure signal quality, including eye pattern (jitter) measurements and Bit Error Rate tests (BER).

This report provides the results of a series of Bit Error Rate tests performed on the DS90C031/032 LVDS Quad Line driver/receiver devices. The results can be generalized to other National LVDS products. Four drivers were used to drive 1 to 5 meters of standard twisted pair cables at selected data rates. Four receivers were used to recover the data at the load end of the cable.

5.5.2 What is a BER Test?

Bit Error Rate testing is one way to measure of the performance of a communications system. The standard equation for a bit error rate measurement is:

Bit Error Rate = (Number of Bit errors)/(Total Number of Bits)

Common measurement points are bit error rates of:

$\leq 1 \times 10^{-12}$ => One or less errors in 1 trillion bits sent

$\leq 1 \times 10^{-14}$ => One or less errors in 100 trillion bits sent

Note that BER testing is time intensive. The time length of the test is determined by the data rate and also the desired performance benchmark. For example, if the data rate is 50Mbps, and the benchmark is an error rate of 1×10^{-14} or better, a run time of 2,000,000 seconds is required for a serial channel. 2,000,000 seconds equates to 555.6 hours or 23.15 days!

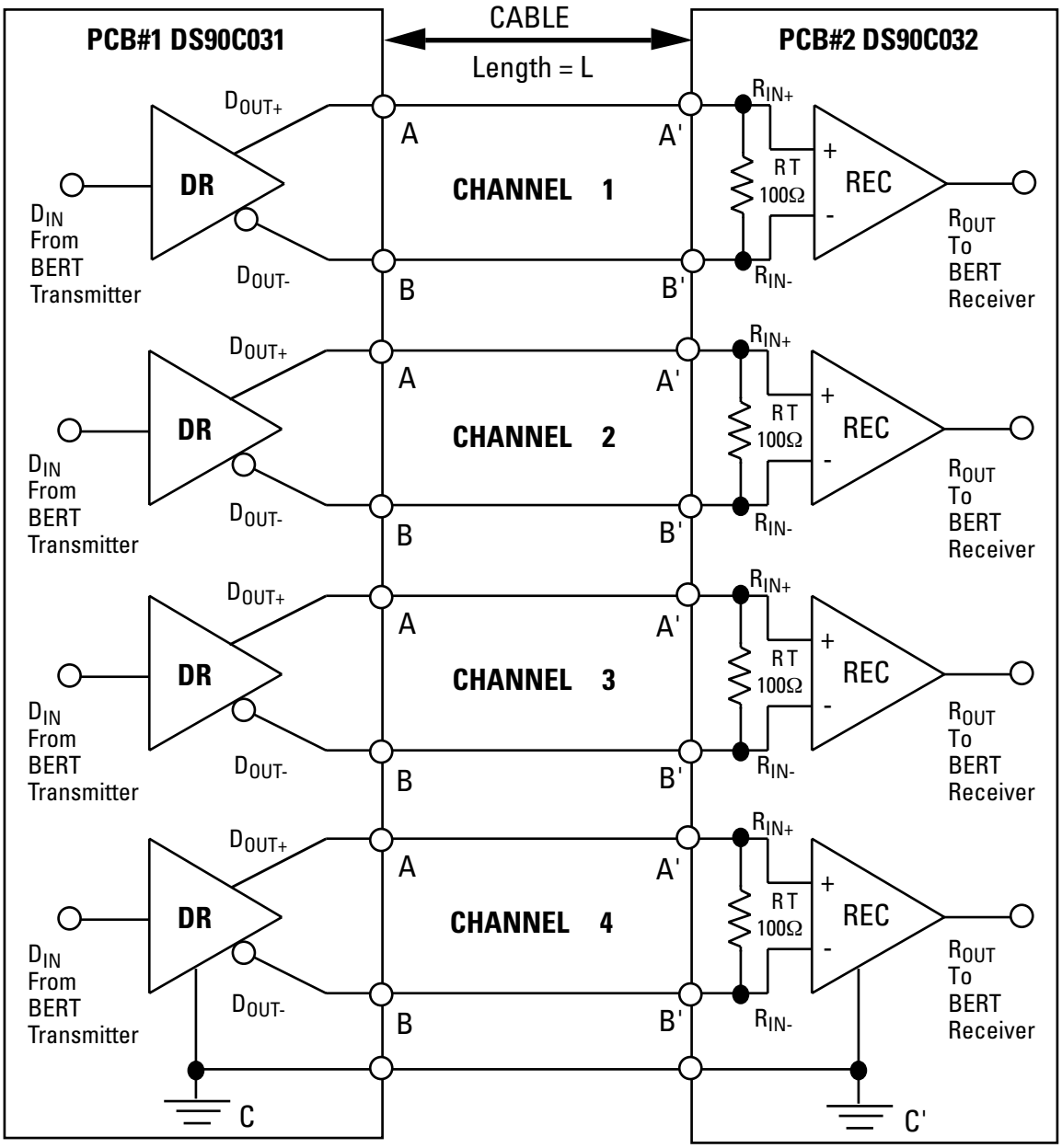
5.5.3 BER Test Circuit

LVDS drivers and receivers are typically used in an uncomplicated point-to-point configuration as shown in the next figure. This figure details the test circuit that was used. It includes the following components:

PCB#1: DS90C031 LVDS Quad Driver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector.

Cable: Cable used for this testing was Berk-Tek part number 271211. This is a 105Ω (Differential-mode) 28 AWG stranded twisted pair cable (25 Pair with overall shied) commonly used in SCSI applications. This cable represents a common data interface cable. For this test report, cable lengths of 1 and 5 meters were tested.

PCB#2: DS90C032 LVDS Quad Receiver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector. A 100Ω surface mount resistor was used to terminate the cable at the receiver input pins.



LVDS BER Test Circuit

5.5.4 Test Procedure

A parallel high-speed BER transmitter/receiver set (Tektronix MultiBERT-100) was employed for the tests. The transmitter was connected to the driver inputs, and the receiver outputs were connected to the BERT receiver inputs. Different cable lengths and data rates were tested. The BER tester was configured to provide a PRBS (Pseudo Random Bit Sequence) of 2^{15}-1 (32,767 bit long sequence). In the first test, the same input signal was applied to all four of the LVDS channels under test. For the other tests, the PRBS was offset by 4-bits, thus providing a random sequence between channels. The coding scheme used was NRZ. Upon system test configuration, the test was allowed to run uninterrupted for a set amount of time. At completion of the time block, the results were recorded which included: elapsed seconds, total bits transmitted and number of bit errors recorded. For the three tests documented next, a power supply voltage of +5.0V was used and the tests were conducted at room temperature.

5.5.5 Tests and Results

The goal of the tests was to demonstrate errors rates of less than 1×10^{-12} are obtainable.

TEST #1 Conditions:

Data Rate = 50Mbps
Cable Length = 1 meter
PRBS Code = 2^{15}-1 NRZ

For this test, the PRBS code applied to the four driver inputs was identical. This created a "simultaneous output switching" condition on the device.

TEST #1 Results:

Total Seconds: 87,085 (1 day)
Total Bits: $1{,}723 \times 10^{13}$
Errors = 0
Error Rate = $< 1 \times 10^{-12}$

TEST #2 Conditions:

Data Rate = 100Mbps
Cable Length = 1 meter
PRBS Code = 2^{15}-1 NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

TEST #2 Results:

Total Seconds: 10,717 (~3 hr.)
Total Bits: 4.38×10^{12}
Errors = 0
Error Rate = $< 1 \times 10^{-12}$

TEST #3 Conditions:

Data Rate = 100Mbps
Cable Length = 5 meter
PRBS Code = 2^{15}-1 NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

TEST #3 Results:

Total Seconds: 10,050 (~2.8 hr.)
Total Bits: 4×10^{12}
Errors = 0
Error Rate = $< 1 \times 10^{-12}$

5.5.6 Conclusions - BERT

All three of the tests ran error free and demonstrate extremely low bit error rates using LVDS technology. The tests concluded that error rates of $< 1 \times 10^{-12}$ can be obtained at 100Mbps operation across 5 meters of twisted pair cable. BER tests only provide a "Go — No Go" data point if zero errors are detected. It is recommended to conduct further tests to determine the point of failure (data errors). This will yield important data that indicates the amount of margin in the system. This was done in the tests conducted by increasing the cable length from 1 meter to 5 meters, and also adjusting the data rate from 50Mbps to 100Mbps. Additionally, bench checks were made while adjusting the power supply voltage from 5.0V to 4.5V and 5.5V, adjusting clock frequency, and by applying heat/cold to the device under test (DUT). No errors were detected during these checks (tests were checks only and were not conducted over time, i.e. 24 hours). BER tests conclude that the PRBS patterns were transmitted error free across the link. This was concluded by applying a pattern to the input and monitoring the receiver output signal.

NOTES

LVDS Reference

Chapter 8

8.0.0 LVDS REFERENCE – APPLICATION NOTES, STANDARDS, WHITE PAPERS, MODELING INFORMATION AND OTHER DESIGN GUIDES

8.1.0 NATIONAL DOCUMENTS

National also offers more in depth application material on LVDS in the form of application notes, conference papers, white papers and other documents. Please visit the LVDS website for the viewing or downloading of documents. The website's URL is: **www.national.com/appinfo/lvds/**

8.1.1 National LVDS Application Notes

The following application notes on LVDS are currently available:

AN-Number	Topic	Parts Referenced
AN-971	Introduction to LVDS	DS90C031/DS90C032
AN-977	Signal Quality – Eye Patterns	DS90C031
AN-1040	Bit Error Rate Testing	DS90C031/DS90C032
AN-1041	Introduction to Channel Link	DS90CR2xx
AN-1059	Timing (RSKM) Information	DS90CRxxx
AN-1060	LVDS - Megabits @ milliwatts (EDN Reprint)	
AN-1084	Parallel Application of Link Chips	DS90Cxxx
AN-1088	Bus LVDS/LVDS Signal Quality	DS90LV017/27, DS92LV010A
AN-1108	PCB and Interconnect Design Guidelines	DS90CR2xx
AN-1109	Multidrop Application of Channel Links	DS90CR2xx
AN-1110	Power Dissipation of LVDS Drivers and Receivers	DS90C031/2, DS90LV031A/32A
AN-1115	Bus LVDS and DS92LV010A XCVR	DS92LV010A
AN-1123	Sorting Out Backplane Driver Alphabet Soup	

8.1.2 National Application Notes on Generic Data Transmission Topics

National also offers many application notes devoted to the general topics of data transmission, PCB design and other topics pertaining to Interface. A few of these are highlighted below.

AN-Number	Topic
AN-216	An Overview of Selected Industry Interface Standards
AN-643	EMI/RFI Board Design
AN-806	Data Transmission Lines and Their Characteristics
AN-807	Reflections: Computations and Waveforms
AN-808	Long Transmission Lines and Data Signal Quality
AN-912	Common Data Transmission Parameters and their Definitions
AN-916	A Practical Guide to Cable Selection
AN-972	Inter-Operation of Interface Standards
AN-1111	An Introduction to IBIS Modeling

A complete list of all application notes is located at: **http:www.national.com/apnotes/apnotes_all_1.html**

8.1.3 National Application Notes on Flat Panel Display Link/LVDS Display Interface

A series of application notes is available on the FPD-Link and LDI chipsets. Please see the FPD website for a list of application notes that are currently available at:

www.national.com/appinfo/fpd/

8.1.4 Conference Papers/White Papers from National

The following conference papers are currently available from the LVDS website at:

www.national.com/appinfo/lvds/

- **BLVDS White Paper**
  Signal Integrity and Validation of Bus LVDS (BLVDS) Technology in Heavily Loaded Backplanes.
  DesignCon99 Paper
- **BLVDS White Paper**
  A Baker's Dozen of High-Speed Differential Backplane Design Tips.
  DesignCon2000 Paper
- **BLVDS White Paper**
  Bus LVDS Expands Applications for Low Voltage Differential Signaling (LVDS).
  DesignCon2000 Paper

8.1.5 Design Tools - RAPIDESIGNERS

The National Semiconductor Transmission Line RAPIDESIGNERs make quick work of calculations frequently used in the design of data transmission line systems on printed circuit boards. Based on principles contained in the National Interface Databook, the Transmission Line RAPIDESIGNER benefits from our many years of experience in designing and manufacturing data transmission and interface products and from helping our valued customers obtain the most from National's Interface Products.

The following calculations can be made with the RAPIDESIGNER for both Microstrip and Stripline geometries.

- Characteristic Impedance (Z_O)
- Intrinsic Delay
- Unterminated Stub Length
- Loaded Impedance
- Differential Impedance
- Propagation Delay
- Reflection Coefficient
- C_O and L_O
- Reactance Frequency

Two versions of the popular RAPIDESIGNER are available while supplies last. The two RAPIDESIGNERs differ in the dimensions supported; one is for METRIC units while the other supports ENGLISH units.

- RAPIDESIGNER, Metric Units, LIT# 633200-001
- RAPIDESIGNER, English Units, LIT# 633201-001

A full Operation and Application Guide is provided in AN-905. Also included in the application note are the formulas for the calculations, accuracy information, example calculations and other useful information.

To obtain a RAPIDESIGNER, contact the National Customer Support Center in your area.

8.2.0 LVDS STANDARD – ANSI/TIA/EIA-644

Copies of the ANSI/TIA/EIA-644 LVDS Standard can be purchased from Global Engineering Documents. Contact information that was current at the time this book was printed is:

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112-5704

or call

USA and Canada: 1.800.854.7179
International: 1.303.397.7956

http://global.ihs.com/

8.3.0 IBIS I/O MODEL INFORMATION

I/O Buffer Information Specification (IBIS) is a behavioral model specification defined within the ANSI/EIA-656 standard. LVDS IBIS models are available from National's Website which can be used by most simulators/EDA tools in the industry. Please see: **http:www.national.com/models/ibis/Interface/**

Also, visit the ANSI/EIA-656 Website: **www.eia.org/EIG/IBIS/ibis.htm** for a vendor listing or contact your software vendor.

Chapter 13 of National's 1999 Interface Databook (LIT# 400058) describes IBIS models in detail. A major portion of this material is also covered in National's Application Note AN-1111.

NOTES

Block Name: LVDSdsm3Ncd
Low Level Differential Driver with Tristate and Wire OR.
(Requires external termination for current output.)

Used to provide both 'cmd_out' data and a fast trigger mode.

Size: Area = 354 X 243μm

Power Requirement: - 2.5V +/- 0.2V , 14mW

Inputs:
Digital -
- wr - wire 'or' enable
- oe - output enable
- wr_datain - logic levels for 'or' output
- cmd_datain – standard data output for Low Level Driver

Analog –
- adjCur - Adjusts current will attach to Vdd in this version
- monSF- Allows monitoring of current source gate voltate. Diagnostic only. →Not pinned out.←

Outputs:
- outPlus – positive (voltage) going output. (3mA sink-source)
- outMinus – negative (voltage) going output. (3mA sink-source)

Output Reference – Current outputs must be referenced to an external voltage (provided by the receiver) of 1.25V +/-.3V A small net current, due to the mismatch in PMOS and NMOS output current mirrors is expected. (~50uA)

Functionality:
Low Level Driver is enabled by 'oe' = hi for either of two operational modes.
Outputs nominal 3mA +/-.5mA
1) wr = low (0V) Full current (3mA) output mode. Intended for use with only one device 'enabled' at at time when multiple devices are connected on the same databus.

cmd_datain	OutPlus	outminus
Lo (0V)	3mA sink	3mA source
Hi (2.5V)	3mA source	3mA sink

2) wr=high (2.5V) 1/2 current , zero offset mode. Outputs source or sink current only when input is high. This allows a wire 'or' mode of several chips together.

wr_datain	OutPlus	outminus
Lo (0V)	~0mA	~0mA
Hi (2.5V)	1.5mA source	1.5mA sink

Wire 'Or' mode was added as part of a *fastout* option to allow a self triggering mode, useful for initial checkout of detector mounted electronincs. In this mode, any of the 16 ternary inputs (attached and enabled) that has dete cted a signal over its selected threshold will apply a logic high at the wr_datain Note that wire 'or' refers only to the connection of multiple , enabled, low level drivers in wire or mode.
When multiple outputs are connected in parallel (up to ~13) the currents add. More than one Low Level Driver output triggering can be detected with a level sensitive receiver. Since the output is ~0 when wr_datain is low no cumumulative offset results when multiple low level drivers are connected in parallel.

Termination - In order to allow careful termination the long twisted pair lines, a high impedance output is utilized. A fixed reference of ~1.25V at the receiver is required and will be part of the termination network. The load used in our SPICE characterization includes 50Ω on each output to a common node connected to a termination voltage through a 75Ω resistor. Stray capacitance is modeled using 12.5pF between outputs and 12.5pF on each output to gnd. SPICE calculations and tests of prototypes indicate that the LOW Level Driver should be able to operate at data rates well in excess of 50MHz. An measured output can be found in the **Fastout** section.

Hookup - a special mode will need to be built into the ROD receiver to accommodate both output modes of this driver. One possibility could be to utilize a programmable offset and threshold in a differential comparator.

Schematics –
The **Single ended to Differential** drive (see schematic) has been designed to match the transition times of high to low and low to high transitions to minimize common mode on the output lines.

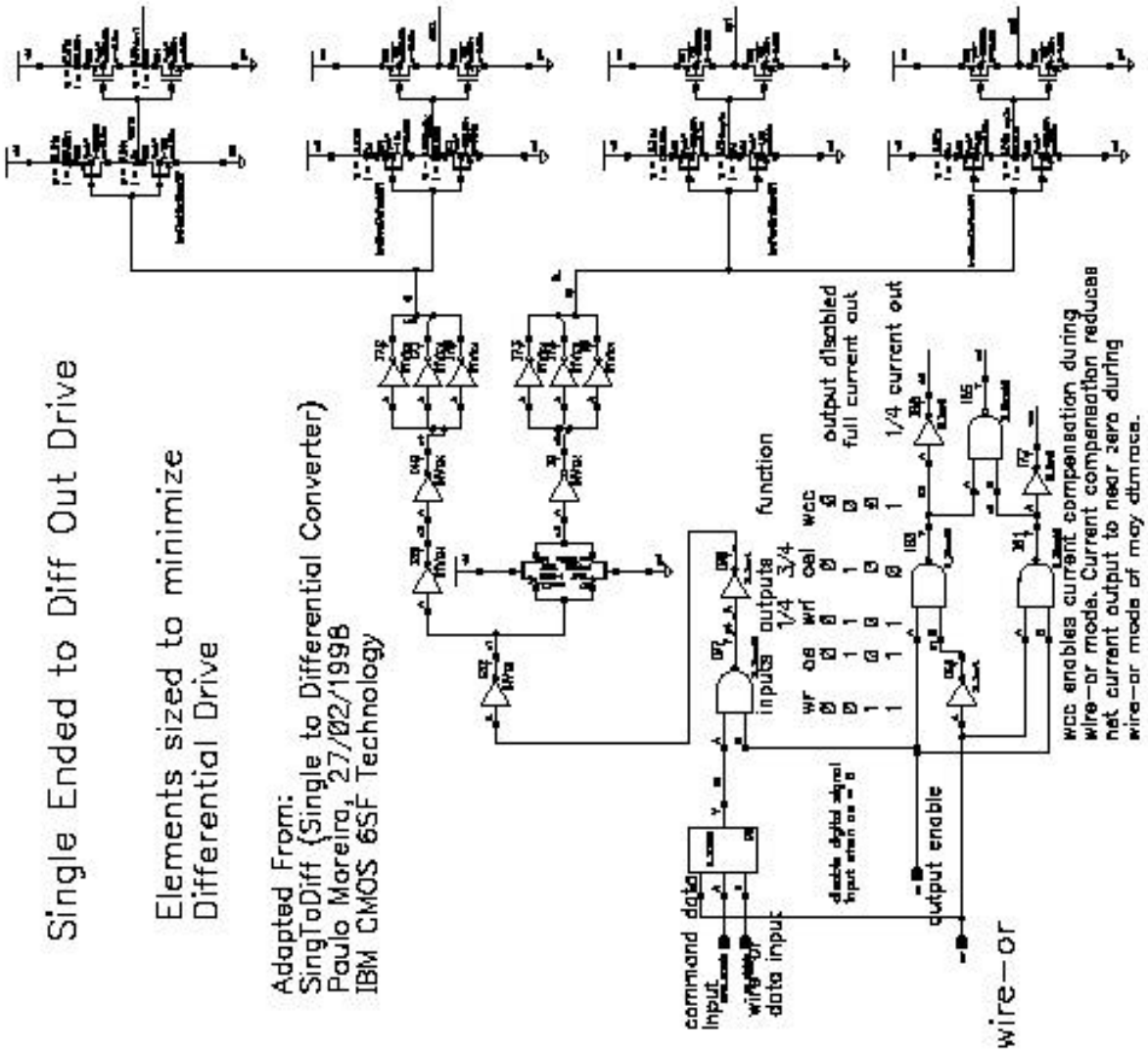
Output Drive with current sources - utilizes a constant current bridge drive network.
Each output (OutPlus, OutMinus) is connected to the drain of one NMOS and one PMOS switch. Current flows from the data selected PMOS switch through the output cable and termination and back through the cable to the NMOS switch.

A mode dependent matched current is provided to the NMOS and PMOS switches by a parallel current mirror pair in 1/4 and 3/4 proportion.
In 'Data Out' mode the parallel current mirror slaves are both switched on resulting in a matched 'sink' and 'source' current of ~3mA. Small differences in the output current can be expected due to differences in matching of the NMOS and PMOS current mirrors.
In wire 'or' mode the current source providing 3/4 of the data mode current is shunted around the switch allowing only 1/4 of the current to be switched by the bridge network. A parallel network is connected to the output providing 1/4 of

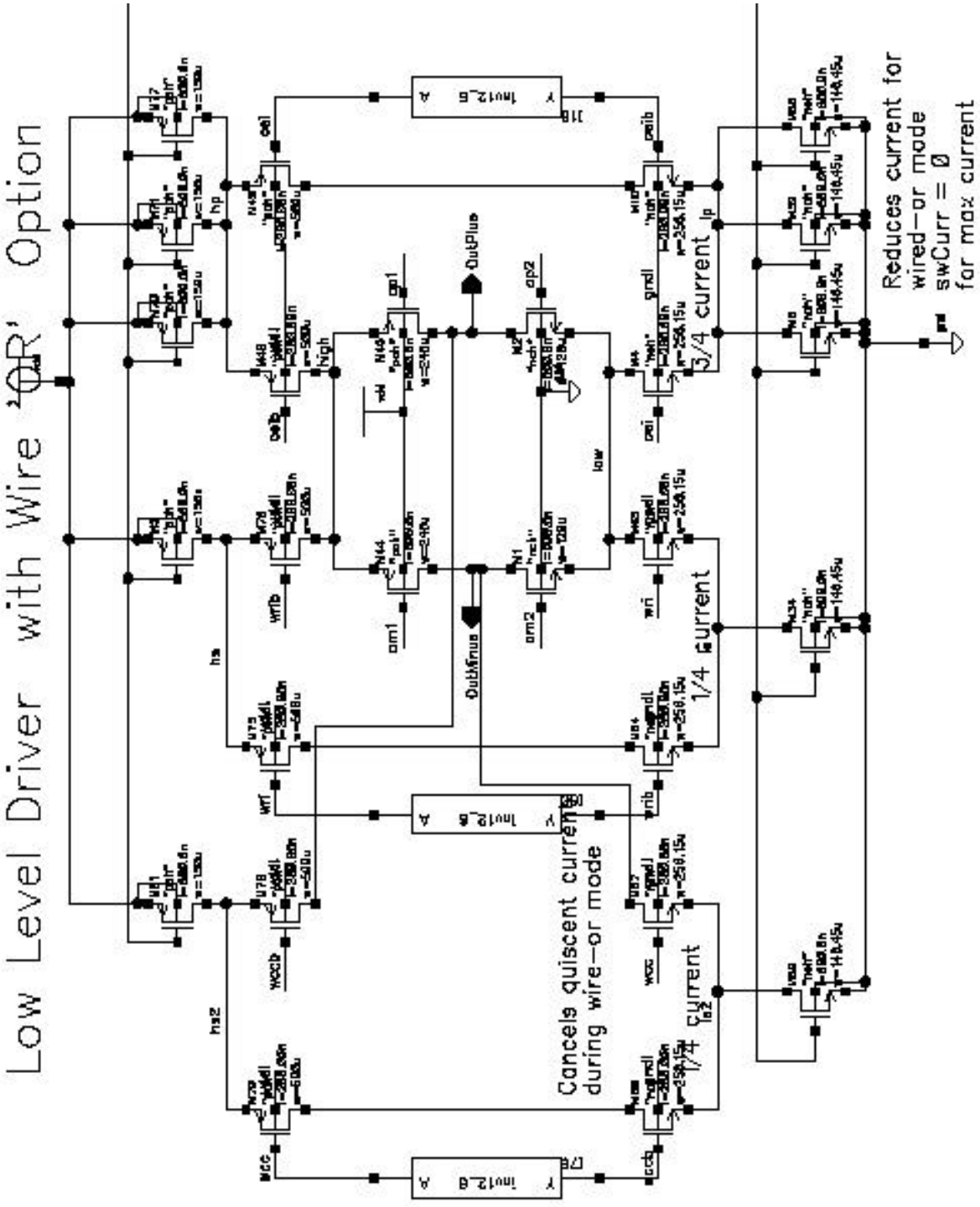
the data mode current to the outputs in a fixed state. It is wired so that when 'wr_datin' is low the currents cancel; no current flows through the cable and when 'wr_datin' is high the currents add resulting in a total current of 1/2 of the normal data mode value.
This block is designed to have constant current draw in all modes of operation.

Current Mirror masters for Low Level Driver - A simple resistor based mirror master is used to provide the output current reference. of approximately 750μA. Output current depends most directly on the fabricated value of sheet resistance, PCres, (211Ω/sq). No difficulty is envisioned with the +/-20% spec, however we expect this is a very conservative value.

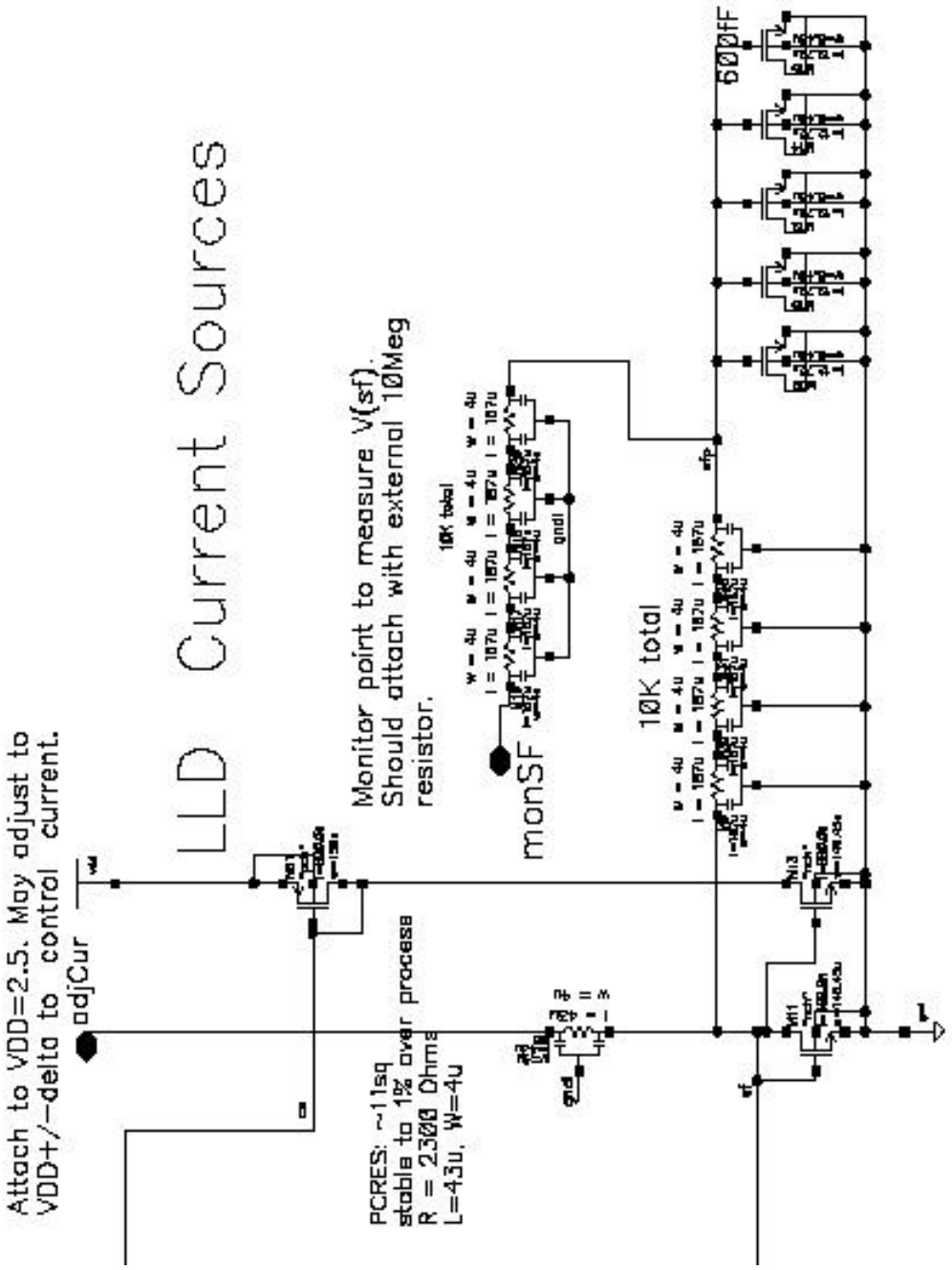
Single ended to Differential Drive
(Digital Logic)



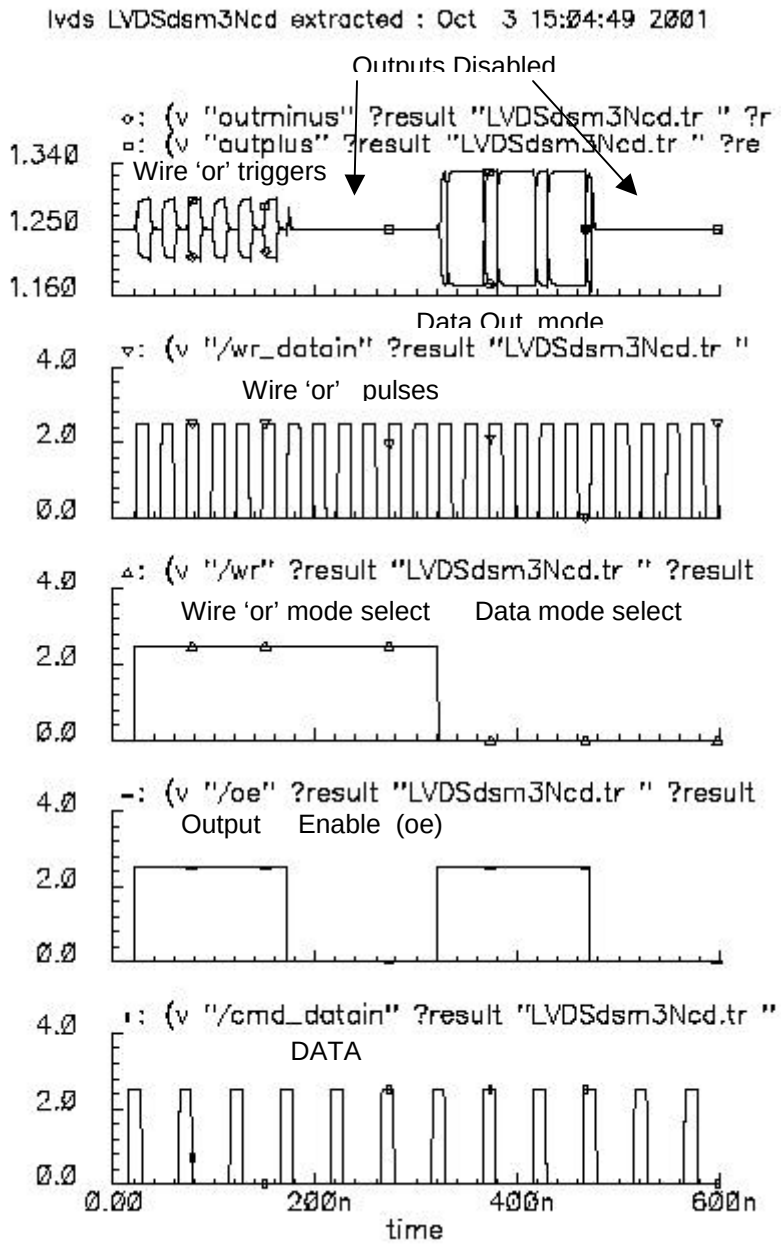
Output Drive with Current sources



Current Mirror Masters for Low Level Driver

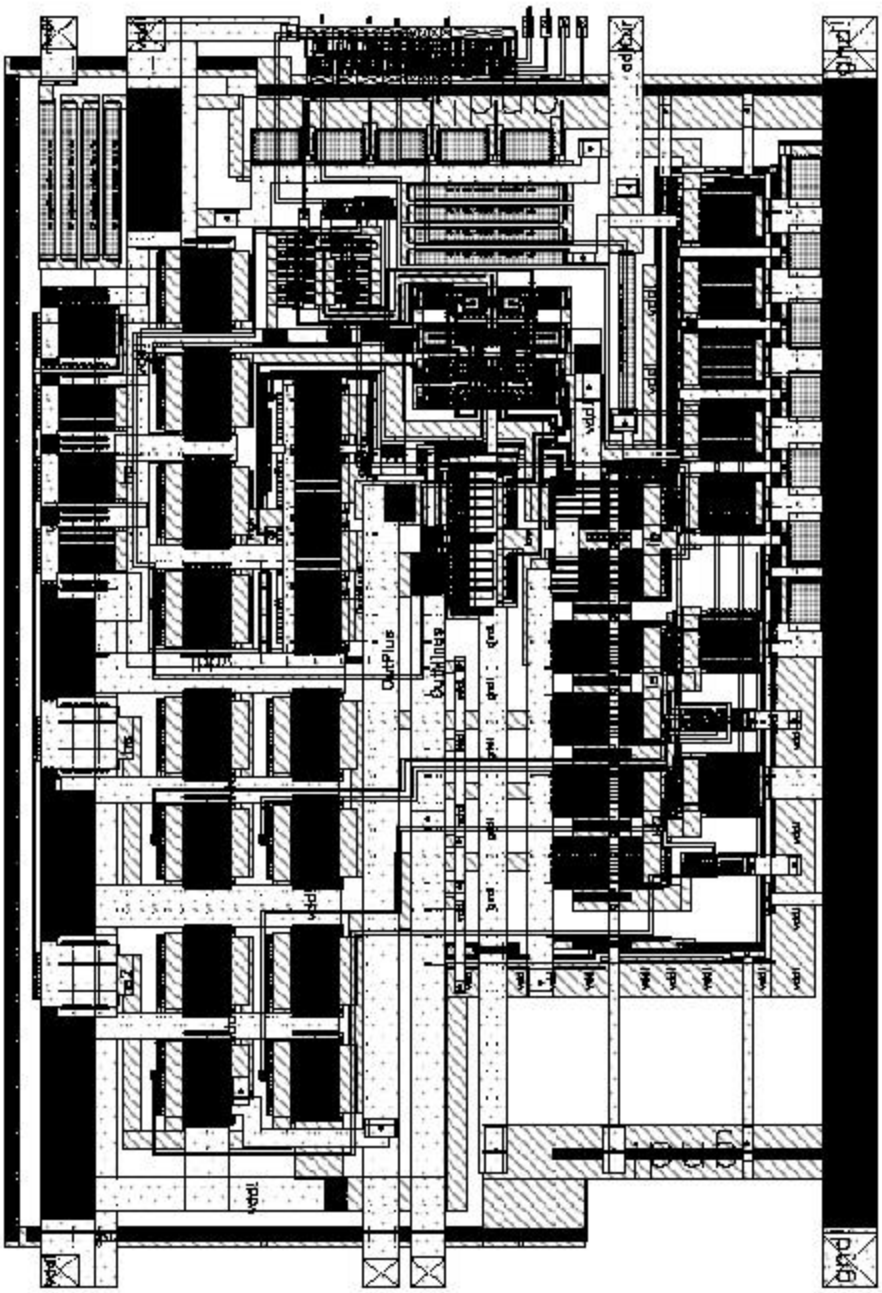


SPICE Calculations



LVDSdsm3Ncd Layout

354 X 243µm



Glossary, Index and Worldwide Sales Offices

Appendix

GLOSSARY

AN	Application Note
ANSI	American National Standards Institute
ASIC	Application Specific Integrated Circuit
B/P	Backplane
BER	Bit Error Rate
BERT	Bit Error Rate Test
BLVDS	Bus LVDS
BTL	Backplane Transceiver Logic
CAT3	Category 3 (Cable classification)
CAT5	Category 5 (Cable classification)
CISPR	International Special Committee on Radio Interference (Comité International Spécial des Perturbations Radioélectriques)
D	Driver
DCR	DC Resistance
DUT	Device Under Test
ECL	Emitter Coupled Logic
EIA	Electronic Industries Association
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EN	Enable
ESD	Electrostatic Discharge
EVK	Evaluation Kit
FCC	Federal Communications Commission
FPD	Flat Panel Display
FPD-LINK	Flat Panel Display Link
Gbps	Gigabits per second
GTL	Gunning Transceiver Logic
Hi-Z	High Impedance
IC	Integrated Circuit
I/O	Input/Output
IBIS	I/O Buffer Information Specification
IDC	Insulation Displacement Connector
IEEE	Institute of Electrical and Electronics Engineers
kbps	kilobits per second
LAN	Local Area Network

GLOSSARY (continued)

LDI	LVDS Display Interface
LVDS	Low Voltage Differential Signaling
Mbps	Mega bits per second
MDR	Mini Delta Ribbon
MLC	Multi Layer Ceramic
NRZ	Non Return to Zero
PCB	Printed Circuit Board
PECL	Pseudo Emitter Coupled Logic
PHY	Physical layer device
PLL	Phase Lock Loop
PRBS	Pseudo Random Bit Sequence
R	Receiver
RFI	Radio Frequency Interference
RS	Recommended Standard
RT	Termination Resistor
RX	Receiver
SCI	Scalable Coherent Interface
SCSI	Small Computer Systems Interface
SDI	Serial Digital Interface
SER/DES	Serializer/Deserializer
SUT	System Under Test
T	Transceiver
TDR	Time Domain Refletometry
TEM	Transverse Electro-Magnetic
TFT	Thin Film Transistor
TI	Totally Irrelevant
TIA	Telecommunications Industry Association
TP	Test Point
TTL	Transistor Transistor Logic
TWP	Twisted Pair
TX	Transmitter
UTP	Unshielded Twisted Pair
VCM	Voltage Common-mode
VCR	Video Cassette Recorder

19-1932; Rev 1; 1/02

MAXIM

SC70, 5ns, Low-Power, Single-Supply, Precision TTL Comparators

General Description

The MAX9010/MAX9011/MAX9013 single and MAX9012 dual, high-speed comparators operate from a single 4.5V to 5.5V power supply and feature low-current consumption. They have precision differential inputs and TTL outputs. They feature short propagation delay (5ns, typ), low-supply current, and a wide common-mode input range that includes ground. They are ideal for low-power, high-speed, single-supply applications.

The comparator outputs remain stable through the linear region when driven with slow-moving or low input-overdrive signals, eliminating the output instability common to other high-speed comparators. The input voltage range extends to 200mV below ground with no output phase reversal. The MAX9013 features complementary outputs and both the MAX9011/MAX9013 have a latch enable input (LE). The MAX9013 is an improved plug-in replacement for the industry-standard MAX913 and LT1016/LT1116, offering lower power and higher speed when used in a single 5V supply application.

For space-critical designs, the single MAX9010 is available in the tiny 6-pin SC70 package. The single MAX9011 is available in a space-saving 6-pin SOT23 package. The dual MAX9012 and the single MAX9013 are available in 8-pin µMAX and 8-pin SO packages. All products in the family are guaranteed over the extended temperature range of -40°C to +85°C.

Applications

High-Speed Signal Squaring

Zero-Crossing Detectors

High-Speed Line Receivers

High-Speed Sampling Circuits

High-Speed Triggers

Fast Pulse-Width/Height Discriminators

Features

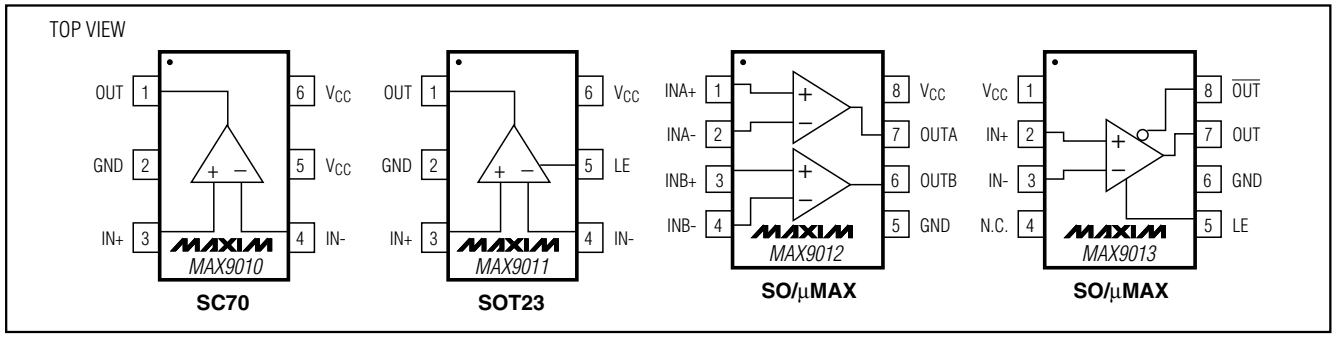
- **Ultra-Fast, 5ns Propagation Delay**
- **Low Quiescent Current:**
  900µA (MAX9010/MAX9011)
  1.3mA (MAX9013)
  2.4mA (MAX9012)
- **Single-Supply 4.5V to 5.5V Applications**
- **Input Range Extends Below Ground**
- **No Minimum Input Signal Slew-Rate Requirement**
- **No Supply-Current Spikes During Switching**
- **Stable when Driven with Slow-Moving Inputs**
- **No Output Phase Reversal for Overdriven Inputs**
- **TTL-Compatible Outputs (Complementary for MAX9013)**
- **Latch Function Included (MAX9011/MAX9013)**
- **High-Precision Comparators**
  0.7mV Input Offset Voltage
  3.0V/mV Voltage Gain
- **Available in Tiny 6-Pin SC70 and SOT23 Packages**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX9010EXT-T	-40°C to +85°C	6 SC70-6	AAA
MAX9011EUT-T	-40°C to +85°C	6 SOT23-6	AADD
MAX9012EUA	-40°C to +85°C	8 µMAX	—
MAX9012ESA	-40°C to +85°C	8 SO	—
MAX9013EUA	-40°C to +85°C	8 µMAX	—
MAX9013ESA	-40°C to +85°C	8 SO	—

Selector Guide appears at end of data sheet.

Pin Configurations



SC70, 5ns, Low-Power, Single-Supply, Precision TTL Comparators

ABSOLUTE MAXIMUM RATINGS

Power Supply (V_{CC} to GND) .....-0.3V to +6V
Analog Input (IN+ or IN-) to GND.....-0.3V to (V_{CC} + 0.3V)
Input Current (IN+ or IN-) .....±30mA
LE to GND .....-0.3V to (V_{CC} + 0.3V)
Continuous Output Current.....±40mA
Continuous Power Dissipation (T_A = +70°C)
6-Pin SC70 (derate 3.1mW/°C above +70°C).....245mW
6-Pin SOT23 (derate 8.7mW/°C above +70°C).....696mW
8-Pin µMAX (derate 4.5mW/°C above +70°C).....362mW
8-Pin SO (derate 5.9mW/°C above +70°C).....471mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (MAX9010/MAX9011)

(V_{CC} = 5V, V_{LE} = 0 (MAX9011 only), V_{CM} = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Inferred from V_{OS} tests		4.5		5.5	V
Power-Supply Current (Note 2)	I_{CC}				0.90	2.1	mA
Input Offset Voltage (Note 3)	V_{OS}	T_A = +25°C			±1	±5	mV
		T_A = T_{MIN} to T_{MAX}				±7	
Input Offset-Voltage Drift	$\Delta V_{OS}/\Delta T$				±2		µV/°C
Input Bias Current	I_B				±0.5	±2	µA
Input Offset Current	I_{OS}				±40	±200	nA
Differential Input Resistance (Note 4)	$R_{IN(DIFF)}$	$V_{IN(DIFF)}$ = ±10mV			250		kΩ
Common-Mode Input Resistance (Note 4)	$R_{IN(CM)}$	-0.2V ≤ V_{CM} ≤ (V_{CC} - 1.9V)			1		MΩ
Common-Mode Input Voltage Range (Note 4)	V_{CM}	Inferred from V_{OS} tests		-0.2		V_{CC} - 1.9	V
Common-Mode Rejection Ratio	CMRR	-0.2V ≤ V_{CM} ≤ (V_{CC} - 1.9V)			95		dB
Power-Supply Rejection Ratio	PSRR	V_{CC} = 4.5V to 5.5V			82		dB
Small-Signal Voltage Gain	A_V	1V ≤ V_{OUT} ≤ 2V			3000		V/V
Output Low Voltage	V_{OL}	V_{IN} ≥ 100mV	I_{SINK} = 0		0.3	0.5	V
			I_{SINK} = 4mA		0.5	0.6	
Output High Voltage	V_{OH}	V_{IN} ≥ 100mV, V_{CC} = 4.5V	I_{SOURCE} = 0	2.7	3.3		V
			I_{SOURCE} = 4mA	2.4	2.9		
Output Short-Circuit Current	I_{OUT}	Sinking			20		mA
		Sourcing			30		
Latch Enable Pin High Input Voltage	V_{IH}	MAX9011 only		2			V
Latch Enable Pin Low Input Voltage	V_{IL}	MAX9011 only				0.8	V
Latch Enable Pin Bias Current	I_{IH}, I_{IL}	MAX9011 only, V_{LE} = 0 and V_{LE} = 5V				±25	µA

ELECTRICAL CHARACTERISTICS (MAX9010/MAX9011) (continued)

(V_{CC} = 5V, V_{LE} = 0 (MAX9011 only), V_{CM} = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Latch Setup Time (Note 8)	t_{SU}	MAX9011 only		2	0		ns
Latch Hold Time (Note 8)	t_H	MAX9011 only		2	0.5		ns
Latch Propagation Delay (Note 8)	t_{LPD}	MAX9011 only			5		ns
Input Noise-Voltage Density	e_n	f = 100kHz			6		nV/√Hz
Propagation Delay (Note 6)	t_{PD+}, t_{PD-}	C_{LOAD} = 5pF, T_A = +25°C	$V_{OVERDRIVE}$ = 100mV		5	8	ns
			$V_{OVERDRIVE}$ = 5mV		5.5	9	
		C_{LOAD} = 5pF, T_A = T_{MIN} to T_{MAX}	$V_{OVERDRIVE}$ = 100mV			9	
			$V_{OVERDRIVE}$ = 5mV			10	
Output Rise Time	t_R	0.5V ≤ V_{OUT} ≤ 2.5V			3		ns
Output Fall Time	t_F	2.5V ≥ V_{OUT} ≥ 0.5V			2		ns
Input Capacitance	C_{IN}	MAX9010EXT			0.8		pF
		MAX9011EUT			1.2		
Power-Up Time	t_{ON}				1		µs

ELECTRICAL CHARACTERISTICS (MAX9012/MAX9013)

(V_{CC} = 5V, V_{LE} = 0 (MAX9013 only), V_{CM} = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Inferred from PSRR test	4.5		5.5	V
Power-Supply Current (Note 2)	I_{CC}	MAX9012		2.4	4.2	mA
		MAX9013		1.3	2.3	
Input Offset Voltage (Note 5)	V_{OS}	T_A = +25°C		±0.7	±3	mV
		T_A = T_{MIN} to T_{MAX}			±5.5	
Input Offset-Voltage Drift	$\Delta V_{OS}/\Delta T$			±2		µV/°C
Input Bias Current	I_B			±0.5	±2	µA
Input Offset Current	I_{OS}			±40	±200	nA
Differential Input Resistance (Note 4)	$R_{IN(DIFF)}$	$V_{IN(DIFF)}$ = ±10mV		250		kΩ
Common-Mode Input Resistance (Note 4)	$R_{IN(CM)}$	-0.2V ≤ V_{CM} ≤ (V_{CC} - 1.9V)		1		MΩ
Common-Mode Input Voltage Range (Note 4)	V_{CM}	Inferred from CMRR test	-0.2		V_{CC} - 1.9	V
Common-Mode Rejection Ratio	CMRR	-0.2V ≤ V_{CM} ≤ (V_{CC} - 1.9V)	75	95		dB
Power-Supply Rejection Ratio	PSRR	V_{CC} = 4.5V to 5.5V	63	82		dB

SC70, 5ns, Low-Power, Single-Supply, Precision TTL Comparators

ELECTRICAL CHARACTERISTICS (MAX9012/MAX9013) (continued)

(V_{CC} = 5V, V_{LE} = 0 (MAX9013 only), V_{CM} = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal Voltage Gain	A_V	1V ≤ V_{OUT} ≤ 2V		1000	3000		V/V
Output Low Voltage	V_{OL}	V_{IN} ≥ 100mV	I_{SINK} = 0		0.3	0.5	V
			I_{SINK} = 4mA		0.5	0.6	
Output High Voltage	V_{OH}	V_{IN} ≥ 100mV, V_{CC} = 4.5V	I_{SOURCE} = 0	2.7	3.3		V
			I_{SOURCE} = 4mA	2.4	2.9		
Output Short-Circuit Current	I_{OUT}	Sinking			20		mA
		Sourcing			30		
Latch Enable Pin High Input Voltage	V_{IH}	MAX9013 only		2			V
Latch Enable Pin Low Input Voltage	V_{IL}	MAX9013 only				0.8	V
Latch Enable Pin Bias Current	I_{IH}, I_{IL}	MAX9013 only, V_{LE} = 0 and V_{LE} = 5V				±25	µA
Input Noise-Voltage Density	e_n	f = 100kHz			6		nV/√Hz
Propagation Delay (Note 6)	t_{PD+}, t_{PD-}	C_{LOAD} = 5pF, T_A = +25°C	$V_{OVERDRIVE}$ = 100mV		5	8	ns
			$V_{OVERDRIVE}$ = 5mV		5.5	9	
		C_{LOAD} = 5pF, T_A = T_{MIN} to T_{MAX}	$V_{OVERDRIVE}$ = 100mV			9	
			$V_{OVERDRIVE}$ = 5mV			10	
Differential Propagation Delay (Notes 6, 7)	$\Delta t_{PD\pm}$	V_{IN} = 100mV step, C_{LOAD} = 5pF, V_{OD} = 5mV			2	3	ns
Channel-to-Channel Propagation Delay (Note 6)	$\Delta t_{PD(ch-ch)}$	MAX9012 only, V_{IN} = 100mV step, C_{LOAD} = 5pF, V_{OD} = 5mV			500		ps
Output Rise Time	t_R	0.5V ≤ V_{OUT} ≤ 2.5V			3		ns
Output Fall Time	t_F	2.5V ≥ V_{OUT} ≥ 0.5V			2		ns
Latch Setup Time (Note 8)	t_{SU}	MAX9013 only		2	0		ns
Latch Hold Time (Note 8)	t_H	MAX9013 only		2	0.5		ns
Latch Propagation Delay (Note 8)	t_{LPD}	MAX9013 only			5		ns
Input Capacitance	C_{IN}	MAX9012EUA/MAX9013EUA			1.5		pF
		MAX9012ESA/MAX9013ESA			2		
Power-Up Time	t_{ON}				1		µs

Note 1: All specifications are 100% tested at T_A = +25°C; temperature limits are guaranteed by design.

Note 2: Quiescent Power-Supply Current is slightly higher with the comparator output at V_{OL}. This parameter is specified with the worst-case condition of V_{OUT} = V_{OL} for the MAX9010/MAX9011 and both outputs at V_{OL} for the MAX9012. For the MAX9013, which has complementary outputs, the power-supply current is specified with either OUT = V_{OL}, $\overline{OUT}$ = V_{OH} or OUT = V_{OH}, $\overline{OUT}$ = V_{OL} (power-supply current is equal in either case).

Note 3: Input Offset Voltage is tested and specified with the Input Common-Mode Voltage set to either extreme of the Input Common-Mode Voltage Range (-0.2V to (V_{CC} - 1.9V)) and with the Power-Supply Voltage set to either extreme of the Power-Supply Voltage Range (4.5V to 5.5V).

Note 4: Although Common-Mode Input Voltage Range is restricted to -0.2V ≤ V_{CM} ≤ (V_{CC} - 1.9V), either or both inputs can go to either absolute maximum voltage limit, i.e., from -0.3V to (V_{CC} + 0.3V), without damage. The comparator will make a correct (and fast) logic decision provided that at least one of the two inputs is within the specified common-mode range. If both inputs are outside the common-mode range, the comparator output state is indeterminate.

Note 5: For the MAX9012, Input Offset Voltage is defined as the input voltage(s) required to make the OUT output voltage(s) remain stable at 1.4V. For the MAX9013, it is defined as the average of two input offset voltages, measured by forcing first the OUT output, then the $\overline{OUT}$ output to 1.4V.

Note 6: Propagation delay for these high-speed comparators is guaranteed by design because it cannot be accurately measured with low levels of input overdrive voltage using automatic test equipment in production. Note that for low overdrive conditions, V_{OS} is added to the overdrive.

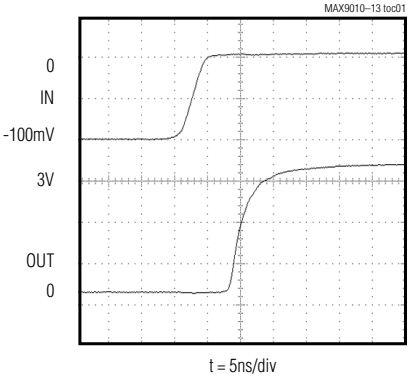
Note 7: Differential Propagation Delay, measured either on a single output of the MAX9012/MAX9013 (or between OUT and $\overline{OUT}$ outputs on the MAX9013) is defined as: $\Delta t_{PD(\pm)} = |(t_{PD+}) - (t_{PD-})|$.

Note 8: Latch times are guaranteed by design. Latch setup time (t_{SU}) is the interval in which the input signal must be stable prior to asserting the latch signal. The hold time (t_H) is the interval after the latch is asserted in which the input signal must remain stable. Latch propagation delay (t_{LPD}) is the delay time for the output to respond when the latch enable pin is deasserted (see Figure 1).

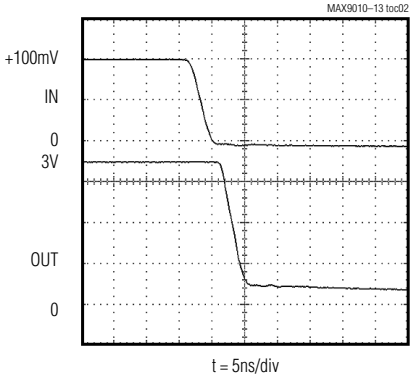
Typical Operating Characteristics

(V_{CC} = 5V, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

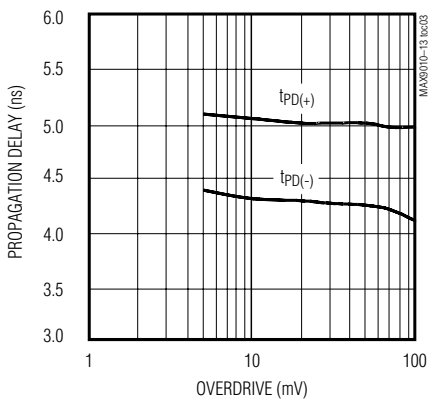
RESPONSE TO +5mV OVERDRIVE



RESPONSE TO -5mV OVERDRIVE



PROPAGATION DELAY vs. INPUT OVERDRIVE

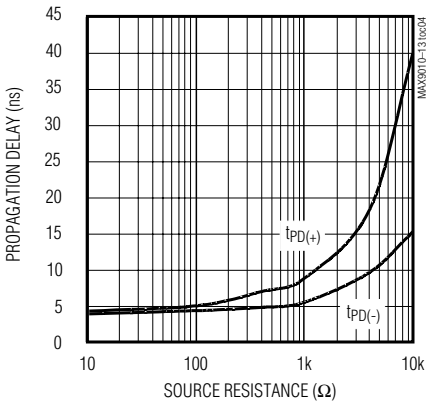


SC70, 5ns, Low-Power, Single-Supply, Precision TTL Comparators

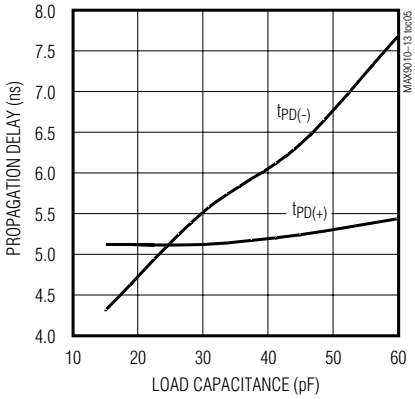
Typical Operating Characteristics (continued)

(V_{CC} = 5V, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

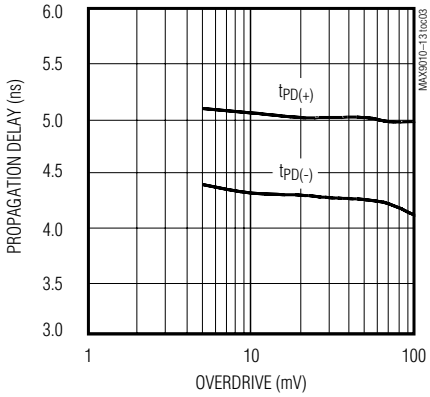
PROPAGATION DELAY vs. SOURCE RESISTANCE



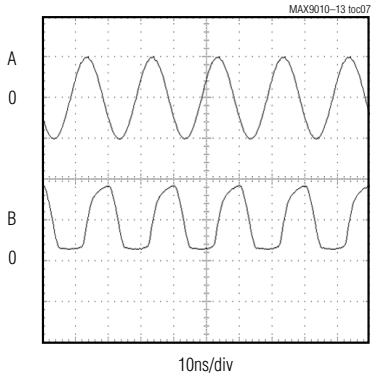
PROPAGATION DELAY vs. LOAD CAPACITANCE



PROPAGATION DELAY vs. INPUT OVERDRIVE

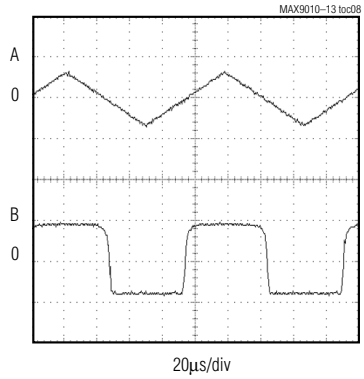


RESPONSE TO 50MHz ±10mV SINE WAVE



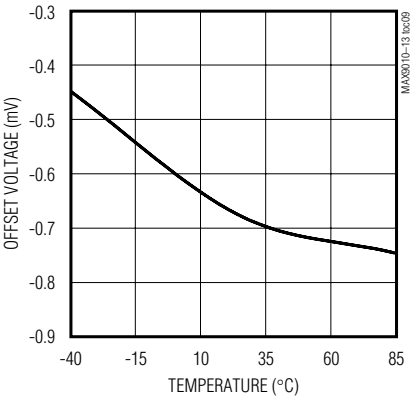
A: Input, 10mV/div
B: Output, 2V/div

RESPONSE TO 10kHz TRIANGLE WAVE

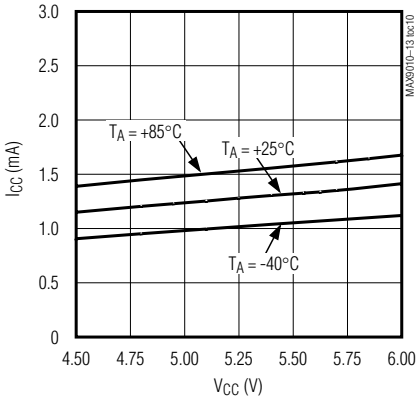


A: Input, 20mV/div
B: Output, 2V/div

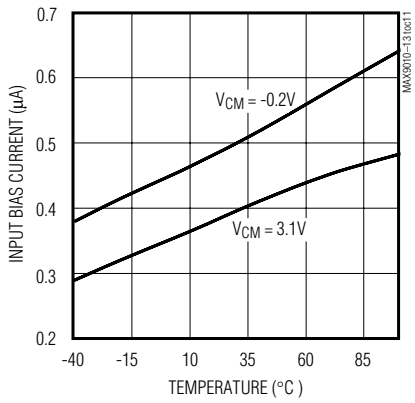
OFFSET VOLTAGE vs. TEMPERATURE



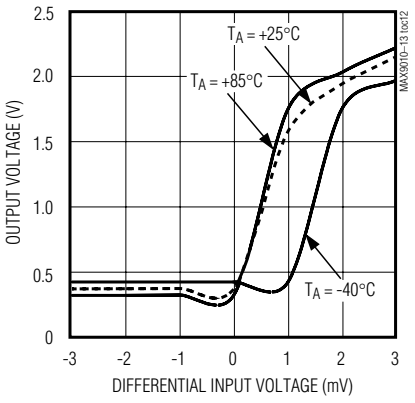
SUPPLY CURRENT vs. SUPPLY VOLTAGE (PER COMPARATOR)



INPUT BIAS CURRENT vs. TEMPERATURE



OUTPUT VOLTAGE vs. DIFFERENTIAL INPUT VOLTAGE



Pin Description

PIN				NAME	FUNCTION
MAX9010	MAX9011	MAX9012	MAX9013		
1	1	—	7	OUT	Comparator Output. OUT is high when IN+ is more positive than IN-.
2	2	5	6	GND	Ground
3	3	—	2	IN+	Noninverting Input
4	4	—	3	IN-	Inverting Input
5, 6	6	8	1	V_{CC}	Positive Power-Supply Voltage. Pins 5 and 6 of the MAX9010 must BOTH be connected to the power-supply rail. Bypass with a 0.1µF capacitor.
—	5	—	5	LE	Latch Enable Input
—	—	1	—	INA+	Noninverting Input, Channel A
—	—	2	—	INA-	Inverting Input, Channel A
—	—	3	—	INB+	Noninverting Input, Channel B
—	—	4	—	INB-	Inverting Input, Channel B
—	—	6	—	OUTB	Comparator Output, Channel B
—	—	7	—	OUTA	Comparator Output, Channel A
—	—	—	4	N.C.	No Connection. Not internally connected. Connect to GND for best results.
—	—	—	8	$\overline{OUT}$	Comparator Complementary Output

Detailed Description

These high-speed comparators have a unique design that prevents oscillation when the comparator is in its linear region, so no minimum input slew rate is required. Many high-speed comparators oscillate in their linear region. One common way to overcome this oscillation is to add hysteresis, but it results in a loss of resolution and bandwidth.

Latch Function

The MAX9011/MAX9013 provide a TTL-compatible latch function that holds the comparator output state (Figure 1). With LE driven to a TTL low or grounded, the latch is transparent and the output state is determined by the input differential voltage. When LE is driven to a TTL high, the existing output state is latched, and the input differential voltage has no further effect on the output state.

Input Amplifier

A comparator can be thought of as having two sections: an input amplifier and a logic interface. The input amplifiers of these devices are fully differential, with input offset voltages typically 0.7mV at +25°C. Input common-mode range extends from 200mV below ground to 1.9V below the positive power-supply rail. The total common-mode range is 3.3V when operating from a 5V supply. The amplifiers have no built-in hysteresis. For highest accuracy, do not add hysteresis. Figure 2 shows how hysteresis degrades resolution.

Input Voltage Range

Although the common-mode input voltage range is restricted to -0.2V to (V_{CC} - 1.9V), either or both inputs can go to either absolute maximum voltage limit, i.e., from -0.3V to (V_{CC} + 0.3V), without damage. The comparator will make a correct (and fast) logic decision provided that at least one of the two inputs is within the specified common-mode range. If both inputs are outside the common-mode range, the comparator output state is indeterminate.

Resolution

A comparator's ability to resolve a small-signal difference, its resolution, is affected by various factors. As with most amplifiers and comparators, the most significant factors are the input offset voltage (V_{OS}) and the common-mode and power-supply rejection ratios (CMRR, PSRR). If source impedance is high, input offset current can be significant. If source impedance is unbalanced, the input bias current can introduce another error. For high-speed comparators, an addi-

SC70, 5ns, Low-Power, Single-Supply, Precision TTL Comparators

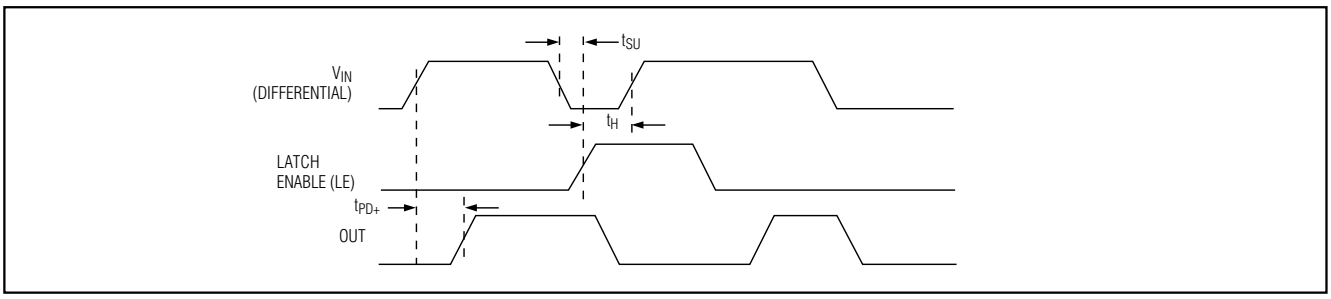


Figure 1. Timing Diagram

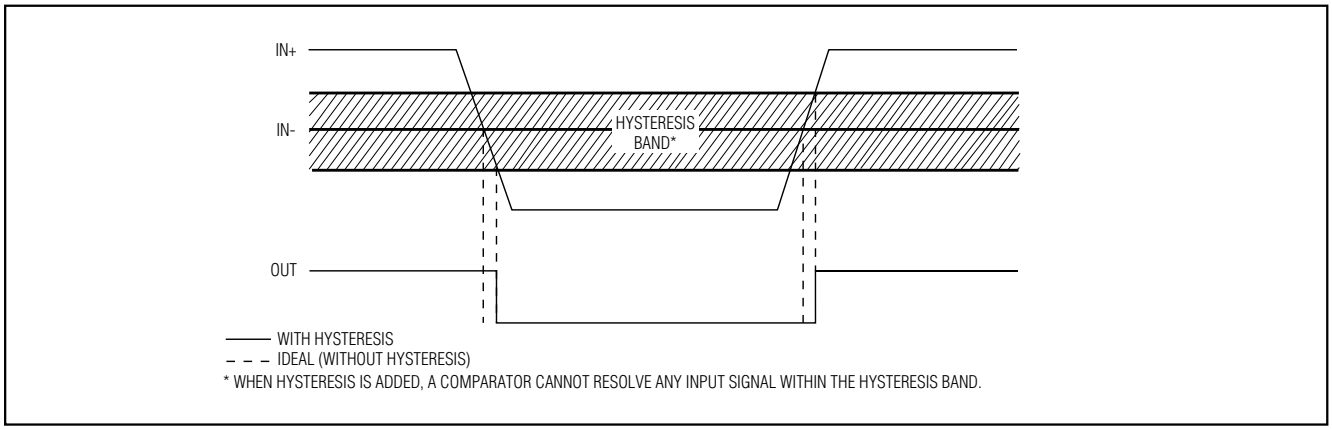


Figure 2. Effect of Hysteresis on Input Resolution

tional factor in resolution is the comparator's stability in its linear region. Many high-speed comparators are useless in their linear region because they oscillate. This makes the differential input voltage region around zero unusable. Hysteresis helps to cure the problem but reduces resolution (Figure 2). The devices do not oscillate in the linear region and require no hysteresis, which greatly enhances their resolution.

Applications Information

Power Supplies, Bypassing, and Board Layout

These products operate over a supply voltage range of 4.5V to 5.5V. Bypass V_{CC} to GND with a 0.1µF surface-mount ceramic capacitor. Mount the ceramic capacitor as close as possible to the supply pin to minimize lead inductance.

As with all high-speed components, careful attention to board layout is essential for best performance. Use a PC board with an unbroken ground plane. Pay close attention to the bandwidth of bypass components and place them as close as possible to the device. Minimize the trace length and area at the comparator inputs. If the source impedance is high, take the utmost care in minimizing its susceptibility to pickup of unwanted signals.

Input Slew Rate

Most high-speed comparators have a minimum input slew-rate requirement. If the input signal does not transverse the region of instability within a propagation delay of the comparator, the output can oscillate. This makes many high-speed comparators unsuitable for processing either slow-moving signals or fast-moving signals with low overdrive. The design of these devices eliminates the minimum input slew-rate requirement. They are excellent for circuits from DC up to 200MHz, even with very low overdrive, where small signals need to be resolved.

SC70, 5ns, Low-Power, Single-Supply, Precision TTL Comparators

Selector Guide

PART	COMPARATORS	LATCH	COMPLEMENTARY OUTPUTS
MAX9010	1	No	No
MAX9011	1	Yes	No
MAX9012	2	No	No
MAX9013	1	Yes	Yes

Chip Information

MAX9010 TRANSISTOR COUNT: 106

MAX9011 TRANSISTOR COUNT: 137

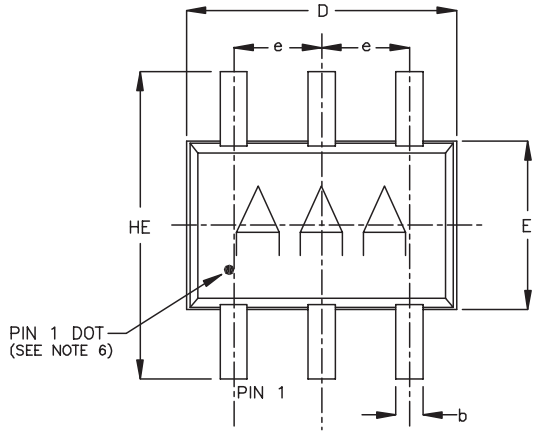
MAX9012 TRANSISTOR COUNT: 212

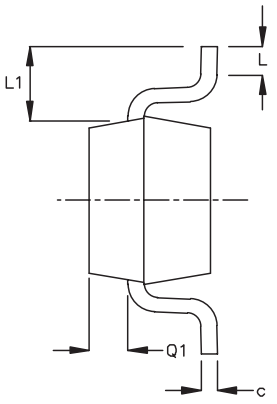
MAX9013 TRANSISTOR COUNT: 145

PROCESS: Bipolar

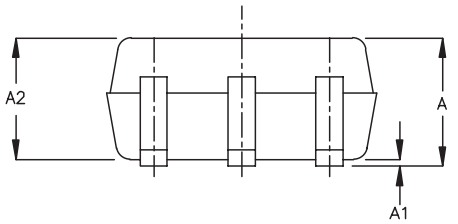
Package Information

SC70, 6L.EPS





SYMBOL	MIN	MAX
e	0.65 BSC	
D	1.80	2.20
b	0.15	0.30
E	1.15	1.35
HE	1.80	2.40
Q1	0.10	0.40
A2	0.80	1.00
A1	0.00	0.10
A	0.80	1.10
c	0.10	0.18
L	0.10	0.30
L1	0.425 TYP.	



1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR
4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70
5. COPLANARITY 4 MILS. MAX.
6. PIN 1 I.D. DOT

MAXIM

PROPRIETARY INFORMATION

TITLE:

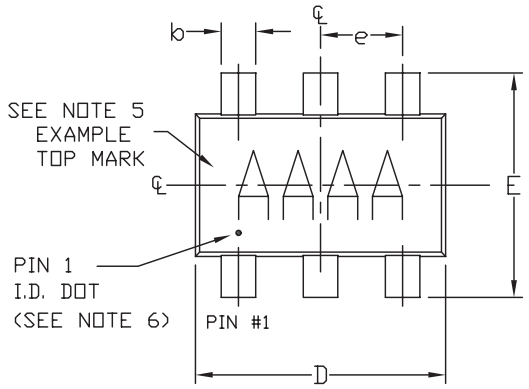
PACKAGE OUTLINE, SC70, 6L

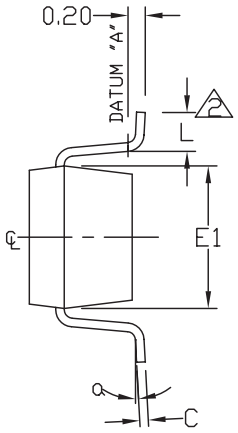
APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0077	B	1/1

SC70, 5ns, Low-Power, Single-Supply, Precision TTL Comparators

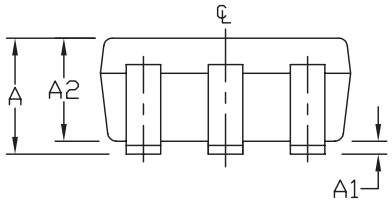
Package Information (continued)

6LSOT.EPS





SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
a	0°	10°



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178.

MAXIM

PROPRIETARY INFORMATION

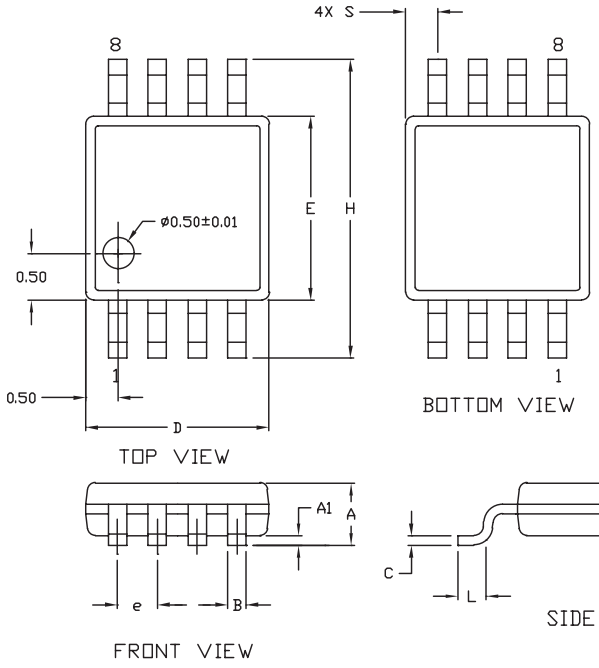
TITLE:

PACKAGE OUTLINE, SOT-23, 6L

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0058	E	1/1

Package Information (continued)

8LUMAXD.EPS



	INCHES		MILLIMETERS		JEDEC INCHES		JEDEC MILLIMETERS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.037	0.043	0.94	1.10	---	0.043	---	1.10
A1	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15
B	0.010	0.014	0.25	0.36	0.010	0.016	0.25	0.40
C	0.005	0.007	0.13	0.18	0.005	0.009	0.13	0.23
D	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
e	0.0256 BSC		0.65 BSC		0.0256 BSC		0.64 BSC	
E	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
H	0.188	0.198	4.78	5.03	0.193 BSC		4.9 BSC	
L	0.016	0.026	0.41	0.66	0.016	0.027	0.40	0.70
α	0°	6°	0°	6°	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC					

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187.

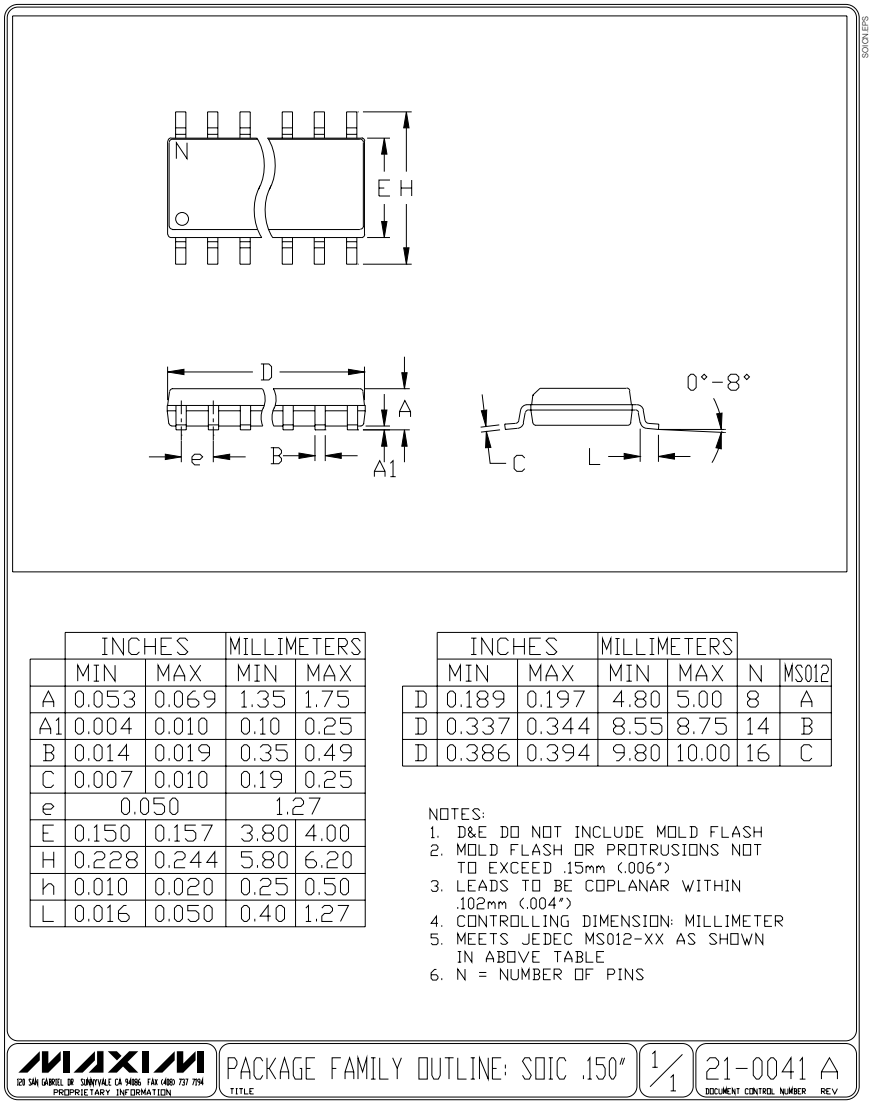
MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 8L uMAX

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0036	I	1/1

SC70, 5ns, Low-Power, Single-Supply, Precision TTL Comparators

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION | PACKAGE FAMILY OUTLINE: SOIC .150" TITLE | 1/1 | 21-0041 A DOCUMENT CONTROL NUMBER REV

National's LVDS Website

Chapter 9

9.0.0 LVDS WEBSITE CONTENTS

9.1.0 NATIONAL WEBSITE

National provides an extensive website targeted for Design Engineers and also Purchasing/Component Engineers. From the main page, you can find:

- Product Tree/Selection Guide
- Datasheets
- Application Notes
- Product Folders
  - View/Download: General Descriptions, Features or the Entire Datasheet
  - Product Status and Pricing Information
  - Application Note Reference
- Packaging Information
- Marking Information
- Technical Support
- Search Engine
- Databooks, CD ROMs and Samples

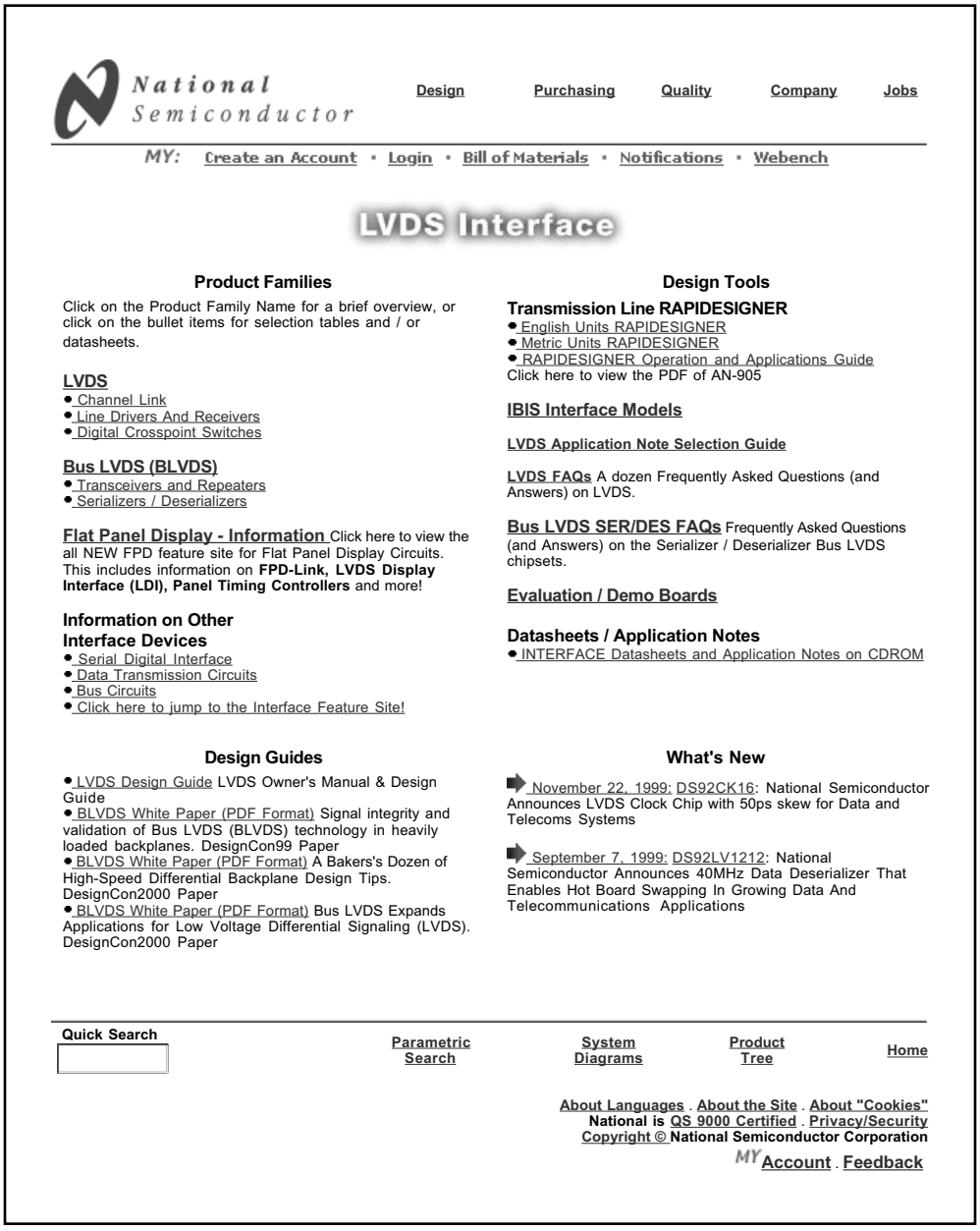
The website's URL is: **www.national.com**

9.2.0 NATIONAL'S LVDS APPINFO WEBSITE

National provides an in depth application site on LVDS. This site provides the design community with the latest information on National's expanding LVDS family. Please visit the LVDS website to view or download documents. On this site, you can locate:

- LVDS Selection Tables
- Frequently Asked Questions (and Answers)
- Application Note Cross Reference Table (AN Number – Topic – Device ID)
- Interface IBIS Models
- Evaluation Boards – Documentation and Ordering Information
- Family Introductions/Overviews
- Design Tools – RAPIDESIGNERS
- Press Releases

The website's URL is: **www.national.com/appinfo/lvds/**



Screen shot of LVDS APPINFO website: www.national.com/appinfo/lvds/

9.3.0 OTHER NATIONAL'S APPINFO WEBSITES

9.3.1 "INTERFACE" Products

National provides an application site on INTERFACE. This site provides the design community with the latest information on National's expanding SDI (Serial Digital Interface) and RS-xxx families. Please visit the INTERFACE website to view or download documents.

9.3.2 "FPD" Products

National provides an in depth application site on Flat Panel Display devices. This site provides the design community the latest information on National's expanding FPD-Link, LDI and TCON families. Please visit the FPD website to view or download documents.

9.3.3 Other/APPINFO/Websites

National provides other in depth application sites. Please visit the main-page for an updated list of pages. This site can be viewed at: **http:www.national.com/appinfo**. It currently includes information on:

- A/D Converters
- Advanced I/O
- Amplifiers
- Audio Products
- Automotive
- Compact RISC
- Custom
- Die Products
- Enhanced Solutions
- Flat Panel Display
- Information Appliance Solutions
- Interface
- LTCC Foundry
- LVDS Interface Products
- Microcontroller
- Micro SMD
- Power
- Scanners
- Temperature Sensors
- USB Technologies
- Wireless Products
- Wireless Basestation Products

NOTES

Selecting an LVDS Device / LVDS Families

Chapter 3

3.0.0 SELECTING AN LVDS DEVICE

3.1.0 GENERAL

National is continually expanding its portfolio of LVDS devices. The devices listed below are current at the time this book goes to press. For the latest list of LVDS devices, please visit our LVDS website at: **www.national.com/appinfo/lvds/**

On this site, you will find the latest LVDS datasheets, application notes, selection tables, FAQs, modeling information/files, white papers, LVDS News, and much much more! The Web is constantly updated with new documents as they are available.

Application questions should be directed to your local National Semiconductor representative or to the US National Interface Hotline: 1-408-721-8500 (8 a.m. to 5 p.m. PST).

LVDS products are classified by device types. Please see below for a short description of each device type and selection table that was current at the time this edition of the LVDS Owner's Manual was printed. Again, visit our web site for the latest information.

3.1.1 Do I need LVDS?

If Megabits or Gigabits @ milliwatts are needed, then LVDS may be the answer for you! It provides high-speed data transmission, consumes little power, rejects noise, and is robust. It is ideal for interconnects of a few inches to tens of meters in length. It provides an ideal interface for chip-to-chip, card-to-card, shelf-to-shelf, rack-to-rack or box-to-box communication.

3.1.2 Which part should I use?

If point-to-point or multidrop configuration is needed – see the LVDS Line Driver/Receivers or Channel Link Family.

If multipoint or certain multidrop configurations are needed – then Bus LVDS offers the technology best suited for these applications.

Parallel? Serialize? Or Serial? – depends upon the application. Small busses typically use the simple PHY parts. However, if the bus is wide, then serialization may make the most sense. Serialization provides a smaller interconnect and reduces cable and connector size and cost. For this application, refer to the Channel Link and also the Bus LVDS SER/DES parts.

3.2.0 LVDS LINE DRIVERS & RECEIVERS

LVDS line drivers and receivers are used to convey information over PCB trace or cable if;

1. You only have a few channels of information to transmit, or

2. Your data is already serialized.

The following table summarizes National's LVDS line drivers and receivers. These devices are also referred to as simple PHYs.

LVDS Driver/Receiver/Transceiver Products

Order Number	# Dr.	# Rec.	Sup. Volt.	Temp	Speed per Channel	Typ ~I_{CC}@ 1Mbps (mA)	Max I_{CC} Disabled (mA)	Driver Max tpd (ns)	Driver Max Ch Skew (ns)	Receiver Max tpd (ns)	Receiver Max Ch Skew (ns)	Package	Comments
DS90LV047ATM	4	0	3.3	Ind	>400Mbps	20	6	1.7	0.5	—	—	16SOIC	
DS90LV047ATMTC	4	0	3.3	Ind	>400Mbps	20	6	1.7	0.5	—	—	16TSSOP	
DS90LV048ATM	0	4	3.3	Ind	>400Mbps	9	5	—	—	2.7	0.5	16SOIC	
DS90LV048ATMTC	0	4	3.3	Ind	>400Mbps	9	5	—	—	2.7	0.5	16TSSOP	
DS90LV031ATM	4	0	3.3	Ind	>400Mbps	21	6	2.0	0.5	—	—	16SOIC	
DS90LV031ATMTC	4	0	3.3	Ind	>400Mbps	21	6	2.0	0.5	—	—	16TSSOP	
DS90LV032ATM	0	4	3.3	Ind	>400Mbps	10	5	—	—	3.3	0.5	16SOIC	
DS90LV032ATMTC	0	4	3.3	Ind	>400Mbps	10	5	—	—	3.3	0.5	16TSSOP	
DS90LV031BTM	4	0	3.3	Ind	>400Mbps	22	6	2.0	0.5	—	—	16SOIC	Available soon
DS90LV031BTMTC	4	0	3.3	Ind	>400Mbps	22	6	2.0	0.5	—	—	16TSSOP	Available soon
DS90LV032BTM	0	4	3.3	Ind	>400Mbps	10	5	—	—	3.0	0.5	16SOIC	Available soon
DS90LV017ATM	1	0	3.3	Ind	>600Mbps	7	—	1.5	—	—	—	8 SOIC	
DS90LV017M	1	0	3.3	Com	>155Mbps	5.5	—	6.0	—	—	—	8 SOIC	
DS90LV018ATM	0	1	3.3	Ind	>400Mbps	5.5	—	—	—	2.5	—	8 SOIC	
DS90LV019TM	1	1	3.3/5	Ind	>100Mbps	16/19	7/8.5	7.0/6.0	—	9.0/8.0	—	14 SOIC	
DS90LV027ATM	2	0	3.3	Ind	>600Mbps	14	—	1.5	0.8	—	—	8 SOIC	
DS90LV027M	2	0	3.3	Com	>155Mbps	9	—	6.0	—	—	—	8 SOIC	
DS90LV028ATM	0	2	3.3	Ind	>400Mbps	5.5	—	—	—	2.5	0.5	8 SOIC	
DS90LV031AW-QML	4	0	3.3	Mil	>400Mbps	21	12	3.5	1.75	—	—	16CERPAK	Mil spec
DS90C031TM	4	0	5	Ind	>155Mbps	15.5	4	3.5	1.0	—	—	16SOIC	
DS90C032TM	0	4	5	Ind	>155Mbps	5	10	—	—	6.0	1.5	16 SOIC	
DS90C031BTM	4	0	5	Ind	>155Mbps	15.5	4	3.5	1.0	—	—	16 SOIC	Pwr Off Hi-Z
DS90C032BTM	0	4	5	Ind	>155Mbps	5	10	—	—	6.0	1.5	16 SOIC	Pwr Off Hi-Z
DS90C031E-QML	4	0	5	Mil	>100Mbps	15.5	10	5.0	3.0	—	—	20 LCC	Military-883
DS90C032E-QML	0	4	5	Mil	>100Mbps	5	11	—	—	8.0	3.0	20 LCC	Military-883
DS90C031W-QML	4	0	5	Mil	>100Mbps	15.5	10	5.0	3.0	—	—	16Flatpack	Military-883
DS90C032W-QML	0	4	5	Mil	>100Mbps	5	11	—	—	8.0	3.0	16Flatpack	Military-883
DS90C401M	2	0	5	Ind	>155Mbps	4	—	3.5	1.0	—	—	8 SOIC	
DS90C402M	0	2	5	Ind	>155Mbps	4.5	—	—	—	6.0	1.5	8 SOIC	
DS36C200M	2	2	5	Com	>100Mbps	12	10	5.5	—	9.0	—	14 SOIC	1394 Link

Note: Evaluation boards utilize a quad driver/receiver pair to perform generic cable/PCB/etc LVDS driver/receiver evaluations, order number LVDS47/48EVK.

3.3.0 LVDS DIGITAL CROSSPOINT SWITCHES

For routing of high-speed point-to-point busses, crosspoint switches may be used. They are also very useful in applications with redundant backup interconnects for fault tolerance. This first device in this planned family of products is now available. It is a 2x2 Crosspoint that operates above 800Mbps and generates extremely low jitter.

LVDS Digital Crosspoint Switches

Order Number	Description	Supply Voltage	Speed	Number of Inputs	Number of Outputs	Package
DS90CP22M-8	2 x 2 800Mbps LVDS Crosspoint Switch	3.3V	800Mbps	2	2	16SOIC

3.4.0 LVDS CHANNEL LINK SERIALIZERS/DESERIALIZERS

If you have a wide TTL bus that you wish to transmit, use one of National's Channel Link devices. Channel Link will serialize your data for you, saving you money on cables and connectors and helping you avoid complex skew problems associated with a completely parallel solution. The following table summarizes National's Channel Link devices.

LVDS Channel Link Serializer/Deserializer Products

Order Number	Mux/Demux Ratio	Type	Supply Voltage	Clock Frequency	Max Throughput	Package	Comments	Eval Board Order Number
DS90CR211MTD	21:3	Transmitter	5	20-40MHz	840Mbps	48TSSOP		CLINK5V28BT-66
DS90CR212MTD	21:3	Receiver	5	20-40MHz	840Mbps	48TSSOP		CLINK5V28BT-66
DS90CR213MTD	21:3	Transmitter	5	20-66MHz	1.38Gbps	48TSSOP		CLINK5V28BT-66
DS90CR214MTD	21:3	Receiver	5	20-66MHz	1.38Gbps	48TSSOP		CLINK5V28BT-66
DS90CR215MTD	21:3	Transmitter	3.3	20-66MHz	1.38Gbps	48TSSOP		CLINK3V28BT-66
DS90CR216MTD	21:3	Receiver	3.3	20-66MHz	1.38Gbps	48TSSOP		CLINK3V28BT-66
DS90CR216AMTD	21:3	Receiver	3.3	20-66MHz	1.38Gbps	48TSSOP	Enhanced Set/Hold Times	CLINK3V28BT-66
DS90CR217MTD	21:3	Transmitter	3.3	20-85MHz	1.78Gbps	48TSSOP		See Note
DS90CR218AMTD	21:3	Receiver	3.3	20-85MHz	1.78Gbps	48TSSOP		See Note
DS90CR218MTD	21:3	Receiver	3.3	20-75MHz	1.575Gbps	48TSSOP		See Note
DS90CR281MTD	28:4	Transmitter	5	20-40MHz	1.12Gbps	56TSSOP		CLINK5V28BT-66
DS90CR282MTD	28:4	Receiver	5	20-40MHz	1.12Gbps	56TSSOP		CLINK5V28BT-66
DS90CR283MTD	28:4	Transmitter	5	20-66MHz	1.84Gbps	56TSSOP		CLINK5V28BT-66
DS90CR284MTD	28:4	Receiver	5	20-66MHz	1.84Gbps	56TSSOP		CLINK5V28BT-66
DS90CR285MTD	28:4	Transmitter	3.3	20-66MHz	1.84Gbps	56TSSOP		CLINK3V28BT-66
DS90CR286MTD	28:4	Receiver	3.3	20-66MHz	1.84Gbps	56TSSOP		CLINK3V28BT-66
DS90CR286AMTD	28:4	Receiver	3.3	20-66MHz	1.84Gbps	56TSSOP	Enhanced Set/Hold Times	CLINK3V28BT-66
DS90CR287MTD	28:4	Transmitter	3.3	20-85MHz	2.38Gbps	56TSSOP		See Note
DS90CR288MTD	28:4	Receiver	3.3	20-75MHz	2.10Gbps	56TSSOP		See Note
DS90CR288AMTD	28:4	Receiver	3.3	20-85MHz	2.38Gbps	56TSSOP		See Note
DS90CR483VJD	48:8	Transmitter	3.3	32.5-112MHz	5.37Gbps	100TQFP		CLINK3V48BT-112
DS90CR484VJD	48:8	Receiver	3.3	32.5-112MHz	5.37Gbps	100TQFP		CLINK3V48BT-112

Note: 85MHz eval boards will be available in the future. For immediate needs, use CLINK3V28BT-66 with 75 or 85MHz parts.

3.5.0 LVDS FPD-LINK

Use National's FPD Link to convey graphics data from your PC or notebook motherboard to your flat panel displays. The next table summarizes National's FPD Link devices. This family has been extended with the LVDS Display Interface chipset that provides higher resolution support and long cable drive enhancements. The LDI Chipset is ideal for desktop monitor applications and also industrial display applications. The FPD-Link receiver function is also integrated into the timing controller devices to provide a small single-chip solution for TFT Panels.

LVDS Flat Panel Display Link (FPD-Link) and LVDS Display Interface (LDI)

Order Number	Color Bits	Type	Supply Voltage	Max Clock Frequency	Clock Edge Strobe	Package	Comments	Eval Board Order Number
DS90CF561MTD	18-bit	Transmitter	5	40MHz	Falling	48TSSOP		FLINK5V8BT-65 *
DS90CR561MTD	18-bit	Transmitter	5	40MHz	Rising	48TSSOP		FLINK5V8BT-65 *
DS90CF562MTD	18-bit	Receiver	5	40MHz	Falling	48TSSOP		FLINK5V8BT-65 *
DS90CR562MTD	18-bit	Receiver	5	40MHz	Rising	48TSSOP		FLINK5V8BT-65 *
DS90CR581MTD	24-bit	Transmitter	5	40MHz	Rising	48TSSOP		FLINK5V8BT-65
DS90CF563MTD	18-bit	Transmitter	5	65MHz	Falling	48TSSOP		FLINK5V8BT-65 *
DS90CR563MTD	18-bit	Transmitter	5	65MHz	Rising	48TSSOP		FLINK5V8BT-65 *
DS90CF564MTD	18-bit	Receiver	5	65MHz	Falling	48TSSOP		FLINK5V8BT-65 *
DS90CR564MTD	18-bit	Receiver	5	65MHz	Rising	48TSSOP		FLINK5V8BT-65 *
DS90CF583MTD	24-bit	Transmitter	5	65MHz	Falling	56TSSOP		FLINK5V8BT-65
DS90CR583MTD	24-bit	Transmitter	5	65MHz	Rising	56TSSOP		FLINK5V8BT-65
DS90CF584MTD	24-bit	Receiver	5	65MHz	Falling	56TSSOP		FLINK5V8BT-65
DS90CR584MTD	24-bit	Receiver	5	65MHz	Rising	56TSSOP		FLINK5V8BT-65
DS90C363AMTD	18-bit	Transmitter	3.3	65MHz	Programmable	48TSSOP		FLINK3V8BT-65 *
DS90CF363AMTD	18-bit	Transmitter	3.3	65MHz	Falling	48TSSOP		FLINK3V8BT-65 *
DS90CF364MTD	18-bit	Receiver	3.3	65MHz	Falling	48TSSOP		FLINK3V8BT-65 *
DS90CF364AMTD	18-bit	Receiver	3.3	65MHz	Falling	48TSSOP	50% CLKOUT	FLINK3V8BT-65 *
DS90C383AMTD	24-bit	Transmitter	3.3	65MHz	Programmable	56TSSOP		FLINK3V8BT-65
DS90CF383AMTD	24-bit	Transmitter	3.3	65MHz	Falling	56TSSOP		FLINK3V8BT-65
DS90CF384MTD	24-bit	Receiver	3.3	65MHz	Falling	56TSSOP		FLINK3V8BT-65
DS90CF384AMTD	24-bit	Receiver	3.3	65MHz	Falling	56TSSOP	50% CLKOUT	FLINK3V8BT-65
DS90C365MTD	18-bit	Transmitter	3.3	85MHz	Programmable	48TSSOP		See Note *
DS90CF366MTD	18-bit	Receiver	3.3	85MHz	Falling	48TSSOP		See Note *
DS90C385MTD	24-bit	Transmitter	3.3	85MHz	Programmable	56TSSOP		See Note
DS90CF386MTD	24-bit	Receiver	3.3	85MHz	Falling	56TSSOP		See Note
DS90C387VJD	48-bit	Transmitter	3.3	112MHz	Programmable	100TQFP		LDI3V8BT-112
DS90C387AVJD	48-bit	Transmitter	3.3	112MHz	Programmable	100TQFP	Non-DC Balanced	NA
DS90CF388VJD	48-bit	Receiver	3.3	112MHz	Falling	100TQFP		LDI3V8BT-112
DS90CF388AVJD	48-bit	Receiver	3.3	112MHz	Falling	100TQFP	Non-DC Balanced	NA

* For 18-bit evaluation, use 24-bit board for evaluation purposes.
Note: 85MHz eval boards will be available in the future. For immediate needs, FLINK3V8BT-65 can be used with 85MHz part.

LVDS Flat Panel Display Timing Controller Products

Order Number	Color Bits	Resolutions Supported	Supply Voltage	Max Clock Frequency	TCON Core	Package	Input/Output	Eval Board Order Number
FPD85310VJD	6 or 8	XGA/SVGA	3.3	65MHz	Programmable	TQFP	LVDS input/TTL dual port output	Call
FPD87310VJD	6 or 8	XGA/SVGA	3.3	65MHz	Programmable	TQFP	LVDS input/RSDS single port output	Call

Note: FPD8710 in sampling phase.

3.6.0 BUS LVDS

Bus LVDS is an extension of the LVDS line drivers and receivers family. They are specifically designed for multipoint applications where the bus is terminated at both ends. They may also be used in heavily loaded backplanes where the effective impedance is lower than 100Ω. In this case, the drivers may see a load in the 30 to 50Ω range. Bus LVDS drivers provide about 10mA of output current so that they provide LVDS swings with heavier termination loads. Transceivers and Repeaters are currently available in this product family. A "10-bit" Serializer and Deserializer family of devices is also available that embeds and recovers the clock from a single serial stream. This chipset also provides a high level of integration reducing complexity and overhead to link layer ASICs. Clock recovery and "Random Lock" digital blocks are integrated with the core interface line driving and receiving functions. The Deserializer (DS92LV1212/1224) can also be hot-plugged into a live data bus and does not require PLL training.

Special functions are also being developed using BLVDS/LVDS technology. This family provides additional functionality over the simple PHY devices. Currently a special low-skew clock transceiver with 6 CMOS outputs (DS92CK16) and a Repeater/MUX with selectable drive levels (DS92LV222A) are available.

Bus LVDS Products

Order Number	Description	Supply Voltage	Speed	Features	Package
DS92LV010ATM	Single Bus LVDS Transceiver	3.3/5	155Mbps/Ch	3.3V or 5V Operation	8SOIC
DS92LV222ATM	Bus LVDS or LVDS Repeater/Mux	3.3	200Mbps/Ch	Repeater, Mux, or 1:2 Clock Driver Modes	16SOIC
DS92LV090ATVEH	9-Channel Bus LVDS Transceiver	3.3	200Mbps/Ch	Low Part-to-Part Skew	64PQFP
DS92LV1021TMSA	10:1 Serializer w/Embedded Clock	3.3	40MHz	400Mbps Data Payload Over Single Pair	28SSOP
DS92LV1210TMSA	1:10 Deserializer w/Clock Recovery	3.3	40MHz	400Mbps Data Payload Over Single Pair	28SSOP
DS92LV1212TMSA	1:10 Random Lock Deserializer w/Clk Recovery	3.3	40MHz	400Mbps Data Payload Over Single Pair	28SSOP
DS92LV1023TMSA	10:1 Serializer w/Embedded Clock	3.3	66MHz	660Mbps Data Payload Over Single Pair	28SSOP
DS92LV1224TMSA	1:10 Random Lock Deserializer w/Clk Recovery	3.3	66MHz	660Mbps Data Payload Over Single Pair	28SSOP
DS92CK16TMTC	1:6 Clock Distribution	3.3	125MHz	50ps TTL output channel-to-channel skew	24TSSOP
More to come…					

3.7.0 SUMMARY

Over 75 different LVDS products are currently offered by National. For the latest in product information, and news, please visit National's LVDS web site at: **www.national.com/appinfo/lvds/**

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