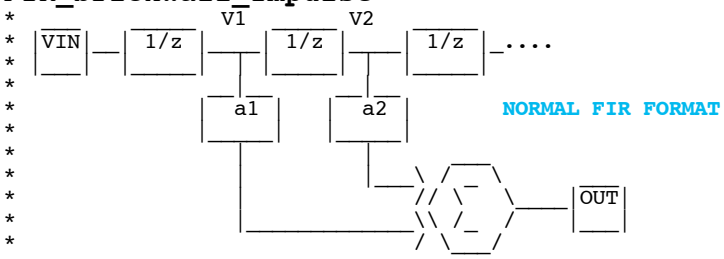
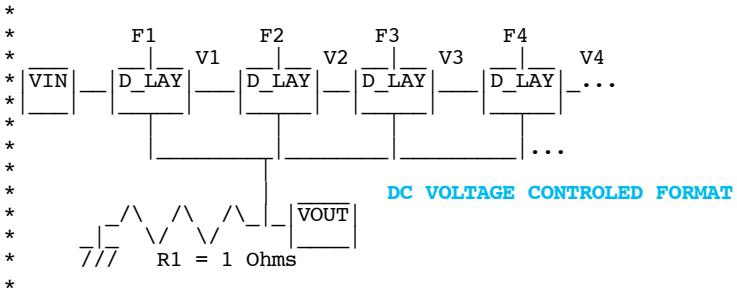
=====FIR_brickwall_Impulse_DC_Controlled=====

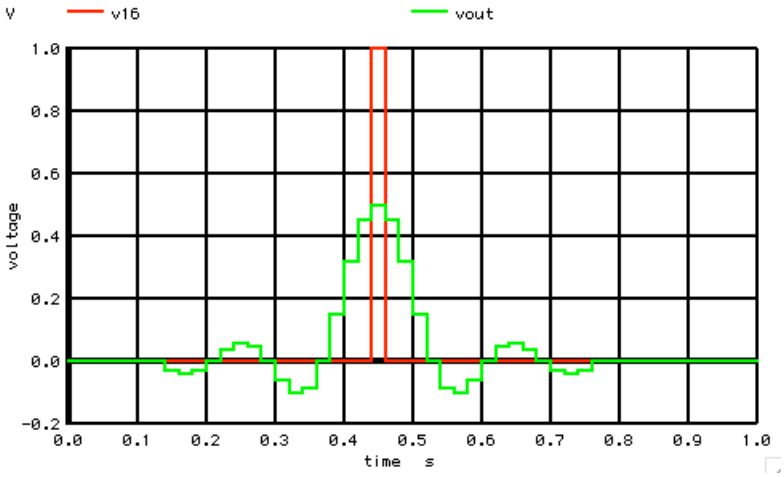
FIR_brickwall_Impulse



A digital filter can approximate the impulse response of a brickwall filter by putting the signal through a series of time delays and feeding a scaled version from each delay point to a common summing point.



This spice simulation will be using delay blocks which receives an external DC scale voltage to scale an output current. This method makes it easy to connect and scale a large number of delay points.



This simulation will use 31 amplitude scaled delay blocks to match a sinc response. The delay point at the 16th stage is simply the input signal with 16 clock delays. While it is not possible to have a impulse response happen before the impulse arrives, the output will look that ways from 16th's stage point of view.

```
*=========SCALED_DELAY=============================================
*            CLK
*
*              |
*  ____     ____|___                        _____
* |VIN|____|D_LAY|_____________________|VOUT|
* |___|    |_____|                     |____|
*                                 | F1
*                        |\  V
*                        |1\/\/\___  _____
*                        | /\/\/   ||IOUT|
*                        |/        ||____|
*
```

```
.SUBCKT   S_DLAY VIN    VOUT   IOUT  CLK  F1
 XZ_DLAY  VIN    VOUT   CLK    Z_DLAY
 BOUT     IOUT   0      I  = -V(VOUT)*V(F1)
.ENDS     S_DLAY
```

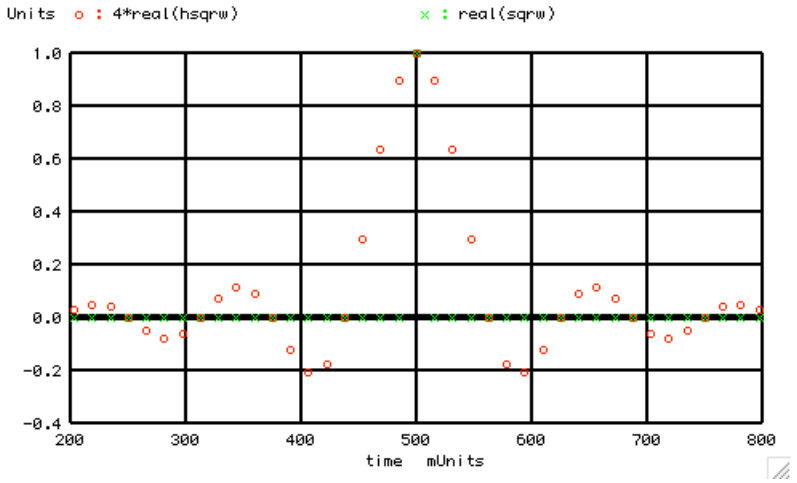
The delay block (Z_DLAY) just delays its input to its output by one clock cycle (CLK). Making the output be a current which scales the delayed output to a DC input (F1) makes constructing the array much easier.

```
*=========Input_Signals=============================================
*V_PULSE  NODE_P NODE_N DC     VALUE   PULSE( VINIT  VPULSE TDELAY TRISE  TFALL  PWIDTH PERIOD )
VIN       VIN    0      DC     0       PULSE( 0      1       .1     1u     1u     20m    33 )
VT        VT     0      DC     0       PWL(   0      0       100    100)
VFIN      FIN    0      DC     1
VFC       FC     0      DC     1
VFS       FS     0      DC     50
BVCLK     CLK    0      V      =       u(sin(6.283*V(FS)*V(VT)))
BF12      F12A   0      V      =       2*sin(3.14*V(FC)/V(FS))
```

The various clock and frequencies can be made DC variable as well.

```
*=========SCALED_DELAY=============================================
XZ_DLAY   VIN    VINZ   CLK              Z_DLAY
XS_DLAY1  VINZ   V1     VOUT   CLK  F17  S_DLAY
XS_DLAY2  V1     V2     VOUT   CLK  F16  S_DLAY
XS_DLAY3  V2     V3     VOUT   CLK  F15  S_DLAY
XS_DLAY4  V3     V4     VOUT   CLK  F14  S_DLAY
XS_DLAY5  V4     V5     VOUT   CLK  F13  S_DLAY
XS_DLAY6  V5     V6     VOUT   CLK  F12  S_DLAY
XS_DLAY7  V6     V7     VOUT   CLK  F11  S_DLAY
XS_DLAY8  V7     V8     VOUT   CLK  F10  S_DLAY
XS_DLAY9  V8     V9     VOUT   CLK  F9   S_DLAY
XS_DLAY10 V9     V10    VOUT   CLK  F8   S_DLAY
XS_DLAY11 V10    V11    VOUT   CLK  F7   S_DLAY
XS_DLAY12 V11    V12    VOUT   CLK  F6   S_DLAY
XS_DLAY13 V12    V13    VOUT   CLK  F5   S_DLAY
XS_DLAY14 V13    V14    VOUT   CLK  F4   S_DLAY
XS_DLAY15 V14    V15    VOUT   CLK  F3   S_DLAY
XS_DLAY16 V15    V16    VOUT   CLK  F2   S_DLAY
XS_DLAY17 V16    V17    VOUT   CLK  F3   S_DLAY
XS_DLAY18 V17    V18    VOUT   CLK  F4   S_DLAY
XS_DLAY19 V18    V19    VOUT   CLK  F5   S_DLAY
XS_DLAY20 V19    V20    VOUT   CLK  F6   S_DLAY
XS_DLAY21 V20    V21    VOUT   CLK  F7   S_DLAY
XS_DLAY22 V21    V22    VOUT   CLK  F8   S_DLAY
XS_DLAY23 V22    V23    VOUT   CLK  F9   S_DLAY
XS_DLAY24 V23    V24    VOUT   CLK  F10  S_DLAY
XS_DLAY25 V24    V25    VOUT   CLK  F11  S_DLAY
XS_DLAY26 V25    V26    VOUT   CLK  F12  S_DLAY
XS_DLAY27 V26    V27    VOUT   CLK  F13  S_DLAY
XS_DLAY28 V27    V28    VOUT   CLK  F14  S_DLAY
XS_DLAY29 V28    V29    VOUT   CLK  F15  S_DLAY
XS_DLAY30 V29    V30    VOUT   CLK  F16  S_DLAY
XS_DLAY31 V30    V31    VOUT   CLK  F17  S_DLAY
```

The 31 delay blocks are shown above. Since the impulse response is symmetrical over time, only half as many DC voltages (F0->F17) are needed. This is were having a normalize print out of a sinc function comes in handy.



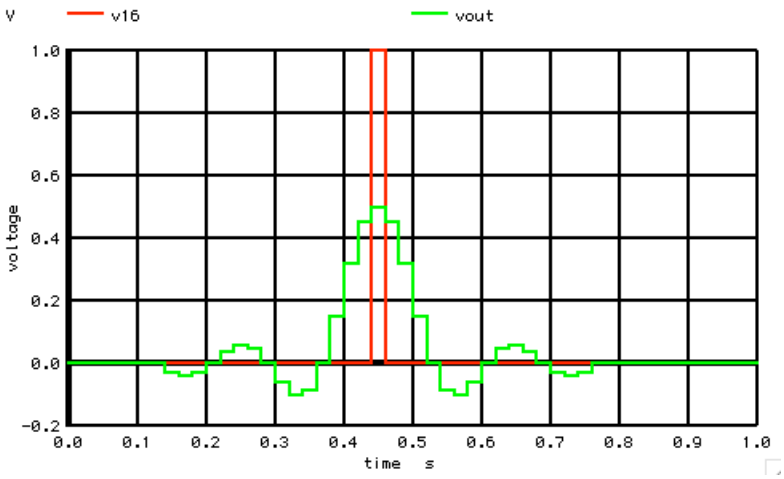

```
*=========SCALED_DELAY=============================================

VF1         F1      0       DC      0
VF2         F2      0       DC      +1.000
VF3         F3      0       DC      +0.900
VF4         F4      0       DC      +0.640
VF5         F5      0       DC      +0.300
VF6         F6      0       DC      +0.000
VF7         F7      0       DC      -0.175
VF8         F8      0       DC      -0.207
VF9         F9      0       DC      -0.125
VF10        F10     0       DC      +0.000
VF11        F11     0       DC      +0.096
VF12        F12     0       DC      +0.118
VF13        F13     0       DC      +0.075
VF14        F14     0       DC      +0.000
VF15        F15     0       DC      -0.060
VF16        F16     0       DC      -0.080
VF17        F17     0       DC      -0.060
```

The 17 DC scaling voltages are shown above. In this format, the FIR filter can be changed by simply changing these DC scaling voltages.

```
*=========SCALED_DELAY=============================================


*TRAN       TSTEP   TSTOP   TSTART  TMAX    ?UIC?
.tran       30u     1       0       30u     UIC
.control
run
set         pensize = 2
plot        v16     vout
.endc
```



Simulating the sinc impulse response is straight forward.

```
============Full_Netlist_For_Copy_Paste========================
FIR_brickwall_Impulse
*   ____     ______      ______      ______
*  |VIN |__|  1/z  |____|  1/z  |____|  1/z  |_....
*  |____|  |_______| |  |_______| |  |_______|
*                    |            |
*                  __|__        __|__
*                 |  a1  |     |  a2  |       NORMAL FIR FORMAT
*                 |______|     |______|
*                    |            |      ___
*                    |            |___\ / _ \
*                    |                // \    \_____|OUT|
*                    |________________\\ /_   /     |___|
*                                      / \___/
*.............................................................
*

*          F1         F2        F3         F4
*        __|__  V1  __|__  V2 __|__  V3  __|__   V4
*|VIN|__|D_LAY|___|D_LAY|__|D_LAY|___|D_LAY|_...
*|___|  |_____|   |_____|  |_____|   |_____|
*          |         |        |          |
*          |_________|________|__________|
*                   |
*                   |          DC VOLTAGE CONTROLED FORMAT
*       _/\  /\  /\_|_|VOUT|
*     _|_  \/  \/      |____|
*     ///   R1 = 1 Ohm
*
*=========Create_Signal==================
*V_PULSE   NODE_P NODE_N DC     VALUE  PULSE( VINIT  VPULSE TDELAY TRISE  TFALL  PWIDTH PERIOD )
VIN        VIN    0      DC     0      PULSE( 0      1      .1     1u     1u     20m    33 )
VT         VT     0      DC     0      PWL(   0      0      100    100)
VFIN       FIN    0      DC     1
VFC        FC     0      DC     1
VFS        FS     0      DC     50
BVCLK      CLK    0      V      =  u(sin(6.283*V(FS)*V(VT)))
BF12       F12A   0      V      =  2*sin(3.14*V(FC)/V(FS))

VF1        F1     0      DC     0
VF2        F2     0      DC     +1.000
VF3        F3     0      DC     +0.900
VF4        F4     0      DC     +0.640
VF5        F5     0      DC     +0.300
VF6        F6     0      DC     +0.000
VF7        F7     0      DC     -0.175
VF8        F8     0      DC     -0.207
VF9        F9     0      DC     -0.125
VF10       F10    0      DC     +0.000
VF11       F11    0      DC     +0.096
VF12       F12    0      DC     +0.118
VF13       F13    0      DC     +0.075
VF14       F14    0      DC     +0.000
VF15       F15    0      DC     -0.060
VF16       F16    0      DC     -0.080
VF17       F17    0      DC     -0.060

XZ_DLAY    VIN    VINZ   CLK                Z_DLAY
XS_DLAY1   VINZ   V1     VOUT   CLK   F17   S_DLAY
XS_DLAY2   V1     V2     VOUT   CLK   F16   S_DLAY
XS_DLAY3   V2     V3     VOUT   CLK   F15   S_DLAY
XS_DLAY4   V3     V4     VOUT   CLK   F14   S_DLAY
XS_DLAY5   V4     V5     VOUT   CLK   F13   S_DLAY
XS_DLAY6   V5     V6     VOUT   CLK   F12   S_DLAY
XS_DLAY7   V6     V7     VOUT   CLK   F11   S_DLAY
XS_DLAY8   V7     V8     VOUT   CLK   F10   S_DLAY
XS_DLAY9   V8     V9     VOUT   CLK   F9    S_DLAY
XS_DLAY10  V9     V10    VOUT   CLK   F8    S_DLAY
XS_DLAY11  V10    V11    VOUT   CLK   F7    S_DLAY
XS_DLAY12  V11    V12    VOUT   CLK   F6    S_DLAY
XS_DLAY13  V12    V13    VOUT   CLK   F5    S_DLAY
XS_DLAY14  V13    V14    VOUT   CLK   F4    S_DLAY
XS_DLAY15  V14    V15    VOUT   CLK   F3    S_DLAY
XS_DLAY16  V15    V16    VOUT   CLK   F2    S_DLAY
XS_DLAY17  V16    V17    VOUT   CLK   F3    S_DLAY
XS_DLAY18  V17    V18    VOUT   CLK   F4    S_DLAY
XS_DLAY19  V18    V19    VOUT   CLK   F5    S_DLAY
XS_DLAY20  V19    V20    VOUT   CLK   F6    S_DLAY
XS_DLAY21  V20    V21    VOUT   CLK   F7    S_DLAY
XS_DLAY22  V21    V22    VOUT   CLK   F8    S_DLAY
XS_DLAY23  V22    V23    VOUT   CLK   F9    S_DLAY
XS_DLAY24  V23    V24    VOUT   CLK   F10   S_DLAY
XS_DLAY25  V24    V25    VOUT   CLK   F11   S_DLAY
```

```
XS_DLAY26 V25    V26    VOUT   CLK  F12  S_DLAY
XS_DLAY27 V26    V27    VOUT   CLK  F13  S_DLAY
XS_DLAY28 V27    V28    VOUT   CLK  F14  S_DLAY
XS_DLAY29 V28    V29    VOUT   CLK  F15  S_DLAY
XS_DLAY30 V29    V30    VOUT   CLK  F16  S_DLAY
XS_DLAY31 V30    V31    VOUT   CLK  F17  S_DLAY
R1        VOUT   0      .5
.tran     30u    1     0      30u    UIC
.control
run
*TRAN     TSTEP  TSTOP  TSTART TMAX   ?UIC?
*tran      10u    2      0      10u
set       pensize = 2
plot      v16 vout

.endc
*=========Switch_Model=======================================
.MODEL    SW      SW(    VT=.5 VH=.1  RON=100m ROFF=100MEG)
*=========SCALED_DELAY=======================================
*            CLK
*
*  ___         __|__          _____
* |VIN|_____|D_LAY|_____________|VOUT|
* |___|     |_____|             |____|
*                    |      | F1
*                    |  |\  V
*                    |_|1\/\/\___|IOUT|
*                      |  /\/\/   |____|
*                      |/
*
.SUBCKT   S_DLAY VIN    VOUT  IOUT  CLK  F1
 XZ_DLAY  VIN    VOUT   CLK  Z_DLAY
 BOUT     IOUT   0      I  = -V(VOUT)*V(F1)
.ENDS     S_DLAY
*=========Z_DLAY============================================
*                                  ____________
*                                 |  _________ |  _____
*  ___     |\          VBF        | |  ___    \|_|     \
* |CLK|__|1\_____________________|_/ |_/   \____|  PE  \_
* |___|  |  /                VLP      |NE \_    |  3   /
*        |/  |/\  /\  /\_____|___|  2 /  |  |___|_____/
*             \/  \/  _|_      /___/   |  |___|
*           RLP       ___             |
*                    |___|
*                CLP ///
*
*  ___     |\  V1  /   V2        |\  V3  /   V4      |\
* |IN |__|4\____/_____________|5\____/_____________|6\_|OUT|
* |___|  | / S1  NE   | _|_   |  / S2  PE   | _|_  |  /|___|
*        |/            |___|  |/             |___| |/
*       Rshunt1        |   |C1  Rshunt2       |   |C2
*     _/\  /\  /\__    |___|  _/\  /\  /\__    |___|
*    |_  \/  \/     ///     |_  \/  \/     ///
*   ///             ///     ///
.SUBCKT   Z_DLAY VIN    OUT    CLK
 B1       VBF    0      V =    u( v(CLK )-.5 )
 RLP      VBF    VLP    10k
 CLP      VLP    0      50n    IC=0
 BNOR2    NE     0      V =    1-u( u(v(VBF )-.5)+u(.5 -v(VLP ) ) -.1)
 BAND3    PE     0      V =      u( u(v(VBF )-.5)*u(.5 -v(VLP ) ) -.1)
 B4       V1     0      V =    V(VIN)
 S1       V1     V2     NE     0    SW
 R1       V2     0      100Meg
 C1       V2     0      1u
 B5       V3     0      V =    V(V2)
 S2       V3     V4     PE     0    SW
 R2       V4     0      100Meg
 C2       V4     0      100u
 B6       OUT    0      V =    V(V4)
.ENDS     Z_DLAY

.end
```

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dsauersanjose@aol.com
Don Sauer