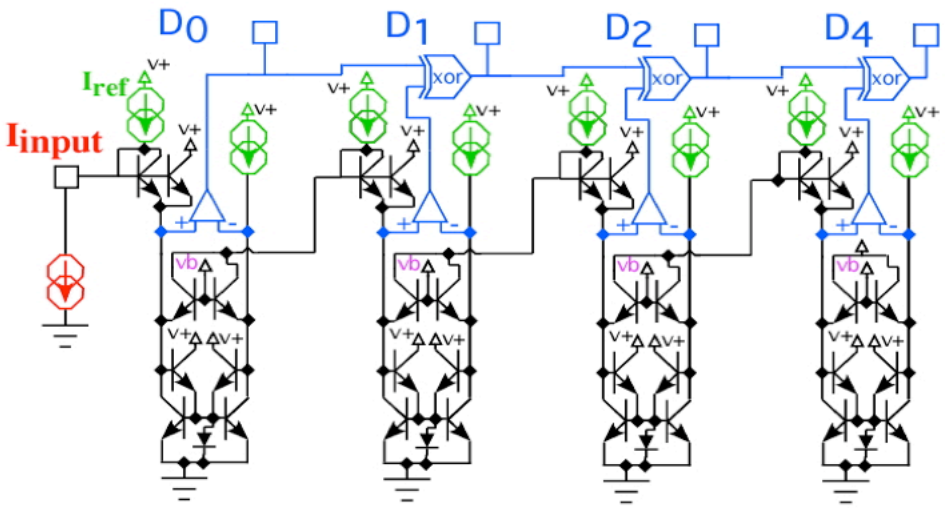
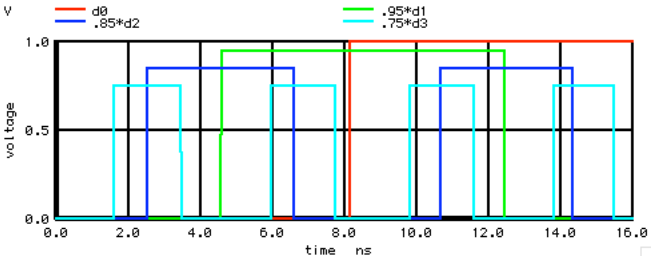
=========Can_Folding_ADC_Get_Any_Simplier?=========



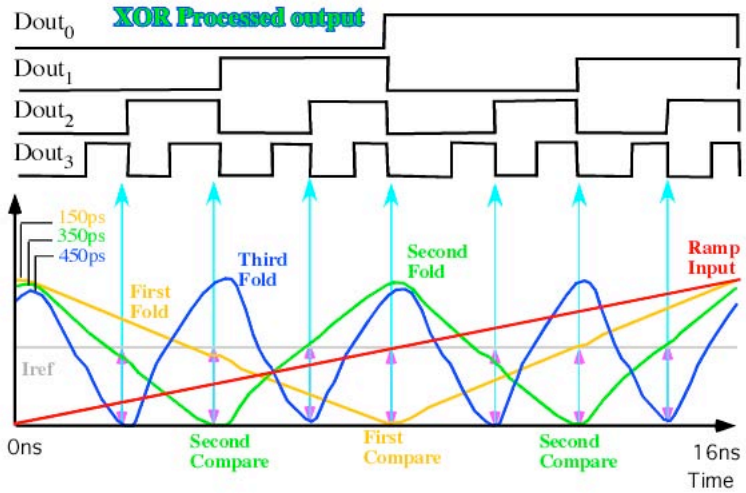
A Simple 4Bit 1GHz Level-Crossing A to D

(US Pat. 7839317)

Patent 7839317 added some further refinements such as adding a 2X current gain stage, and biasing the voltage clamping transistors with voltage source Vb to limit voltage swing to be around +/-50mV. Other than that, connecting 4 absolute current comparators in series is all that is needed to build a 4bit ADC. All the active signal path NPN transistors are shown above in black. Eight equal DC reference currents are shown in green.
The input current is shown in red. Using just these elements, the current comparator produces four differentialoutput voltages that are naturally gray coded (Shown below).
The symbolic blue circuity shows how a normal binary output can be derived.



This circuit was invented 40 years too late. It would have been possible to come out with this flash Analog to digital converter at the same time as the LM741 and LM555.
Only NPNs are in the signal path. They are all minimum geometry. And not many are needed.
It is not hard to translate an input voltage to a current.
The result would be a very fast voltage comparator which has a multi-bit digital output.
And it can track a moving input signal without needing a sample and hold.

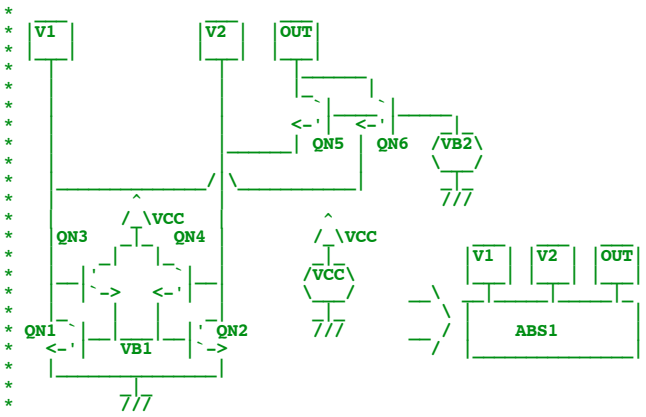


The signal folding and XOR digital processing are shown above for a 5GHz process.
A 16nsec ramp up currentis being tracked to produce a unique LSB step every 1nsec.
Remember that ftau is were emitter current is split equally between base and collector.
So the challenge will be to operate as close to ftau as possible.

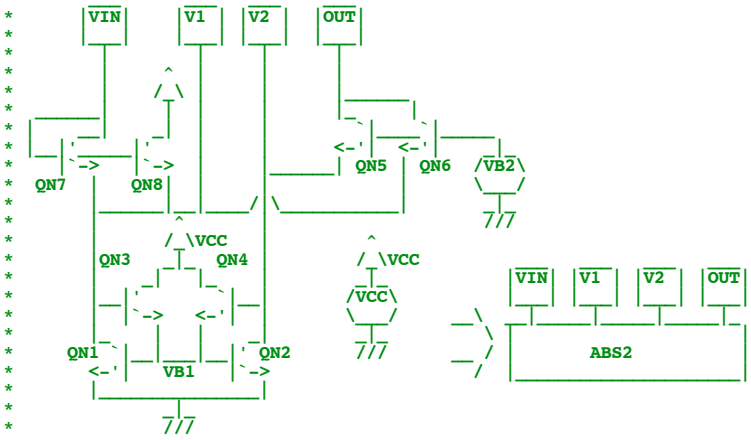
This invention is a different style of sampling data.
Where as normal analog to digital sampling is done with a clock,
this sampling is being done only when something happens.
That completely changes the rules.

========Spice_Code==================================

```
ABS_ADC_16ns
*
* IIN    VCC
*    ^     ^           ^          ^          ^          ^          ^          ^
*   /_\   /_\          /_\VCC     /_\VC      /_\VCC     /_\VC      /_\VCC     /_\VCC
*    _|_   _|_ IREF0    _|_        _|_ IREF2   _|_        _|_        _|_        _|_
*  /_ _\ /_ _\        /_ _\      /_ _\      /_ _\      /_ _\IREF4 /_ _\      /_ _\ IREF6
*  \/ \/ \/ \/        \/ \/      \/ \/      \/ \/      \/ \/      \/ \/IREF5  \/ \/
*  /\_/\ /\_/\    R0  /\_/\      /\_/\   R1  /\_/\      /\_/\   R2  /\_/\      /\_/\   ^
*  \___/ \___/        \___/IREF1 \___/      \___/IREF3 \___/      \___/      \___/  /_\VCC
*     |     |          _|_        |          _|_        |          _|_        |     |
*    _|_   _|_        /_ _\      _|_        /_ _\      _|_        /_ _\     _|_   _|_
*   |V1| |V2| |OUT| |V3| |V4| |V5| |V6| |V7| |V8| |V9| |V10| |V11| |V12| |V13| |V14|
*   |__| |__| |___| |__| |__| |__| |__| |__| |__| |__| |___| |___| |___| |___| |___|
*   _|_____|_____|_  _|_____|_____|_  _|_____|_____|_  _|_____|_____|_  _|_____|_____|_
*  |     ABS1     | |      ABS2A     | |      ABS2B     | |      ABSC      |
*  |_______________| |________________| |________________| |________________|
*
*
.OPTIONS GMIN      =1e-12  METHOD     =TRAP   set srcsteps = 1
VCC     VCC  0     DC  4
IIN     VCC  V1    PWL(  0 0 16n 2m 320n 0 520n 2m)

.tran   .01n    16n

BD0     D0    0     V = u(V(V1)-V(V2))
BD1     D1    0     V = u(V(V4)-V(V5))
BD2     D2    0     V = u(V(V8)-V(V9))
BD3     D3    0     V = u(V(V12)-V(V13))
*BD4    D4    0     V = u(V(V16)-V(V17))

XXOR1   D0    D1     VXOR1  XOR
XXOR2   D2    VXOR1  VXOR2  XOR
XXOR3   D3    VXOR2  VXOR3  XOR

IREF0   VCC  V2    1m
XABS1   V1   V2    OUT   ABS1
R0      OUT  V3    1

IREF1   VCC  V3    1m
IREF2   VCC  V5    1m
XABS2A  V3   V4    V5   V6   ABS2
R1      V6   V7    1

IREF3   VCC  V7    1m
IREF4   VCC  V9    1m
XABS2B  V7   V8    V9   V10  ABS2
R2      V10  V11   1

IREF5   VCC  V11    1m
IREF6   VCC  V13    1m
XABS2C  V11  V12    V13   V14  ABS2
R3      V14  VCC    1

.model npnv2  npn ( is=1e-18 bf=300 )


.model     npnv2         npn (
*=========================================================
+IS=1.1E-17    NF=1.0       BF=320      VAF=330      IKF=6e-03
*=========================================================
+CJE=2E-14     VJE=0.65     MJE=0.3
+CJC=2E-14     VJC=0.65     MJC=0.3
+CJS=3E-14     VJS=0.35     MJS=0.19    XCJC=0.42
+TF=2E-11      XTF=1.25     VTF=1       ITF=0.0035
+TR=6E-09      FC=0.9       PTF=210
*=========================================================
+KF=1.0E-16    AF=1
+XTB=1.4       EG=1.11      XTI=8      TNOM=25 )

.model     npnv         npn (
*=========================================================
+IS=1.1E-17         BF=320
*=========================================================
+CJE=2E-14
+CJC=2E-14
+CJS=3E-14
+TF=4E-11  )

.SUBCKT  XOR  A  B    C
BXOR     C    0  V = V(A)*(1-V(B)) + V(B)*(1-V(A))
.ends
```




```
.SUBCKT ABS1 V1    V2   OUT
QN1      V1   VB1   0    npnv      1
QN2      V2   VB1   0    npnv      1
QN3      VC   V1    VB1 npnv      1
QN4      VC   V2    VB1 npnv      1
QN5      OUT  VB2   V2   npnv      1
QN6      OUT  VB2   V1   npnv      1
VC       VC   0     DC   4
VB2      VB22 0     DC   2.15
RB2      VB22 VB2   20k
RB1      VB1  0     60k
.ends
```




```
.SUBCKT ABS2 VIN   V1  V2       OUT
QN1      V1   VB1   VE1  npnv      1
QN2      V2   VB1   VE2  npnv      1
QN3      VCC  V1    VB1  npnv      1
QN4      VCC  V2    VB1  npnv      1
QN5      OUT  VB2   V2   npnv      1
QN6      OUT  VB2   V1   npnv      1
QN7      VIN  VIN2  V1   npnv      1
QN8      VCC  VIN2  V1   npnv      1.02
VCC      VCC  0     DC   6
VB2      VB22 0     DC   2.45
RB2      VB22 VB2   1m
RB1      VB1  VBB   8k
QN7B     VBB  VBB   0    npnv      1
RBP      VIN  VIN2  1
RQ1      VE1  0     200
RQ2      VE2  0     200
VCL      VCL  VB2   DC   .4
*QCL     VCC  VCL   OUT  npnv      1

.ends


.control
set    pensize = 2
run
plot  v(v3) -v(out)  v(v7) -v(v6) v(v11) -v(v10)
plot  v(v3) -v(out)  v(v7) -v(v6) v(v11) -v(v10) xlimit 320n 520n

plot  d0     .95*d1        .85*d2        .75*d3
plot  v(d0)  .95*v(vxor1)  .85*v(vxor2)  .75*v(vxor3)
.endc
.end


8.18.11_1.47PM
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```