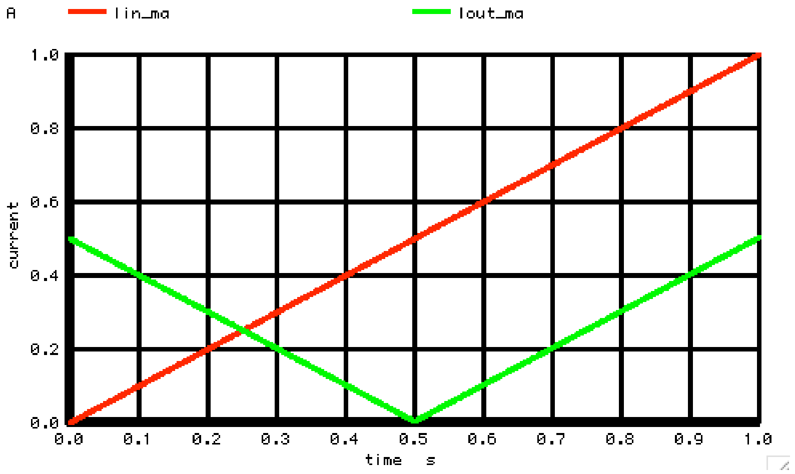
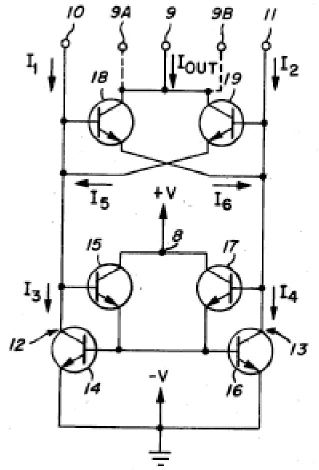
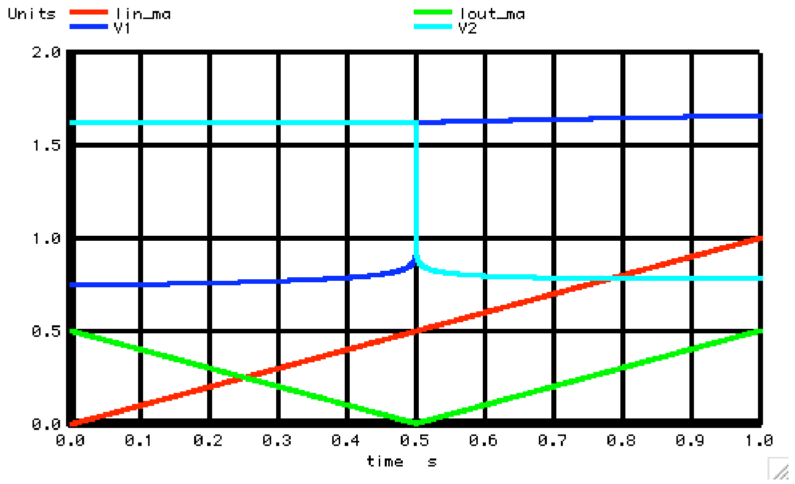
===ABSOLUTE_VALUE_CURRENT_COMPARATOR===========

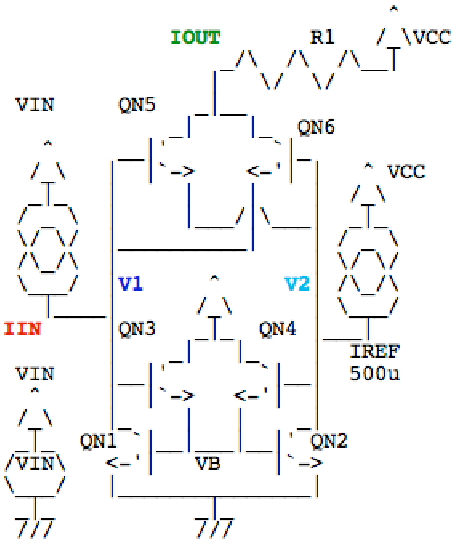


4,069,460
Current comparator circuit



While reading about various folding ADC architectures,
some of the input/output waveforms appeared to be very familiar.
As it turns out, patent 4069460 happens to produce a folding pattern
to the output current when a ramp input current is applied.





It just so happens that an absolute value current comparator
both binary compares and folds an input current at the same time.
The principle is that the currents in QN1 and QN2 are always equal.
A 500uA DC current is applied to node V2.
When the input current Iin is zero, QN1 gets its 500uA current from QN6.
When the input current Iin is 500uA, no current to flow through QN5 or QN6.
And when Iin is 1000uA, 500uA flow thru QN5.

So the circuit is doing a current comparison of the input current.
When Iin is less than Iref, then V2 is 600mV higher that V1.
And the reverse is true when Iin is greater then Iref.
Transistors QN5 and QN6 clamp V2 and V1 to prevent QN1 and Qn2 from saturating.
And as a side benefit, the output current follows this equation.

IOUT = ABS(Iin - Iref)

In other words, the input current gets folded around the reference current to the output at the same time it is compared to a reference current to produce a differential output voltage.

========Spice_Code==================================

```
ABSOLUTE_VALUE_COMPARATOR
*
*                                  ^
*                 VOUT       R1   /_\VCC
*                     _/\  /\  /\__|
*                    |   \/  \/
*     VCC     QN5   _|__
*                 _|    |_  QN6
*       ^     __|'        `|_
*      /_\   |  |`->    <-'| |   ^ VCC
*      _|_   |     |    |    |  /_\
*     / _ \  |     |___/|\___|  _|_
*     \/ \/  |__________|    | / _ \
*     /\_/\  |               | \/ \/
*     \___/  |V1     ^     V2| /\_/\
*       |____|      /_\      | \___/
*    IIN     |QN3   _|_  QN4 |___|
*            |    _|   |_    |  IREF
*     VCC    |__|'       `|__|  500u
*      ^     |  |`->   <-'|  |
*     /_\    |_    |   |    _|
*     _|_  QN1 `|__|___|__|' QN2
*    /VIN\   <-'|   VB    |`->
*    \___/   |_______________|
*     _|_           _|_
*     ///           ///
*

.OPTIONS GMIN      =1e-18  METHOD     =trap
IIN     VIN  V1    PWL(  0 0 1 1m )
Iref    0    V2    .5m
VCC     VCC  0     DC  2
VIN     VIN  0     DC  2
R1      VOUT VCC   1
QN1     V1   VB    0   npnv     1
QN2     V2   VB    0   npnv     1
QN3     VCC  V1    VB  npnv     1
QN4     VCC  V2    VB  npnv     1
QN5     VOUT V1    V2  npnv     1
QN6     VOUT V2    V1  npnv     1

.tran   1m    1
.model npnv  npn ( is=1e-18 bf=300 )
.control
set    pensize = 3
run
let Iin_ma = -i(vin)*1000
let Iout_ma = -i(vcc)*1000

plot  v(vcc) -v(vout)
plot  -i(vcc)
plot  -i(vin)
plot  v(v1)
plot  v(v1)  ylimit 0 2

plot  Iin_ma  Iout_ma  V1 V2
plot   Iin_ma  Iout_ma

.endc
.end
```

8.18.11_1.24PM
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